A 10-Bit 100-MSample/s Pipelined Analog-to-Digital Converter Using Digital Calibration Technique

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Abstract: *This paper presents a 10-bit 100-Msample/s pipelined analog-to-digital converter (ADC) using the foreground mode of calibration technique proposed in* [1]. *This technique can overcome the capacitors mismatch, gain error, and amplifier nonlinearities. Simulation results show that the ADC achieves a peak signal-to-noise-and-distortion ratio (SNDR) of 64 dB, a peak spurious-free dynamic range (SFDR) of 74 dB, a differential nonlinearity (DNL) of 0.12 least significant bit (LSB) and a integral nonlinearity (INL) of 0.3 LSB for a sinusoidal input signal with 30 MHz frequency. The ADC core* (*without calibration circuitry*) *consumes 27mW power from a 1V supply voltage in a 90-nm CMOS technology.*

Keywords: Pipelined ADCs, capacitor mismatch, gain error, amplifier nonlinearities, digital calibration.

1. Introduction

Design of high-performance pipelined ADCs is an interesting topic in the ADC concept. As device dimensions and supply voltages are scaled down, design of high speed and high resolution pipelined ADCs becomes more challenging. Capacitor matching and high-gain amplifiers are the main issues in the design of high resolution pipelined ADCs [2-4].

A common way to overcome the performance limitations in pipelined ADCs is to employ a calibration technique. Generally, there are two types of calibration methods. First types are named foreground calibration methods where the converter normal operation is stopped and then the error measurement process is performed. In this case, if the error sources change over the time, a new calibration cycle has to be started [5]. Second types of calibration techniques operate in the background where they improve the ADC linearity without interrupting the converter normal operation [5]. When calibration is done in the digital domain, it can take advantage of scaling. The cost of this calibration technique is the increased complexity in the digital domain, but, the area and power dissipation in digital part can be reduced through scaling.

This paper describes a pipelined ADC where calibrated with foreground mode of digital calibration technique reported by authors in [1], to achieve high-speed and high-resolution simultaneously without needing high precision analog building blocks. The paper is organized as follows. Sect. 2 describes the ADC architecture. The calibration technique is presented in Sect. 3. Section 4 addresses the circuit design of the ADC building blocks. Section 5 presents the circuit simulation results. The conclusions are given in Sect. 6.

2. ADC architecture

Pipelined ADCs are composed of several low-resolution stages. In each stage, the input is sampled and quantized by the sub-ADC, and then the residue signal is amplified using a switched-capacitor multiplying digital-to-analog converter (MDAC). The ADC general block diagram is shown in Fig. 1. Commonly, 1.5-bit/stage architecture is used for high speed pipelined ADCs [6]. Each 1.5-bit stage is composed of a 1.5-bit sub-ADC and a 1.5-bit MDAC circuit. With bit redundancy and digital correction in a 1.5-bit/stage configuration, pipelined converters are insensitive to offset errors in their sub-ADCs and amplifiers, and the errors mainly stem from the gain errors and nonlinearities in the amplifiers [2, 3].

A circuit implementation of the 1.5-bit stage is shown in Fig. 2. During sampling phase, ϕ_1, the input voltage is sampled on sampling capacitor C_S and the feedback capacitor, C_F, is discharged. During the next phase, ϕ_2, the capacitor C_F is switched in the amplifier feedback loop, while the capacitor C_S is switched to $\{-V_{ref}, 0, V_{ref}\}$ depending on the sub-ADC output, D. This configuration is chosen instead of the commonly used capacitor flip-around configuration; because here, signal and the sub-DAC output see the same gains and hence the calibration process is simplified [3].

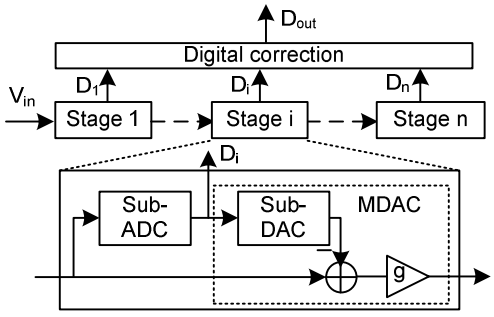

Fig. 1: General block diagram of pipelined ADCs.

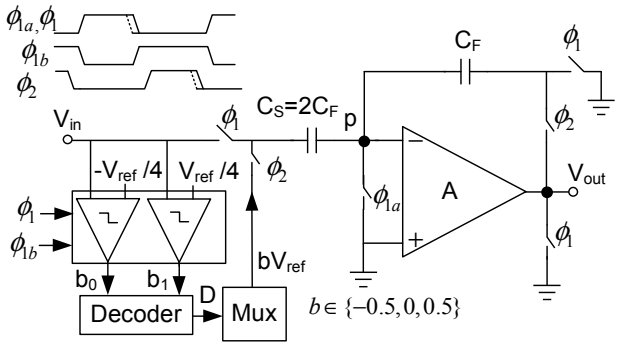

Fig. 2: Switched capacitor implementation of 1.5 bit stage and its timing.

3. Calibration technique summary

As mentioned in [3], by defining the digital equivalent of stage input and output signals as D_{out} and D_{in}, and D as sub-ADC digital output, the digital equivalent of stage input can be expressed as:

$$D_{in} = D_1 + \beta_1 D_{out} + \beta_3 D_{out}^3 \quad (1)$$

If coefficients β_1 and β_3 are available, the inverse function of the stage is resulted. By extending this result to all stages of ADC, the inverse function of ADC is obtained and the ADC input signal is digitized without any dependency to the analog elements preciseness [1]. Hear, the measurement of coefficients β_1 and β_3 is done by using the constant calibration signals without any dependency to their accuracy. The ADC has 12 1.5 bit stages and a 2 bit flash backend ADC. The linear and nonlinear term coefficients in (1) is measured for stages 1 and 2 where in the stages 3 to 8 the linear term coefficients are only measured. In this paper, the foreground mode of calibration technique reported in [1] is used for coefficients measurement.

In the foreground calibration method, the ADC normal operation is stopped and the calibration signal is injected to the ADC. To calibrate the i^{th} stage, firstly it is supposed that the stage suffers just from the linear error (i.e. $\beta_3=0$) and the backend stages are calibrated so that the stage output is perfectly digitized by backend stages

$$D_{in,i} = D_i + \beta_{1i} D_{out,i} \quad (2)$$

For calibration, the i^{th} stage is configured as two-mode stage. Consider that a constant calibration signal with the value slightly great than $0.25V_{ref}$ (comparator threshold voltage) is applied to the stage input. The calibration signal is digitized in two different modes. First, as shown in Fig. 3(a), the stage is configured in normal operation mode and its sub-ADC output, D_i=1, and the digitized output for $0.25V_{ref}$ with backend stages, $D_{out1,i}$, are stored in a memory. Second, the stage is configured as multiply-by-two configuration (Fig. 3(b)) and the digitized output for the same calibration signal, $D_{out2,i}$, is also stored in a memory. With these two stored data and from (1) with β_3= 0, the digitized stage input are obtained as:

$$\begin{aligned} D_{in1,i} &= D_i + \beta_{1i} D_{out1,i} \\ D_{in2,i} &= \beta_{1i} D_{out2,i} \end{aligned} \quad (3)$$

where β_{1i} is i^{th} stage linear term coefficient. Because the stage input is the same in the two modes, $D_{in1,i} = D_{in2,i}$, so:

$$\beta_{1i}(D_{out2,i} - D_{out1,i}) = D_i \quad (4)$$

Therefore the stage coefficient can be extracted from two stored values and the stage sub-ADC output in normal mode operation. To simplify the needed hardware in the coefficient extraction, we can use the Least Mean Square (LMS) algorithm [7] as:

$$\beta_{1i}(n+1) = \beta_{1i}(n) + \mu.e(n).D_{out,i} \quad (5)$$

where μ is the LMS algorithm update step size, n is update index and

$$e(n) = 1 - \beta_{1i}(n)(D_{out2,i} - D_{out1,i}) \quad (6)$$

Hence, without any dependency to the accuracy of the calibration signal, the stage linear error is extracted. By extending the applied technique, the nonlinear term coefficient in the stage inverse function, (1), can also be extracted.

If the full swing input is applied to the amplifier, the maximum deviation is obtained from the ideal input-output faction of the amplifier. With this view, another calibration signal with a value of $0.5V_{ref}$ is used. Because the stage should be configured in multiply-by-two mode, so the maximum input that caused the stage output to reach to its maximum value is $0.5V_{ref}$. Since the amplifier has the offset error, the input cannot be as large as this value. So, for nonlinear error extraction, a second calibration signal is applied to the stage with a value slightly less than $0.5V_{ref}$. In this condition for linear and nonlinear term coefficients extraction, two discussed calibration inputs are applied in the two different mentioned modes and the results are stored in the memory. With these stored results we have:

$$\begin{aligned} D_{in1,i} &= D_i + \beta_{1i} D_{out1,i} + \beta_{3i} D_{out2,i}^3 \\ D_{in2,i} &= \beta_{1i} D_{out2,i} + \beta_{3i} D_{out2,i}^3 \end{aligned} \quad (7)$$

Hence, the coefficients are extracted as follows:

$$\begin{aligned} \beta_{1i}(n+1) &= \beta_{1i}(n) + \mu_1.e(n).(D_{out2,i} - D_{out1,i}) \\ \beta_{3i}(n+1) &= \beta_{3i}(n) + \mu_3.e(n).(D_{out2,i}^3 - D_{out1,i}^3) \end{aligned} \quad (8)$$

where μ_1 and μ_3 are the update step size of LMS algorithm in the coefficients extraction and:

$$e(n) = 1 - \beta_{1i}(n)(D_{out2,i} - D_{out1,i}) - \beta_{3i}(n)(D_{out2,i}^3 - D_{out1,i}^3) \quad (9)$$

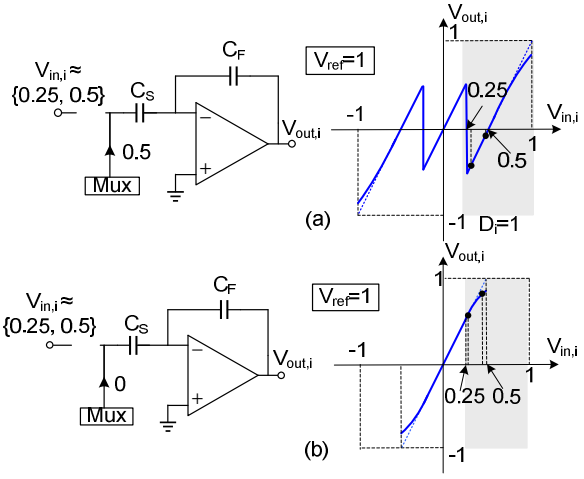

Fig. 3: The i^{th} stage transfer function (a) Normal operation mode (b) Multiply-by-two mode.

4. ADC circuits implementation details

A 10-bit 100MS/s pipelined ADC has been designed in a 90-nm CMOS technology with 1-V power supply using the proposed calibration method. The detailed circuit implementation of this ADC is described in this section.

4.1 The ADC input sample and hold circuit

Using an input sample and hold circuit relaxes the timing requirement of the first MDAC [3] although this circuit is power hungry. Without this S/H the timing mismatch between the first stage sub-ADC and MDAC paths is critical and can degrade the ADC performance if the amount of mismatch to be large.

The redundancy used in the 1.5bit/stage structure can alleviate this problem, but, it must be ensured to leave enough margin for comparators' offset voltage. So a reasonable path matching must be done [3]. Approximately the same path for sub-ADC and MDAC in the first stage can be done by using the special timing in the sub-ADC comparators to minimize the path mismatch where the sufficient settling time for the MDAC is remained. This timing is shown in Fig. 5.

4.2 Amplifiers

The main blocks that determine the speed and power consumption of the ADC are primarily its amplifiers. As shown in Fig. 4, a two stage Miller compensated amplifier with two cascaded common source amplifiers is used as ADC amplifiers. This amplifier has large output swing with low DC gain. The pMOS input pair is chosen due to its low input common-mode voltage. This simplifies the design of switches connected to the amplifier inputs where simple nMOS switches can be utilized. A simple switched capacitor common mode feedback (CMFB) circuit is used to control the common mode voltage of the output nodes. The bias current of the output stage is defined as a multiple of first stage tail transistor (M11) through the current mirror devices. The ADC first stage amplifier transistor sizes are shown in Table I. Minimum channel length devices are used in amplifying transistors to achieve higher bandwidth. But, this limits the DC gain only to 38dB. For ADC second stage, the amplifier elements are scaled down by a factor of 2 and in the rest stages, a scaling factor of 4 is used.

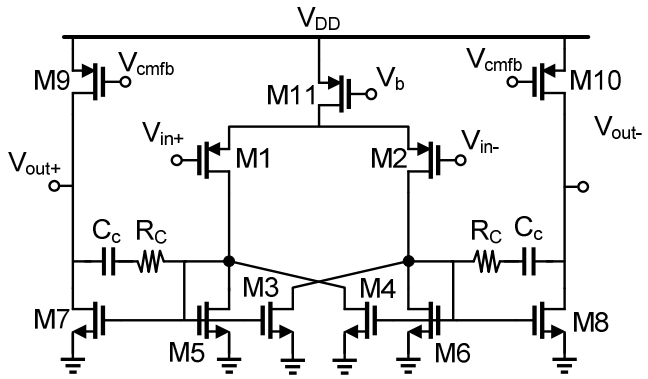

Fig. 4: Amplifier architecture.

TABLE I. First stage amplifier transistor sizes.

Parameter	size
M1,2	8×6μm/0.09μm
M3,4	3×4μm/0.18μm
M5,6	3×4μm/0.18μm
M7,8	12×8μm/0.09μm
M9,10	24×24μm/0.18μm
M11	20×16μm/0.18μm
R_C ,C_C	60Ω,0.6pF

4.3 Comparators

For matching requirements without input S/H, the comparators in the first stage must rapidly regenerate to ensure the MDAC has enough time for adequate settling. Figure 5(a) shows the single-ended implementation of the comparator used in the sub-ADCs where the reference voltage is realized by capacitors ratio [8]. In this structure, C_{in}=80 fF and C_{ref}=20 fF are used for $\pm 0.25 V_{ref}$ realization. Moreover, because of redundancy, a simple dynamic latch [8] shown in Fig. 5(b) is employed.

4.4 Sampling switches

The switches in the sampling network need whole ADC linearity. Due to low power supply voltage, the bootstrapping technique is utilized to realize highly linear switches. The sampling switches of the first stage is tested in the sampling circuit and have the distortion components about 72 dB below the full-scale at the Nyquist frequency input.

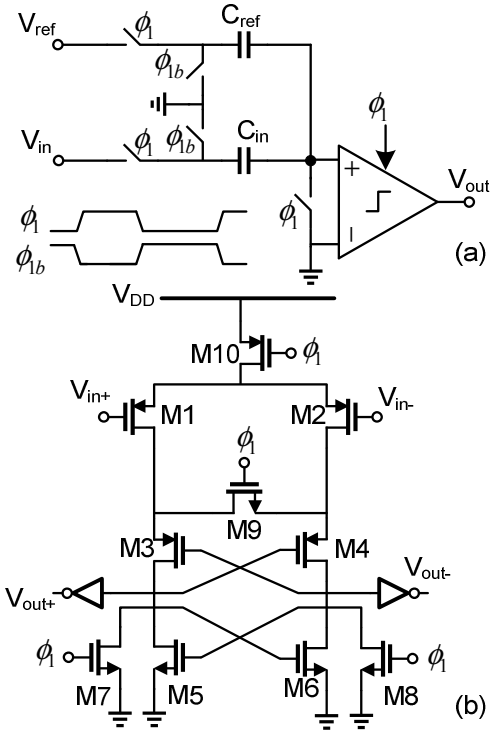

Fig. 5: (a) Comparator architecture and (b) dynamic latch.

4.5 Sampling capacitors

With thermal noise considerations, the stages 1 and 2 have 0.8 pF and 0.4 pF sampling capacitors, respectively, and the rest stages use 0.2 pF sampling capacitor where the

maximum 0.1% capacitor mismatch is considered in each stage.

4.6 Two-mode stage

As mentioned in Sect. 3, the calibration algorithm needs a two-mode stage. This is simply implemented by two-mode multiplexer in the sub-DAC realization. In normal operation mode of stage, the multiplexer is controlled with sub-ADC digital outputs and the respective voltage is connected to its output as DAC voltages. In the multiply-by-two mode, the multiplexer outputs have the common mode voltage to realize a gain of 2 in the MDAC.

5. Simulation results

The ADC has been simulated in standard 90-nm CMOS technology with 1-V supply voltage. The analog circuits are simulated in HSPICE where the calibration process is implemented with MATLAB.

Figures 6 and 7 plot the simulated DNL and INL before and after the calibration, respectively, at a sampling frequency of 100 MHz. With 0.1% capacitors mismatch, the uncalibrated ADC has a peak INL of 10 LSB. After calibration, the peak INL falls to bellow 0.5 LSB. Figure 8 shows the simulated output spectrum for a 48 MHz, 1-V peak-to-peak differential analog input sampled at 100 MHz.

To evaluate the ADC performance in the Nyquist band, the SNDR and SFDR are calculated for several input signal frequencies. The peak SNDR and peak SFDR are equal to 64 dB and 74dB, respectively, after calibration (Fig. 9). The number of iterations in the LMS algorithm for each stage (with μ_1=1/256 and μ_3=1/1024) is about 2^{12} ADC sampling periods, so the total calibration time is about 8×2^{12} ADC sampling periods.

The achieved performance for the simulated pipelined ADC and the comparison with recently reported ADCs is shown in Table II using a figure of merit (FoM) defined by:

$$FoM = \frac{Power}{2^{ENOB} \times f_S} \qquad (10)$$

where *Power* and f_S refer to the ADC power consumption and sampling frequency, respectively, and *ENOB* shows its effective number of bits [9]. The designed ADC achieves the lowest *FoM* although the comparison is not completely fair since the simulation results reported here are compared with the measurement results.

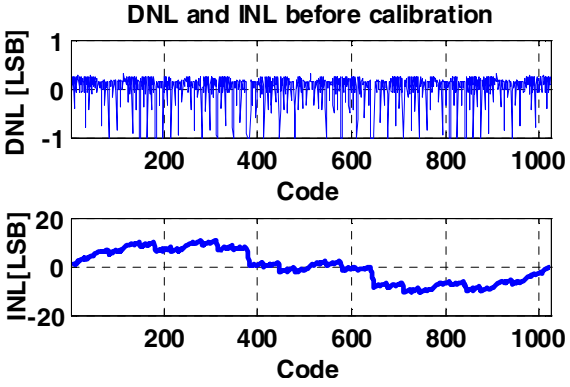

Fig. 6: Simulated INL and DNL before calibration.

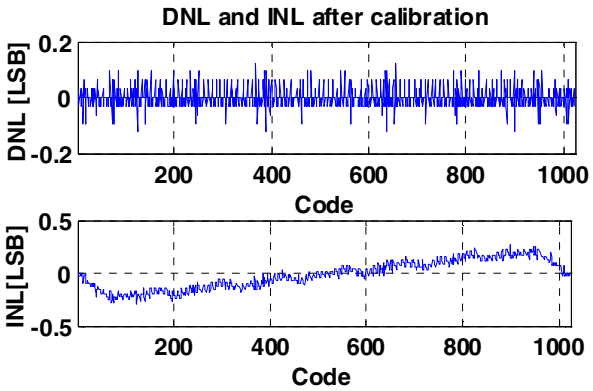

Fig. 7: Simulated INL and DNL after calibration.

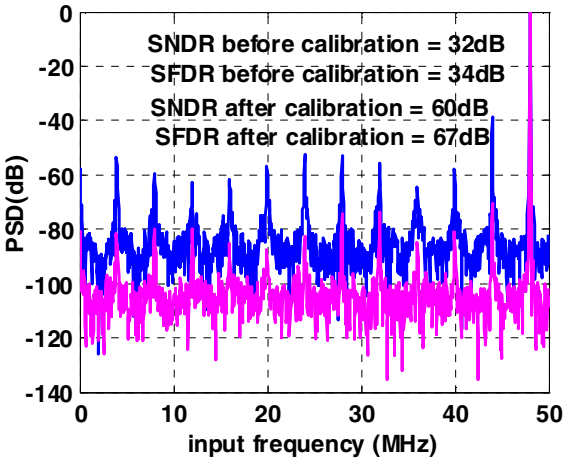

Fig. 8: Simulated output spectrum.

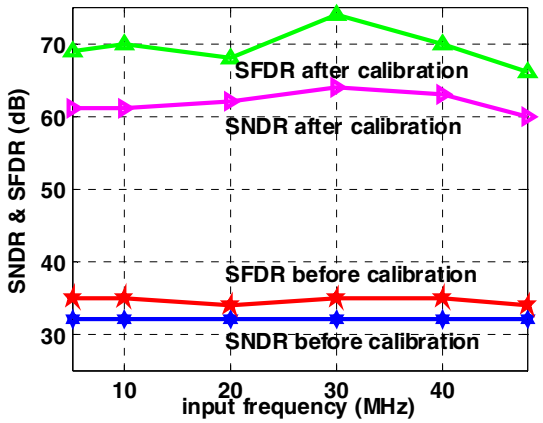

Fig. 9: SNDR and SFDR vs. ADC input signal frequency.

TABLE II. Performance comparison of the simulated ADC.

Ref.	Process	V_{DD} (V)	f_s (MS/s)	INL (LSB)	DNL (LSB)	SFDR (dB)	SNDR (dB)	Analog power (mW)	FoM (pJ.V/step)
This work	90nm	1	100	±0.3	-0.12	74	64	27	0.21
[2]	0.25µm	2.5	80	+0.24	+0.09	84.5	72.6	340	1.2
[3]	90nm	1.2	200	+1.3	+0.59	-	64	348	1.33
[9]	90nm	1.2	500	1	0.4	-	52	55	0.33
[10]	90nm	1.2	100	3.6	0.54	85	69.8	93	0.37

6. Conclusions

In this paper a 10-bit 100-Msample/s pipelined ADC is designed using a digital calibration technique. The capacitors mismatch, gain errors, and amplifier nonlinearities are digitally calibrated. The circuit level simulation results verify the usefulness of designed pipelined ADC.

Acknowledgements

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