A Simple Digital Background Gain Error Calibration Technique for Pipelined ADCs

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***Abstract*— This paper presents a simple digital background calibration technique to eliminate the gain errors of 1.5bit/stage pipelined analog-to-digital converters caused by finite DC gain of stage amplifiers. In this technique, the gain errors are extracted by creating a mismatch between stage sub-ADC threshold voltages in the "split ADC" architecture derived from [1] and [2]. The technique is tested on a prototype 12bit 1.5bit/stage pipelined ADC with maximum 50dB amplifier DC gain. MATLAB and Simulink environment simulations show 19dB SNDR and 45dB SFDR improvements after calibration technique is applied on the first four stages of the ADC, which were limited to 52dB and 55dB before calibration.**

Keywords-Pipelined ADCs; Gain errors; Digital background calibration, Split ADC

I. INTRODUCTION

Analog to digital converters (ADCs) are identified as large mixed-signal circuits that widely used in signal processing circuits and systems. Among various ADC architectures, the pipelined converter is proved to be very efficient for high speed and medium to high resolutions. As shown in Fig. 1, a pipelined ADC is composed of several low-resolution stages. In each stage, the input is sampled and quantized by the sub-ADC, and then the residue signal is amplified to fit into the next stage's full-scale range using a switched-capacitor multiplying digital-to analog converter (MDAC) circuit.

The most limiting parameters of a highly linear pipelined ADC are the capacitor mismatch, finite DC gain in amplifiers and offset voltage in amplifiers and comparators. The offset voltage error is tolerated using a digital redundancy technique and in highly linear pipelined ADC, if for *kT/C* noise considerations the capacitance values are chosen sufficiently high, then no digital calibration is needed to overcome the capacitor mismatch [3] while it is necessary to use calibration techniques to reduce the errors produced by finite DC gain as the technologies scale down.

There are several approaches to improve the accuracy of these ADCs which can be categorized into two groups: analog element calibration and digital one [4]. In the first group, the errors are corrected by adjusting the ADC elements in the analog domain. The analog calibration has two drawbacks. First, any temperature and power fluctuations may degrade its performance. Second, this calibration technique is not an economically optimum solution in spite of digital techniques which use modern mixed-signal technologies advantageous to correct the errors in the digital domain [4]. The digital calibration can be performed in two forms. In foreground techniques, the process is done by stopping the ADC normal conversion while in background techniques, the ADC is always working. In the background methods, the errors are measured by a slow but accurate ADC such as a sigma-delta ADC [5], statistical-based method [1] or the "split ADC" concept [2] and then the parameters are corrected in the digital domain. In this paper, a digital background calibration technique is proposed that uses the "split ADC" concept to eliminate the gain errors in pipelined ADCs caused by finite DC gain of the stage amplifiers.

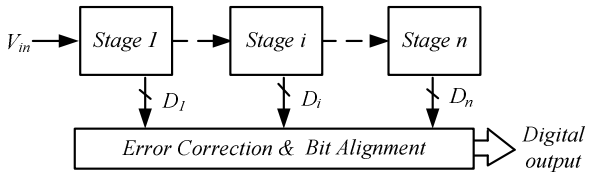

Figure 1. General block diagram of pipelined ADCs.

This paper is organized as follows. Section II reviews the conventional high speed pipelined ADCs. Then gain error modeling in pipelined ADC stages are introduced in section III. Section IV details the proposed calibration method. Simulation results are presented in section V, and section VI concludes this paper.

II. CONVENTIONAL HIGH SPEED PIPELINED ADCS

Conventional high speed pipelined ADCs with *N* bits of resolution, consist of *N-2* identical stages and a 2-bit flash ADC as a last stage. Each 1.5-bit stage is composed of a 1.5-bit sub-ADC and a 1.5-bit flip-around MDAC circuit. The single-ended circuit implementation of 1.5-bit stage is shown in Fig. 2. During sampling phase, Φ_s, the input voltage is sampled on two identical capacitors C_S and C_F then during the next phase, Φ_a, the capacitor C_F is switched in the opamp's feedback loop, while the capacitor C_S is switched to $\{V_{ref}, 0, -V_{ref}\}$ depending on the output of the sub-ADC. For linear amplifier and capacitors, the transfer function of the stage is given by,

$$V_{res} = (1+\gamma)\left((2+\alpha)V_i - (1+\alpha)bV_{ref}\right), \qquad (1)$$

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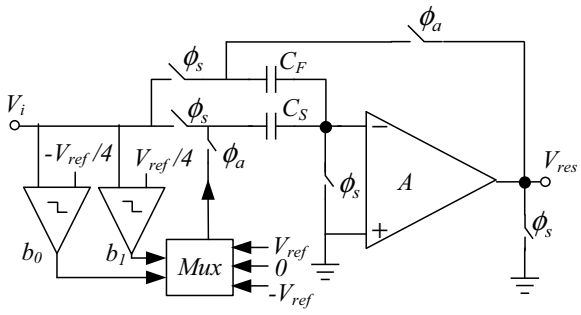

Figure 2. Single-ended circuit implementation of 1.5-bit stage.

$$1+\alpha = \frac{C_S}{C_F} \qquad 1+\gamma = \frac{1}{1+\frac{1}{A}(1+\frac{C_S}{C_F})}, \qquad (2,3)$$

where C_S and C_F are sampling and feedback capacitors respectively and A is the amplifier DC gain. In an ideal ADC, i.e. with no capacitor mismatch and infinite amplifier gain, the residue voltage of stage is simplified to,

$$V_{res} = 2V_i - bV_{ref}, \qquad (4)$$

where b is {-1,0,1}, depending on the input voltage level.

III. Gain Errors Calibration

A. Linear Errors of the 1.5-bit/Stage Pipelined ADC

Equation (1) shows that the stage output is affected by two major nonideal factors, γ and α, which are resulted from finite opamp gain and capacitor mismatch. A linear modeling of these errors is shown in Fig. 3. As mentioned before, if the capacitance values are chosen sufficiently high according to the noise considerations, no digital calibration is needed to overcome the capacitor mismatch, so α is negligible in this equation and we can consider the stage as Fig. 4. Then, the stage output voltage, V_{res}, is digitized by the later ADC stages as backend ADC. The digital output, is obtained by adding the half of digital reference, $D[bV_{ref}]$ to the half of digitized residue, $D[V_{res}]$. In this case, what is subtracted in the MDAC can be restored digitally, however, the analog reference subtracted in (1) is affected by γ, and it does not match with the ideal digital reference. Fig. 5(a) shows this effect in the stage transfer curve. Hence, the linearity of pipelined ADCs is affected by gain errors of the stages. Since $(1+\gamma)V_{ref}$ is subtracted in the analog domain, but the ideal $D[bV_{ref}]$ is added in the digital domain, a mismatch error occurs at the comparator threshold point and the ADC shows nonlinearity in its performance.

B. Digital Calibration Concept

The mismatch between the analog reference, V_{ref}, and the digitized reference, $D[V_{ref}]$ can be eliminated by reducing the non-ideal factors in the analog domain or adjusting in the digital domain. The analog implementations usually increase the circuit complexity, especially at low supply voltages. In the digital implementation, only the digital reference needs to be adjusted to match the nonideal analog [1] .Thus, the analog reference should be measured accurately with the back-end ADC. The digital calibration concept is explained in Fig. 5(b). While $b(1+\gamma)V_{ref}$ is subtracted in the MDAC, the digital value of $D[b(1+\gamma)V_{ref}]$ is added back instead of the ideal $D[bV_{ref}]$ to eliminate the mismatch error. Even after this calibration, the overall gain slope error remains, but the gain slope correction is not necessary since the ADC transfer function is linear [1].

Therefore,

$$D_{out} = 0.5(D[V_{res}] + b.D[(1+\gamma)V_{ref}]), \qquad (5)$$

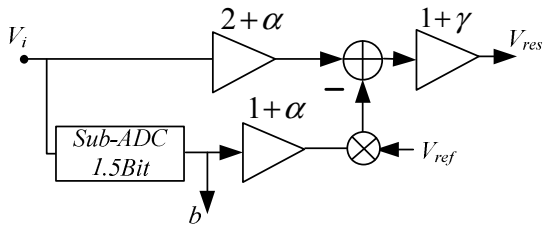

Figure 3. Linear errors modeling in 1.5 bit stage.

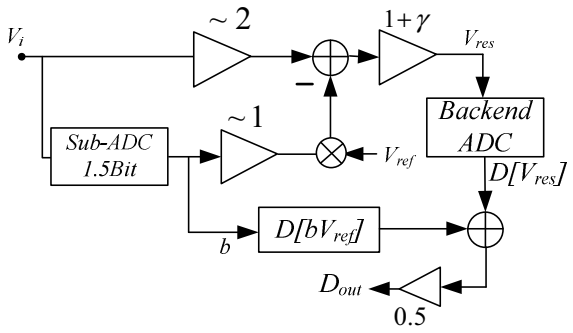

Figure 4. Simplified stage model and digital output calculation.

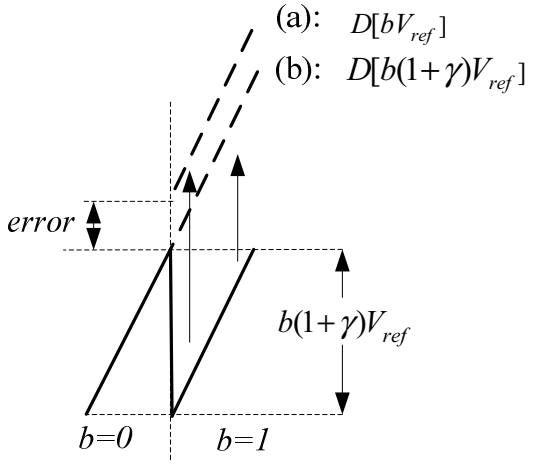

Figure 5. Gain error effect in transfer curve, (a) without calibration (b) with calibration.

There are several methods to measure these errors, such as statistical method used in [1] or applying a sigma- delta ADC as mentioned in [5]. In this paper, a simple concept known as "Split ADC" derived from [1] and [2] is used to measure the errors. In split architecture the ADC is split into two channels, each converting the same input and producing individual output codes and the average of the two outputs is reported as the ADC output code. The background calibration signal is developed from the difference between codes. If both ADCs are correctly calibrated, the two outputs will agree, and the difference will be zero. The concept of this architecture is shown in Fig. 6. Since the final ADC output is generated by sum of the two ADC outputs, each ADC can be designed with half of the capacitance to meet thermal noise requirements, thus each ADC consumes approximately half of the power and area required in a single ADC designed for the same resolution [2].

As mentioned in [2] the split ADC concept is not sufficient for error estimation by itself, because if the errors of the channels are equal, the difference between the channels will become zero that is incorrect.

IV. Proposed Calibration Technique

A. Stage Analog Reference Measurement

Here a simple technique is used to measure the analog V_{ref}. Assuming errors just in the first stage, all of the next stages are lumped into a backend as an ideal independent ADC to digitize the first stage analog output. In this method, the calibration signal is produced by shifting channel "A" first stage sub-ADC threshold voltages in split architecture, as shown in Fig. 7. If two channels are the same, the non-zero difference between their outputs is resulted from this shifting. We must consider that the threshold shifting must be less enough to limit the residue voltage to the full range voltage, (i.e. V_{ref}). In the 1.5 bit stage, this shifting must be less than $1/4V_{ref}$. This region is given up for the offset compensation in sub-ADC thresholds. So, we divide this region into two parts, half for offset compensation and the rest for the threshold voltages shifting, thus the voltage shifting value is equal to $1/8V_{ref}$. In this case, despite the calibration signal is generated from the difference of the two channels outputs, the final digital output is the same when there is no shift, because this created mismatch in sub-ADC can be solved by the redundancy used here.

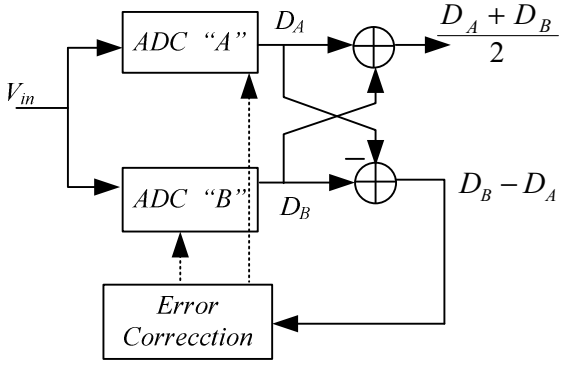

Figure 6. Split ADC concept.

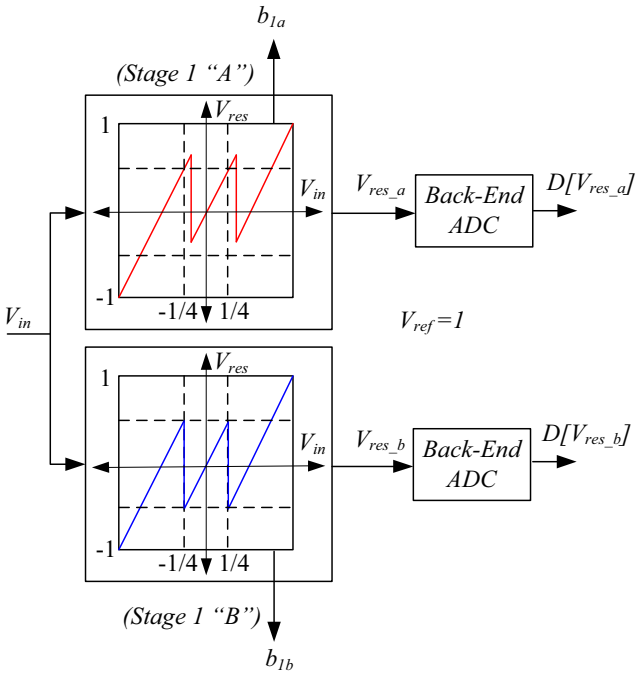

Figure 7. Proposed method for the errors extraction.

To simplify the calibration algorithm, assume that the first stages in paths *A* and *B* have the same error as mentioned in [6]. Fig. 8 helps to understand this calibration concept. Input voltage of stages is identical all the time and except at the regions *i* and *ii,* stages residue voltage are equal, so we can measure these gaps as the analog V_{ref} using the difference of two digitized residue voltages.

$D[V_{res\text{-}b}]$ and $D[V_{res\text{-}a}]$ in Fig. 7 are the digital forms of first stages residue voltages while in Fig. 8 at the regions *i* and *ii* we have

$$b_{1a} - b_{1b} = -1\,, \tag{6}$$

By subtracting the two digital forms of residue voltages, the input signal is deleted and the analog V_{ref} is extracted using

$$D[V_{res\_a}] - D[V_{res\_b}] = (1+\gamma)V_{ref} + E_a - E_b\,, \tag{7}$$

where E_a and E_b are the backend ADC errors in channels A and B, respectively. By averaging (7), the analog V_{ref} is resulted and then the digital output is calculated from (5).

$$\overline{D[V_{res\_a}] - D[V_{res\_b}]} = (1+\gamma)V_{ref}\,, \tag{8}$$

B. Comparison with Conventional Methods

In this technique, the gain errors are calibrated by creating a mismatch between stages threshold voltage of sub-ADC in split structure while in [1], the gain error is measured by inserting a pseudo random calibration signal and statistical based methods which needs a long calibration time. On the other hand, since there is no calibration signal used here, its

construction and preciseness makes no trouble. In [2], the errors are measured by multimode sub-ADCs and in [6] only the first stage error is calibrated. The most important advantage of this method is low calibration time which is resulted from split structure.

However, the accuracy of the method is restricted by the backend ADC's accuracy and also channel mismatch. We can use additional stages in backend ADCs to increase its accuracy and use adaptive channel equalizing to decrease the channel mismatch. If the capacitor mismatch is not negligible in low resolution ADCs, we can use the architectures that are less sensitive to mismatch such as [7]. More over, the stage amplifier must be linear enough to makes no problem for this technique.

V. Simulation Results

The proposed technique was simulated behaviorally using MATLAB and Simulink environment. In these simulations, a 12 bit 1.5bit/stage 2-channel split ADC was used and the technique was applied on the first four stages, while using 8 bit ideal ADC as a backend considering 50dB DC gain for amplifiers. The technique implementation is started applying the calibration technique on the 4th stage and then coming to the first stage. The sub-ADCs of first four stages in channel "A" is considered as two modes ADC, where during stage calibration, threshold voltages are shifted by $1/8V_{ref}$ while after the calibration they are the same as channel "B" sub-ADCs. Circuit implementation of this condition is easy, the threshold voltage can be realized by capacitors ratio or transistors size in comparators. Here a simulation with 16384 full scale input samples (i.e. V_{ref}) shows the ADC achieves 71dB SNDR and 100dB SFDR after calibration while it was limited to 52dB SNDR and 55dB SFDR before calibration. Fig. 9 shows the ADC output spectrum before and after calibration while SNDR and SFDR versus input signal frequency before and after calibration are illustrated in Fig. 10 and Fig. 11. These plots express the efficiency of the proposed technique for different input frequencies.

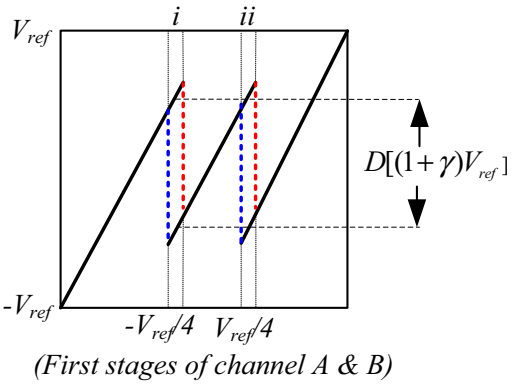

Figure 8. The transfer curve of first stages in split ADC.

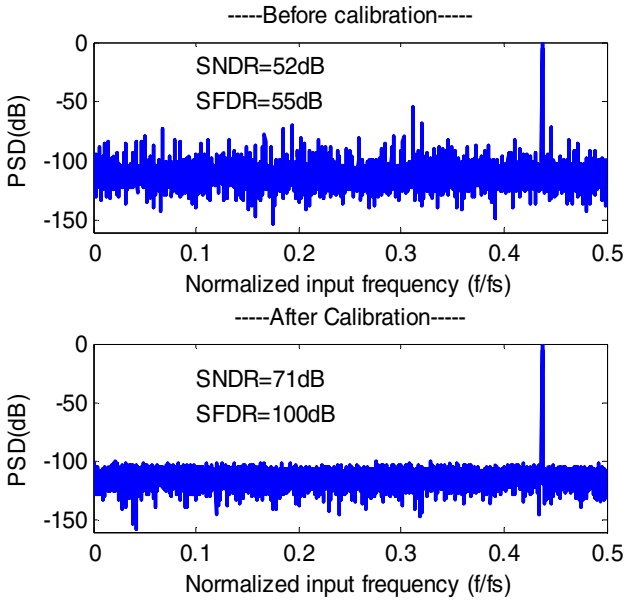

Figure 9. ADC output spectrum before and after calibration.

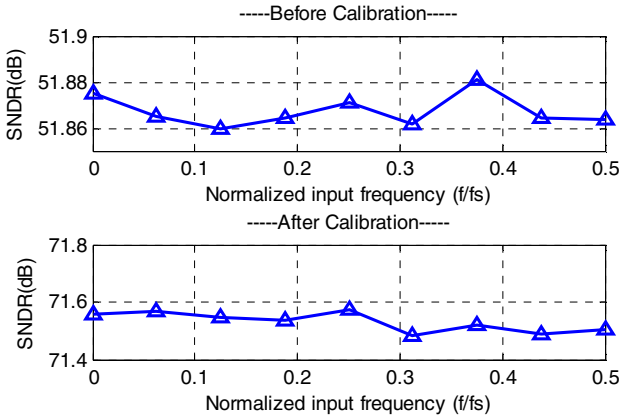

Figure 10. Simulated SNDR vs. the input signal frequency.

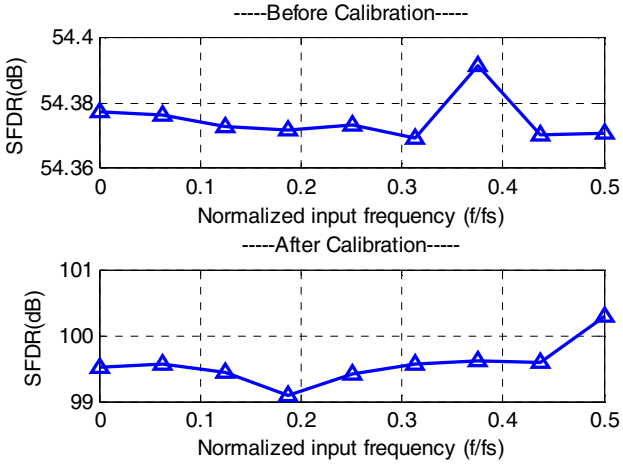

Figure 11. Simulated SFDR vs. the input signal frequency.

VI. CONCLUSION

In this paper a digital background calibration technique was presented to eliminate the linear errors of 1.5bit/stage pipeline ADCs produced by finite DC gain in stage amplifiers. In this technique, the errors were modeled as the analog reference voltage error and by recalculating the digital output with measured reference voltage, the calibrated output is obtained. The stage analog reference voltage was extracted using a created mismatch between stage sub-ADC threshold voltages in the "split ADC" architecture. Efficiency of this method is proved with behavioral simulations using MATLAB and Simulink environments.

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