A Fully Digital Calibration Technique for Nonlinearity Correction in Pipelined ADCs

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***Abstract*— This paper presents a digital background calibration technique for 1.5 bit/stage pipelined analog-to-digital converters. The proposed method corrects for capacitors mismatch, gain error and gain nonlinearities. The new algorithm uses a calibration signal, modified stages and skip-fill method for error calibration while does not require any accurate calibration signal and any added analog circuitry; just a digital finite impulse response filter is needed to implement the polynomial interpolation recovering the skipped samples. The technique is tested on a prototype 12-bit 80-MS/s pipelined ADC which has a capacitors mismatch of 0.1% and 38 dB amplifier DC gain. Simulated in a 90-nm CMOS technology with HSPICE, the ADC achieves 0.25LSB of peak DNL, ±0.25LSB of peak INL, 72dB peak SNDR and 78dB peak SFDR while the core of ADC (without calibration circuitry) consumes only 57.8 mW from a 1V power supply.**

Keywords-Pipelined ADCs; capacitor mismatch; gain error; amplifier nonlinearity; digital background calibration

I. INTRODUCTION

Design of high-speed, high-resolution ADCs is a key issue in high-performance digital communication systems [1]. The pipelined ADCs can produce such speeds but the design of high precision analog elements gets more challenging as the device dimensions and supply voltages are scaled down. The capacitor mismatch, gain error and gain nonlinearities are the major limiting parameters of pipelined ADCs in deep submicron low-voltage technologies [1, 2].

A common way to overcome these precision limitations is applying a calibration technique to the converter. The correlation-based error calibration methods are the digital background techniques introduced recently [3-5]. The time spent for the calibration is an important factor which is much in these methods because the input signal appears as uncorrelated noise with larger amplitude than the calibration signal [3].

This paper describes a digital background calibration technique for pipelined ADCs to fulfill the requirements of high-performance digital communication systems without any high-gain amplifier. The proposed technique uses a calibration signal with reduced number of samples required to converge the process, since the calibration signal is applied when the input signal is skipped. Furthermore, using modified structures for pipelined stages relaxes the accuracy of the calibration signal. The skipped input samples are recovered using an FIR polynomial interpolation filter in digital domain [6].

II. ADC ERRORS MODELING

A pipelined ADC is composed of several low-resolution stages. Commonly, a 1.5-bit/stage architecture is used for high-speed pipelined ADCs [3]. Each 1.5-bit stage is composed of a 1.5-bit sub-ADC and a 1.5-bit multiplying-digital-to-analog converter (MDAC) circuitry. With redundancy and digital correction in a 1.5-bit/stage configuration, the pipelined converters are insensitive to the offset errors in their sub-ADCs and amplifiers, so errors mainly stem from the capacitors mismatch, gain errors and gain nonlinearities of the amplifiers [7]. A single-ended circuit implementation of a 1.5-bit stage with capacitor non-flip-round MDAC is shown in Fig. 1. During sampling phase, Φ_1, the input voltage is sampled on sampling capacitor C_S and the feedback capacitor, C_F, is discharged. Then in the next phase, Φ_2, the capacitor C_F is switched in the amplifier feedback loop, while C_S is switched to $\{-0.5V_{ref}, 0, 0.5V_{ref}\}$ depending on the digital output of the sub-ADC, D. This configuration is chosen instead of the more commonly used capacitor flip-around configuration, because it simplifies the modeling of the MDAC and hence the calibration process [1, 8].

As discussed in [8], the digital equivalent of stages input, D_{in}, with above- mentioned structure can be approximated by a third-order polynomial function as:

$$D_{in} = D + \beta_1 D_{out} + \beta_3 D_{out}^3 \quad (1)$$

where D is equal to {-1, 0, 1} depending on the stage input level and D_{out} is the digital equivalent of stage output. Using this modeling, it is shown that the error sources including capacitors mismatch and gain errors and nonlinearities are defined as stages input-output characteristic [8]. So this model would be the reference point in errors calibration. Knowing β_1 and β_3 in (1), the inverse function of stage can be obtained. Extending this result to all stages of the ADC, its inverse function can be calculated and the input signal is digitized without any dependence to the preciseness of the analog blocks.

The coefficients β_1 and β_3 in (1) are calculated using two different approaches in the previously published literature [9, 10]. In [9], a highly accurate DAC is used to produce an analog input signal to the ADC to measure the coefficients while in [10], definite voltage levels produced by a resistor ladder are digitized using a ΣΔ ADC. Here, an optimal method is

proposed that uses two-mode stages in the calibration mode to extract the stages inverse function without requiring any accurate calibration signal.

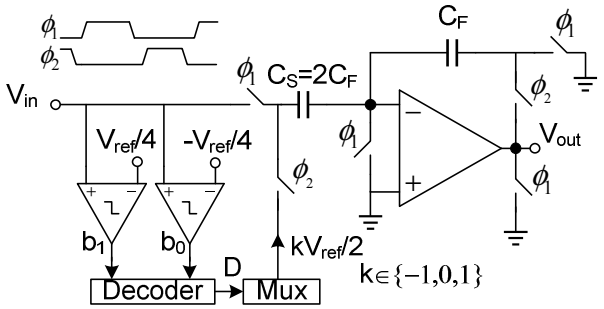

Figure 1. A 1.5-bit stage with capacitor non-flip-around MDAC.

III. Proposed Calibration Technique

The proposed calibration technique measures the coefficients in (1) using a calibration signal. The ADC contains 14 stages with 1.5 bit configuration and a 2-bit flash ADC as the last stage. Linear and nonlinear term coefficients in (1), β_1 and β_3, are measured independently for the first two stages while for the stages 3 to 14 just linear coefficients, β_1, are considered. In the following, the measurement process is described in foreground mode and then the algorithm for background implementation is discussed.

In the foreground mode, it is supposed that the ADC is stopped and it can impose the calibration signal. To calibrate the i^{th} stage, first it is supposed that stage suffers only from the linear error and the backend stages are ideal. In other words, the stage output is perfectly digitized by backend stages, so:

$$D_{in,i} = D_i + \beta_{1i} D_{out,i} \tag{2}$$

where $D_{in,i}$ and $D_{out,i}$ are the digital equivalent of i^{th} stage input and output respectively, D_i is the stage sub-ADC digital output and β_{1i} is its linear term coefficient.

To apply the calibration technique, the i^{th} stage is configured as a two-mode stage. Consider that a constant calibration signal, V_1, with the value of slightly greater than $0.25V_{\text{ref}}$ (comparator threshold voltage) is applied to the stage input. The calibration signal is digitized in two different manners. First, as shown in Fig. 2(a) with stage transfer function, the i^{th} stage is configured as 1.5-bit configuration and then its sub-ADC digital output, D_i=1, and the digitized output for $0.25V_{\text{ref}}$ as the test input signal, $D_{out1,i}$, are stored in a memory. Second, as shown in Fig. 2(b), the stage is configured as a multiply-by-two configuration and the digitized output for V_1, $D_{out2,i}$, is stored in a memory too. With this two stored data and known β_{3i}=0, it is resulted from (2) that

$$V_{in,i} = V_1 \rightarrow \quad D_{in1,i} = D_i + \beta_{1i} D_{out1,i}, \quad D_{in2,i} = \beta_{1i} D_{out2,i} \tag{3}$$

Note that the stage input is the same in the two processes ($D_{in1,i}$=$D_{in2,i}$), so:

$$\beta_{1i}(D_{out2,i} - D_{out1,i}) = D_i \tag{4}$$

Therefore, the coefficient can be extracted from two stored values and the stage sub-ADC digital output in 1.5-bit configuration. In other words, with no need for accurate calibration signal, β_{1i} is extracted. In the i^{th} stage coefficient extraction, it was supposed that the stage output is perfectly digitized with backend stage. The ADC stages are calibrated from 14th stage to first one so when the i^{th} stage is in the calibration process, backend stages will produce a corrected accurate digital output. Extending the applied technique, the nonlinear term coefficient in the stage inverse function can be extracted too. If the full scale input is applied to the amplifier, maximum deviation from ideal input-output function is obtained. With this view, another calibration signal which is equal to $0.5V_{\text{ref}}$ is used too. Since the stage is used in the multiply-by-two configuration, so the maximum input value would be $0.5V_{\text{ref}}$. But, if the amplifier has an offset voltage, the input amplitude would be limited more. So for nonlinear coefficient extraction, the second calibration signal value, V_2, would be slightly less than $0.5V_{\text{ref}}$.

Consequently, to extract both linear and nonlinear term coefficients together, V_1 and V_2 are applied to the stage and the results are stored in the memory to be used by the Least Mean Square (LMS) algorithm [11]. With stored results, it yields from (1):

$$V_{in,i} = V_1, V_2 \rightarrow \begin{cases} D_{in1,i} = D_i + \beta_{1i} D_{out1,i} + \beta_{3i} D_{out1,i}^3 \\ D_{in2,i} = \beta_{1i} D_{out2,i} + \beta_{3i} D_{out2,i}^3 \end{cases} \tag{5}$$
$$\Rightarrow \beta_{1i}(D_{out2,i} - D_{out1,i}) + \beta_{3i}(D_{out2,i}^3 - D_{out1,i}^3) = D_i$$

So, the coefficient can be extracted with the following equation:

$$\begin{aligned} \beta_{1i}(n+1) &= \beta_{1i}(n) + \mu_1 . e(n) . (D_{out2,i} - D_{out1,i}) \\ \beta_{3i}(n+1) &= \beta_{3i}(n) + \mu_3 . e(n) . (D_{out2,i}^3 - D_{out1,i}^3) \end{aligned} \tag{6}$$

where μ_1 and μ_3 are the LMS update step size in the coefficients extraction and $e(n)$ is given by:

$$e(n) = 1 - \beta_{1i}(n)(D_{out2,i} - D_{out1,i}) - \beta_{3i}(n)(D_{out2,i}^3 - D_{out1,i}^3) \tag{7}$$

The background calibration was performed by skip-fill method proposed in [6]. As shown in Fig. 3, for the i^{th} stage

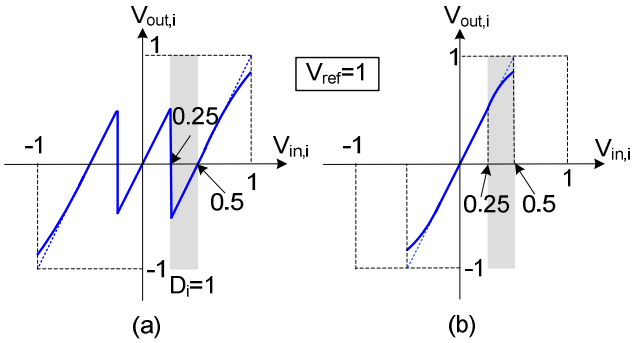

Figure 2. Stage transfer function in calibration (a) 1.5-bit configuration, and (b) multiply-by-two configuration.

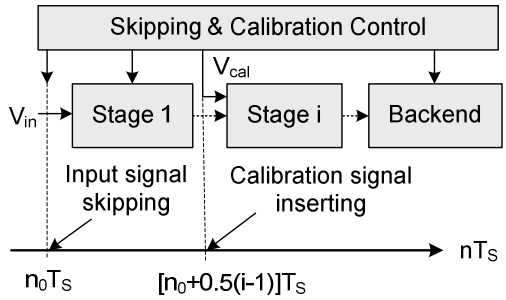

Figure 3. Background implementation of the proposed calibration.

background calibration, the ADC input sample is skipped at n_0T_S and then the calibration signal, V_{cal}, is inserted to this stage in the produced time slut at $[n_0+0.5(i\text{-}1)]T_S$ where T_S and n_0 are the sampling period and time index, respectively. So, in the proposed technique, the calibration is done at the created time sluts without interrupting the ADC normal operation and the skipped samples are recovered with a nonlinear digital interpolator. Here, the accuracy of the predictor that used in the [12] is enough which is a nonlinear polynomial interpolator as mentioned in [6].

IV. ADC Circuits Implementation

To evaluate the performance of the proposed calibration technique, a 12-bit 80MS/s pipelined ADC has been designed in the circuit level with a 90-nm CMOS technology.

In the implemented ADC, the input sample and hold circuit is eliminated with time constant matching of existing paths in the first stage [13]. As shown in Fig. 4 a two-stage Miller compensated amplifier with two cascaded common source amplifiers is used as ADC amplifiers where its dc gain is only 38dB. The charge distribution structure is used as the comparator in the sub-ADCs with dynamic latch [14]. In addition, for the switches needing high linearity, the bootstrapping technique [15] is used. The two-mode stages are simply implemented by a two-mode multiplexer in the stage sub-DAC realization.

V. Simulation Results

The ADC has been simulated in a standard 90-nm CMOS technology with 1V supply voltage. The analog circuits are simulated with HSPICE where the calibration process is implemented in MATLAB. Figure 5 plots the first stage coefficients extraction. If the calibration algorithm worked at the ADC speed, the number of samples for extraction of all stages coefficients is about 14×2^{12} samples. Figure 6 shows the simulated output spectrum before and after the calibration for a 1MHz, 1.2V peak-to-peak differential analog input sampled at 80MHz where the SNDR and SFDR improvements are over 35 dB and 39 dB, respectively. For survey of ADC performance in the Nyquist band, the SNDR and SFDR are calculated for several input signal frequency. The simulation results are shown in Fig. 7. The peak SNDR is equal to 73 dB after calibration for an input frequency of 10 MHz.

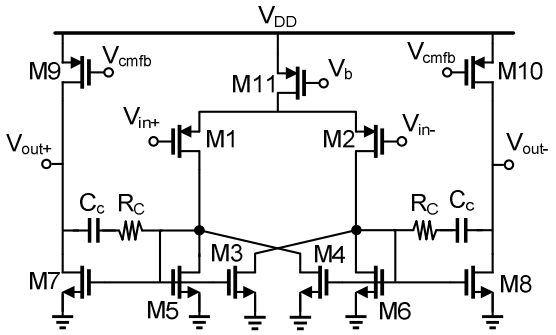

Figure 4. Stages amplifier architecture.

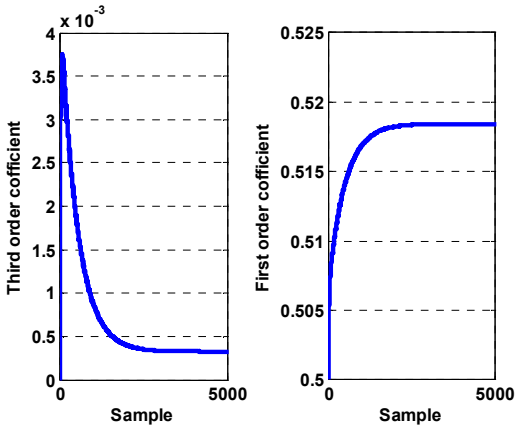

Figure 5. First stage coefficients extraction.

Figure 8 plots the simulated DNL and INL before and after the calibration, respectively, at the sampling frequency of 80MHz. The uncalibrated ADC has a peak INL of 43 LSB. After calibration, the peak INL falls to bellow 0.5 LSB. The analog circuits consume only 57.8 mW from 1V supply voltage. Table I summarizes the resulted performance of the simulated ADC and comparison with recently implemented ADCs.

The interpolator is realized with an FIR filter in MATLAB where uses 80 samples after and 80 samples before skipped sample for interpolation. Because of the filter tap weights are symmetrical and rapidly decreasing toward zero [12]; the interpolator is realized with only 20 first taps weight.

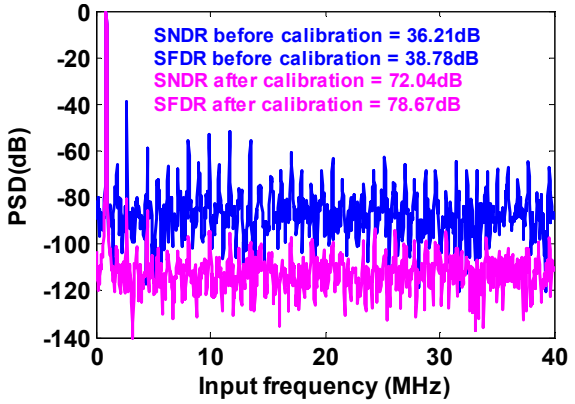

Figure 6. SNDR and SFDR before and after the calibration.

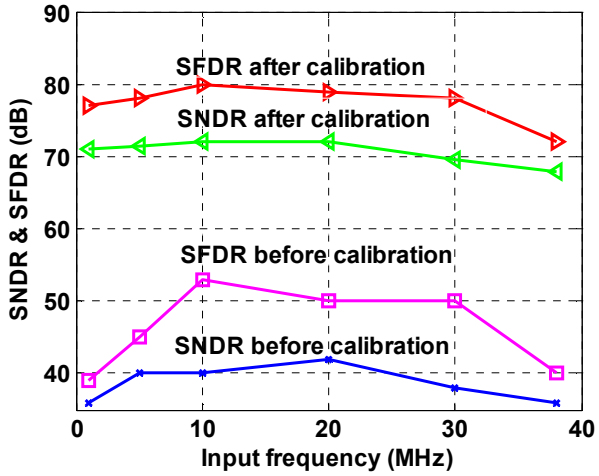

Figure 7. SNDR and SFDR vs. ADC input signal frequency.

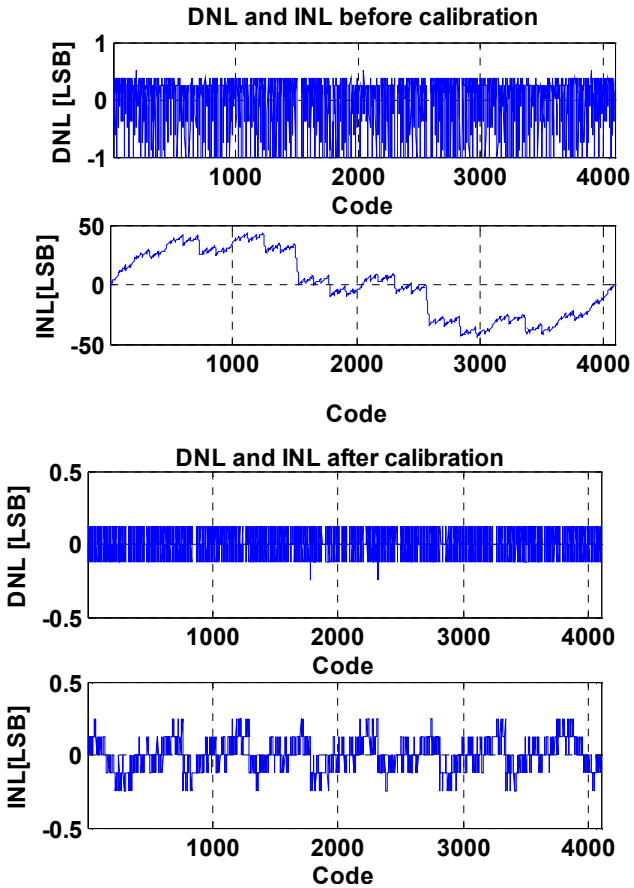

Figure 8. Simulated DNL and INL before and after the calibration.

VI. CONCLUSIONS

This paper describes a digital background calibration technique for 1.5 bit/stage pipelined analog-to-digital converters. The proposed method corrects for capacitors mismatch, gain error and gain nonlinearities by using a calibration signal, modified stages and skip-fill method for error calibration without requiring any accurate calibration signal and extra analog circuits. The proposed calibration technique was tested in a 12bit 80MS/s pipelined ADC.

Table I. Performance comparison of the simulated 12-bit ADC.

Ref.	Process	V_{DD} (V)	f_s (MS/s)	INL (LSB)	DNL (LSB)	SFDR (dB)	SNDR (dB)	Analog power (mW)	FoM (pJ.V/step)
This work	90nm	1	80	±0.25	-0.25	78	72	57.8	0.22
[1]	0.25µm	2.5	80	+0.24	+0.09	84.5	72.6	340	3
[5]	90nm	1.2	100	3.6	0.54	85	69.8	93	0.44
[8]	90nm	1.2	200	+1.3	+0.59	-	64	348	1.6
[9]	90nm	1.2	500	1	0.4	-	52	55	0.4

REFERENCES

[1] Grace et al., "A 12-bit 80-msample/s pipelined ADC with bootstrapped digital calibration," *IEEE J. Solid-State Circuits*, vol. 40,no. 5, pp. 1038–1046, May 2005.

[2] B. Murmann and B. E. Boser, "A 12 b 75 MS/s pipelined ADC using open-loop residue amplification," *IEEE J. Solid-State Circuits*, pp. 2040–2050, Dec. 2003.

[3] J. Li and U. Moon, "Background calibration techniques for multistage pipelined ADC's with digital redundancy," *IEEE Trans. Circuits Syst. II*, vol. 50, no. 9, pp. 531–538, Sep. 2003.

[4] Y.-S. Shu and B.-S. Song, "A 15-bit linear 20-MS/s pipelined ADC digitally calibrated with signal-dependent dithering," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp.342-350, Feb. 2008.

[5] A. Panigada, and I. Galton, "A 130 mW 100 MS/s pipelined ADC with 69 dB SNDR enabled by digital harmonic distortion correction," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3314-3328, Dec. 2009.

[6] U.-K. Moon and B.-S. Song, "Background digital calibration techniques for pipelined ADC's," *IEEE Trans. Circuits Syst. II*, vol. 44, pp. 102–109, Feb. 1997.

[7] S. H. Lewis et al., "A 10-b 20-MSample/s analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 27, no. 3, pp. 351–357, Mar. 1992.

[8] B. D. Sahoo, and B. Razavi, "A 12-bit 200-MHz CMOS ADC ," IEEE J. Solid-State Circuits, vol. 44, pp. 2366–2380, Sep. 2009.

[9] A. Verma, and B. Razavi, "A 10-Bit 500-MS/s 55-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3039–3050, Nov. 2009.

[10] T.-H. Shu et al., "A 13-b 10-MSample/s ADC digitally calibrated with oversampling delta-sigma converter," *IEEE J. Solid-State Circuits*, vol. 30, no. 4, pp. 443–452, Apr. 1995.

[11] S. S. Haykin, Adaptive Filter Theory, 3rd ed. Upper Saddle River, NJ: Prentice-Hall, 1996.

[12] R. G. Massolini et al., "A fully digital fast convergence algorithm for nonlinearity correction in multistage ADC," *IEEE Trans. Circuits Syst. II*, vol. 53, no.5, pp. 389-393, May 2006.

[13] D.Y. Chang, "Design techniques for a pipelined ADC without using a front-end sample-and-hold amplifier," *IEEE Trans. Circuits Syst. I: Reg. papers*, vol. 51, pp. 2123-2132, Apr. 2004.

[14] L. Sumanen et al., "CMOS dynamic comparators for pipeline A/D converters," *ISCAS*, vol. 5, pp. 157-160, 2002.

[15] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio sigma-delta modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE J. Solid Sate Circuits*, vol. 36, pp. 349-355, Mar. 2001.