A Novel Digital Background Calibration Technique for Pipelined ADCs

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***Abstract*—This paper presents a novel and simple digital background calibration technique to eliminate the linear errors of 1.5bit/stage pipelined analog-to-digital converters (ADCs) caused by capacitor mismatch and finite DC gain of stage amplifiers. In this technique, by injecting a determined calibration signal in a modified conventional multiplying digital-to-analog converter (MDAC) and split structure, the errors are measured while it is not necessary to use an accurate calibration signal. As a case study, the technique is tested on a prototype 12bit 1.5bit/stage split pipelined ADC with 60 dB amplifier DC gain and 0.1% capacitor mismatch using MATLAB and Simulink environment simulations. After calibration, the ADC achieves 71 dB SNDR and 82dB SFDR which are restricted to 58dB and 63dB respectively before calibration.**

***Index Terms*—Pipelined ADCs, linear errors, digital background calibration, split ADC.**

I. INTRODUCTION

Analog to digital converters are identified as large mixed-signal circuits that widely used in signal processing circuits and systems. Among various ADC architectures, the pipelined converter is proved to be very efficient for high speed and medium to high resolutions. A pipelined ADC is composed of several low-resolution stages. In each stage, the input is sampled and quantized by the sub-ADC, and then the residue signal is amplified to fit into the next stage's full-scale range using a switched-capacitor (SC) MDAC circuit.

The most limiting parameters of a highly linear pipelined ADC are the capacitor mismatch, finite DC gain in amplifiers and offset voltage in amplifiers and comparators. The offset voltage error is tolerated using a digital redundancy technique while it is necessary to use calibration techniques to reduce the errors produced by capacitor mismatch and finite DC gain as the technologies scale down. There are several approaches to improve the accuracy of MDAC which can be categorized into two groups: analog element calibration and digital one [1]. In the first group, the errors are corrected by adjusting the ADC elements in the analog domain. The analog calibration has two drawbacks. First, any temperature and power fluctuations may degrade its performance. Second, this calibration technique is not an economically optimum solution in spite of digital techniques which use modern mixed-signal technologies advantageous to correct the errors in the digital domain [1]. The digital calibration can be performed in two forms. In foreground techniques, the process is done with stopping the ADC normal conversion while in background techniques, the ADC is always working. In the background methods, the errors are measured by a slow but accurate ADC such as a sigma-delta ADC [2], statistical-based method [3] or the "split ADC" concept [4] and then the parameters are corrected in the digital domain.

In this paper, a digital background calibration technique is proposed for 1.5bit/stage pipelined ADCs by applying a calibration signal to the stage sub-DAC and using the "split ADC" concept. That can eliminate the linear errors in pipelined ADCs which arise from the capacitor mismatch and finite DC gain of the stage amplifiers.

II. LINEAR ERRORS CALIBRATION

A. Linear Errors Modeling in 1.5 bit/Stage Pipelined ADC

An M-bit pipelined ADC with 1.5bit/stage architecture is typically composed of (M-2) 1.5bit stages and a 2bit backend flash ADC. The "capacitor flip-around" MDAC is usually used in high speed 1.5bit/stage pipelined ADCs because of its large feedback factor in the closed-loop configuration which results in fast settling [3]. Fig. 1 shows the SC implementation of 1.5bit/stage pipelined ADC. Here the input signal is sampled by both sampling and feedback capacitors and compared with comparators threshold voltage during the sampling phase. In the next phase, the difference of input signal and sub-DAC output known as the residue signal is amplified. When the amplifiers and capacitors are linear, the transfer function of each stage is given by

$$V_{res} = g\left((1+\frac{C_S}{C_F})V_i - (\frac{C_S}{C_F})kV_{ref}\right), \quad g = \frac{1}{1+\frac{1}{A}(1+\frac{C_S}{C_F})} \qquad (1)$$

where C_S and C_F are the sampling and feedback capacitors, respectively, A is the amplifier DC gain and k is the stage digital output with values equal to {-1,0,1}, depending on the stage input voltage level [5]. Assuming an ideal ADC, with no capacitor mismatch and infinite DC gain of amplifiers, the analog output of each stage is simplified as

$$V_{res} = 2V_i - kV_{ref}, \qquad (2)$$

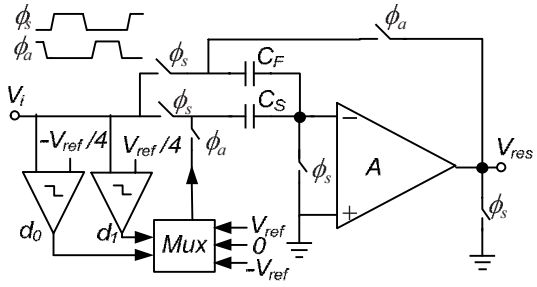

Fig. 1. A 1.5 bit stage with "capacitor flip-around" MDAC

But actually, the ADC output will be deviated from the ideal one because of the capacitor mismatch and finite DC gain of the amplifiers. As discussed in [6], the errors produced by these circuit nonidealities can be corrected with measuring the voltage gaps in the input-output transfer curve of stages.

B. Digital Background Calibration

The stage output voltage, V_{res}, is digitized by the later ADC stages named as backend ADC. As given by (3), the digital equivalent of the stage input voltage, D_{in}, is calculated by adding the digital reference, $D[V_{ref}]$, to the digitized residue, $D[V_{res}]$, and then divided by 2.

$$D_{in} = (D[V_{res}] + k.D[V_{ref}])/2, \quad (3)$$

With this view, what is subtracted in the MDAC can be restored digitally. However, the analog reference voltage subtracted in (2) is affected by capacitor mismatch and finite DC gain of amplifier, and therefore, it does not match with the ideal digital reference.

The mismatch between the analog reference, V_{ref}, and the digitized reference, $D[V_{ref}]$, can be eliminated by adjusting the digital reference [6]. Although after this calibration, the overall gain slope error remains, but the gain slope correction is not necessary in many applications, since the linearity of ADC transfer function is enough [6].

Therefore, with ideal backend ADC, the calibrated digital output is

$$D_{in} = (D[V_{res}] + k.D[RCF.V_{ref}])/2, \quad (4)$$

where RCF is the reference correction factor. In this paper a simple concept known as "Split ADC" and a determined calibration signal is used to measure this correction factor. In split architecture the ADC is composed of two channels, each converting the same input signal and producing individual output codes then the average of the two outputs is reported as the ADC output code. The background calibration signal is developed from the difference between these codes. If both ADCs are correctly calibrated, the two outputs will agree, and the difference will be zero. Since the final ADC output is generated by the sum of the two ADC outputs, each ADC used in this architecture can be designed with half of the capacitance values to meet thermal noise requirements, thus each ADC has approximately half of the power consumption and area of a single ADC designed for the same resolution [4].

III. Proposed Calibration Technique

A. Stage Reference Voltage Correction Factor Measurment

In the proposed method, the stage reference error is measured by applying a constant calibration signal to the sub-DAC in the "split ADC" structure. As shown in Fig. 2, the calibration signal, V_{cal}, is inserted to the sub-DAC of first stage in channel A. In fact this signal is used to create mismatch between both channels [4]. The effect of adding this calibration signal to the stage sub-DAC input can be seen in the transfer curve. In 1.5bit/stage architecture used here, we divide the region given up for the offset compensation in sub-ADC into two parts, a part of it for offset compensation and the rest for calibration signal adding, thus V_{cal} is chosen equal to $V_{ref}/8$. As shown in Fig.3, by applying the calibration signal into the first stage of channel A, the transfer curve changes to dashed lines. In fact, in this technique the reference voltages of stage's sub-DAC are modulated by the calibration signal value. Assuming reference errors in first stage, all of the next stages are lumped into a backend as an ideal independent ADC to digitize the stage analog output. If channels in split structure are equal and the analog outputs of the first stage are perfectly digitized by the backend ADC, the difference of digital output of backend ADCs ($D[V_{resa}]$ and $D[V_{resb}]$) is proportional to reference errors of first stage in channel A.

$$D[V_{resb}] - D[V_{resa}] = RCF_{1a}.V_{cal} \quad (5)$$

$$RCF_{1a} = g.(\frac{C_S}{C_F}) \quad (6)$$

where RCF_{1a} is the first stage reference correction factor. As shown in (5), when V_{cal} is added to the stage sub-DAC input, its analog output value is proportional to V_{cal}.

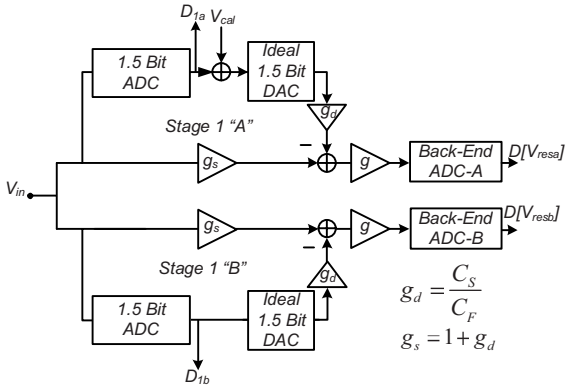

Fig. 2. Proposed method for stage reference voltage extraction.

Therefore, assuming ideal backend ADC and equal channels in split ADC structure, we can measure the reference error in first stage of channel *A* that is proportional to capacitor mismatch and finite DC gain of amplifier. The same work is repeated for first stage of channel *B*. In other words, the calibration signal is applied to sub-DAC in first stage of channel B, and the reference errors in this stage is measured using the difference of digital outputs of backend ADCs. But, this measurement method has several drawbacks. The accuracy of measurement depends on the accuracy of V_{cal}, as shown in (5). Furthermore, we assumed the two channels are equal for split structure while in a real ADC these channels are not same. Finally, the accuracy of this measurement method is limited by the backend ADC errors. So, other techniques are proposed to complete the calibration procedure.

B. Accuracy of Calibration signal

Here, a constant voltage with value of $V_{ref}/8$ is used as calibration signal. Since, it is difficult to build a calibration signal with a very accurate known magnitude in the analog domain [3] so the accuracy of measurment results depend on the accuracy of calibration signal. For this resaon, we use another method to measure the reference erorr independent of the accuracy of calibration signal as used in [5].

Using a modified version of MDAC helps us in this method. As shown in Fig. 4, here two constant signals are used as calibration signal. During the sampling phase, the first calibration signal, V_1, is sampled on feedback capacitor and an extra capacitor, C_E, with sampling capacitor are sampling the input voltage (C_E is equal to C_E and C_S and is emitted when calibration is done). In amplifying phase, the second calibration signal, V_2, is inserted with C_S in MDAC and C_F is rounded in feedback mode and C_E is switched to the DAC voltage. By these two constant voltages, the stage reference voltage is extracted without any dependence on their accuracy. This measurement is done in several steps. At the first time, V_1 is set to $7V_{ref}/8$ and V_2 is equal to V_{ref} so the term g_{r1} is measured. In the second time, V_1 is set to $7V_{ref}/8$ and V_2 is equal to $6V_{ref}/8$ which gives g_{r2}. At the *7th* measurement V_1 is set to $V_{ref}/8$ and V_2 is $2V_{ref}/8$ and g_{r7} is gained. Finally, V_1 and V_2 are set to $V_{ref}/8$ and ground respectively and g_{r8} is obtained. With this procedure, inserted calibration signal in every step is equal to $V_{ref}/8$. Using the following equations the reference error of first stage in channel *A* is gained.

$$g_{ri} = gV_{ref} \times \begin{cases} (\frac{8-i}{8}) - (\frac{9-i}{8})(\frac{C_S}{C_F}), & i = \{1,3,5,7\} \\ (\frac{9-i}{8}) - (\frac{8-i}{8})(\frac{C_S}{C_F}), & i = \{2,4,6,8\} \end{cases}, \qquad (7)$$

Therefore,

$$RCF_{1a}.V_{ref} = \sum_{i=1}^{8} (-1)^i .g_{ir} \qquad (8)$$

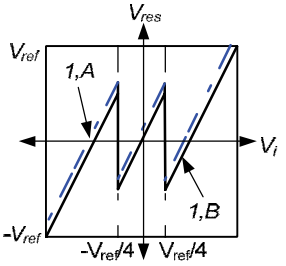

Fig. 3. Transfer curve of the first stages of split ADC in calibration .

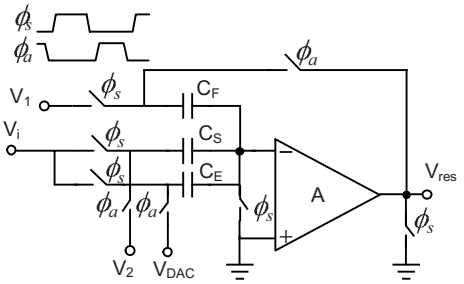

Fig. 4. Modified MDAC for RCF measurment.

A same procedure is repeated for the first stage of next channel. Therefore, it is not necessary to use accurate calibration signals in this technique because these are eliminated from (8) so it is enough to use a resistor string to generate the voltages V_1 and V_2.

C. Channel Mismatch Measurment

We assumed that two channels are equal, also channel mismatch is an important limiting factor, so before the reference error is measured, we must make the two channels equal as much as possible. For this purpose, we use the channel mismatch eliminating concept in time interleaved pipeline ADCs [1]. Before inserting any calibration signal to ADC, a sign-sign version of Least-Mean-Square (*LMS*) algorithm is utilized to extract the channel mismatch factor [8].

$$ch_{mis}(i) = ch_{mis}(i-1) - \mu sign(\varepsilon) sign(D_a) \qquad (9)$$

where ch_{mis} is channel mismatch while D_a and D_b are digital output of channel *A* and *B* ADCs respectively, $\varepsilon = (D_b - D_a)$ is the error signal, and μ is the update step-size in *LMS* algorithm. This factor is used in reference error measurement as correction factor of two channels.

D. Comparision with Convetional Methods

In this technique, a calibration signal is applied to the sub-DAC instead of sub-ADC in [3], therefore it reduce the input signal range. Also the calibration signal used here is a deterministic signal which decreases the power dissipation in digital units by eliminating the extra circuitry needed for random signal generation [5] and it is not necessary to use a calibration signal with accurate known magnitude in the

analog domain as used in [6]. Although, the accuracy of reference error measurement is restricted by the backend stages here but it can be improved by using additional stages in the backed ADC. Further more, in this method the similar stages of two channels have independent errors while in [7] it is supposed that the gain errors of the first stages in two channels are equal. The most important advantage of this method is low calibration time which is resulted from split structure and determined calibration signal.

IV. Simulation Results

The proposed technique was simulated behaviorally using MATLAB and Simulink environment. In these simulations, a 12 bit 1.5bit/stage 2-channel split ADC was used and the technique was applied on the first two stages, while using 10 bit ideal ADC as a backend. The calibration is started form 2nd stages in channel *A* and *B* and then moved to the first stages. Stage MDACs have maximum 60 dB DC gain for amplifiers and 0.1% capacitor mismatch. Here, 16384 input samples are used for *LMS* algorithm in channel mismatch extraction which its step-size was 2^{-16}. For each stage reference measurement, mentioned eight steps is repeated 100 times and the results is averaged. After calibration, the ADC With $0.8V_{ref}$ input amplitude, achieves 71 dB SNDR and 82dB SFDR which are restricted to 58dB and 63dB respectively before calibration. Fig. 5 shows the output spectrum of this 2-channel split ADC before and after calibration, Fig. 6 illustrates the simulated SNDR versus the input signal frequency with and without calibration and Fig. 7 illustrates the simulated SFDR versus the input signal frequency with and without the calibration.

V. Conclusions

In this paper a digital background calibration technique was presented to eliminate the linear errors of 1.5bit/stage pipeline ADCs produced by the capacitor mismatch and finite DC gain in stages amplifiers. The errors were modeled as the reference voltage error and by measuring the digital equivalent of stage reference voltage with determined calibration signal in the modified MDAC and the "split ADC" concept, the calibrated output is obtained.

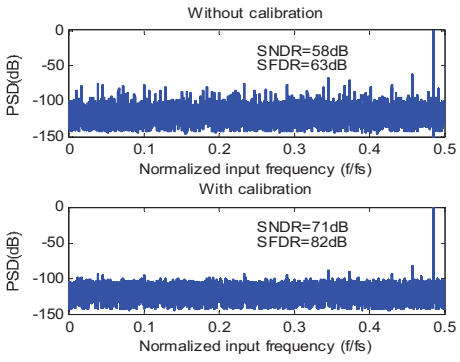

Fig. 5. ADC output spectrum without and with calibration.

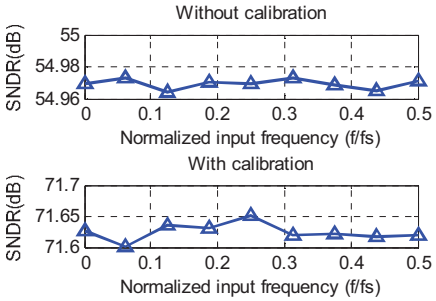

Fig. 6. Simulated SNDR vs. the input signal frequency without and with calibration

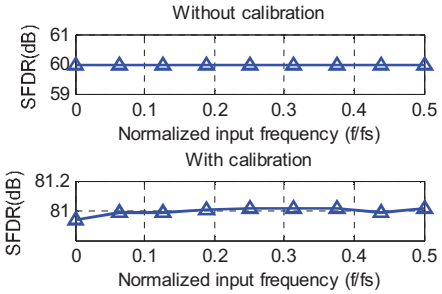

Fig. 7. Simulated SFDR vs. the input signal frequency without and with calibration.

References

[1] F. Maloberti, "*Data converters*," Springer-Verlag, pp 362-364, 2007.

[2] T. Shu, B. Song, and K. Bacrania, "A 13-b 10-Msample/s ADC digitally calibrated with oversampling delta-sigma converter," *IEEE J. Solid-State Circuits*, vol. 30, pp. 443-452, April 1995.

[3] D. Y. Chang, J. Li, and U.-K. Moon, "Radix-based digital calibration techniques for multi-stage recycling pipelined ADCs," *IEEE Trans. Circuits Syst., I*, vol. 51, no. 11, pp. 531-538, Nov. 2004.

[4] J. McNeill, M. C. W. Coln, and B. J. Larivee, "Split ADC architecture for deterministic digital background calibration of a 16-bit 1-MS/s ADC," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2437-2445 Dec. 2005.

[5] K. El-sankary and M. Sawan, "A background calibration technique for multibit/stage pipelined and time-interleaved ADCs" *IEEE TCAS II*, vol. 53, no. 6, pp. 448-452, June 2006.

[6] Yun-Shiang Shu, and Bang-Sup Song, "A 15-bit Linear 20-MS/s Pipelined ADC Digitally Calibrated With Signal-Dependent Dithering," *IEEE J. Solid-State Circuits,* vol. 43, no. 2, pp.342-350, Feb 2008.

[7] M. Taherzadeh-Sani and A. Hamoui, "Digital background calibration of a 0.4-pJ/step 10-bit pipelined ADC without PN generator in 90-nm digital CMOS," *IEEE Asian Solid-State Circuits Conference*, pp. 53-56, Nov. 2008.

[8] S. S. Haykin, *Adaptive Filter Theory*, 3rd ed. Upper Saddle River, NJ: Prentice-Hall, 1996.