A Fast Settling On-Chip Low-Dropout Regulator with a Robust Frequency Compensation Scheme

Mortaza Mojarad and Mohammad Yavari
Integrated Circuits Design Laboratory, Department of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran
E-mails: mmojarad@aut.ac.ir, myavari@aut.ac.ir

Abstract: *An on-chip low-dropout (LDO) voltage regulator with a novel technique to improve the settling time and a robust frequency compensation scheme is presented in this paper. The total capacitance required for the utilized compensation topology is only 2.8 pF. The proposed LDO regulator was implemented in a standard 0.35 µm CMOS technology and the simulation results show that the implemented LDO regulator operates from a supply voltage of 2 V to 4 V with a dropout voltage of 200 mV and the maximum load current of 120 mA, consuming 45 µA quiescent (ground) current.*

Keywords: Low-dropout regulators, voltage regulators, on-chip regulators, fast settling, frequency compensation.

1. INTRODUCTION

An on-chip power management system may contain several output-capacitorless linear regulators. For handheld battery operated devices, the regulators are expected to have lower power consumption in order to increase the battery life and operating time. Today, low quiescent current, low-dropout (LDO) regulators are spectacularly popular and are widely used for their power efficient nature [1].

For conventional regulators, a large off-chip capacitor ranging from 1 µF to 10 µF is used at the output node to improve both the stability and transient response which leads to smaller settling (recovery) time and reduced under/overshoots [2]. Obviously, this amount of capacitance cannot be integrated on a single chip. Therefore, an on-chip regulator suffers from inherent deteriorated stability and transient response. In order to boost the overall performance of on-chip regulators, especially in terms of stability and settling time, new frequency compensation schemes and transient response enhancement techniques are required to be developed.

Since the settling time and the value of under/overshoot of the regulated output voltage affects the performance of the system supplied by the LDO, transient response is one of the most important and critical specifications for LDO regulators. The transient response of an LDO is mostly dependent upon three parameters; closed loop stability, gain-bandwidth product, and slewing performance at the gate of the large output power transistor, among which the latter dominates the overall settling time. This is due to the high aspect ratio of the power transistor which results in large parasitic capacitances at the gate of the power MOSFET.

Recently, various topologies have been proposed to compensate frequency and transient responses of on-chip LDO regulators. Most of which consider an LDO regulator as a two or three stage amplifier and use Nested Miller Compensation (NMC) based pole splitting approaches to guarantee its stability [1]–[4]. Also, different slew rate enhancement techniques and circuitries have been designed to boost the slew rate and thus improve the transient response, as well. For a three stage LDO regulator which consists of a two stage error amplifier and a power MOSFET, the slewing at the gate of the power MOSFET has an asymmetric behavior. To investigate this, a conventional three stage on-chip LDO regulator is shown in Fig. 1, where $M_{1\text{-}4}$ form the second stage of the error amplifier, M_P represents the power MOSFET and R_{F1} and R_{F2} are the sampling feedback resistors. V_{REF} is provided by a reference circuit and I_{Load} is the load current. It should be noted that the frequency compensation loop is left out. When large amounts of load current decrease (increase) in a short time, the output voltage and the sampled voltage, V_{FB}, rise (fall) suddenly, the first stage enters the non-linear (slewing) region, and V_1 reaches V_{DD} (ground). Therefore, in the first case when V_1, which is the gate-source voltage of M_1, nears V_{DD}, a large amount of current is injected to the gate of the power MOSFET through $M_{1\text{-}3}$, charging the large parasitic capacitor at this node, resulting in a reasonable slew rate and settling time. On the contrary, by falling V_1 to ground, transistors $M_{1\text{-}3}$ enter the cut-off region and drain current through M_4 which is limited by its gate bias voltage, discharges the gate parasitic capacitor at a slower rate. In this case, the slew rate is very small and thus the settling time is dramatically increased.

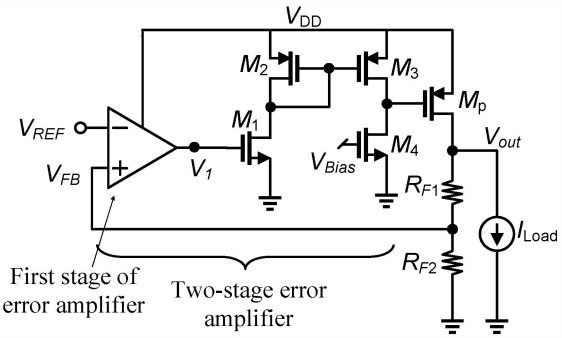

Fig. 1. Basic three stage LDO regulator.

This paper focuses on improving the transient response by using an appropriate frequency compensation scheme to achieve higher gain-bandwidth product and sufficient stability, and providing a push-pull stage at the gate of power MOSFET to get a symmetrical slewing and hence improved settling behavior.

2. CIRCUIT IMPLEMENTATION

Herein, a systematic approach for frequency compensation task and a novel method to improve the slew rate and the transient response are discussed.

2.1 The ac Response of the Proposed LDO

Figure 2 shows the small-signal model of the proposed on-chip regulator with DAFSMC (Dual Active Feedback with Single Miller Capacitor) compensation strategy. This topology was proposed in [5] to compensate three stage amplifiers and led to tangible results and proven feasibility. Here, it has been shown that this topology can be used to compensate the frequency response of three stage LDO regulators, as well. It is instructive to note that due to large parasitic capacitors of the power MOSFET and variable load current, most of the compensation schemes, proposed for three stage amplifiers, do not lead to acceptable results in three stage LDO regulators. In order to investigate the practicality of DAFSMC strategy for three stage on-chip LDO regulators, the open-loop transfer function has been obtained by small-signal analysis of Fig .2.

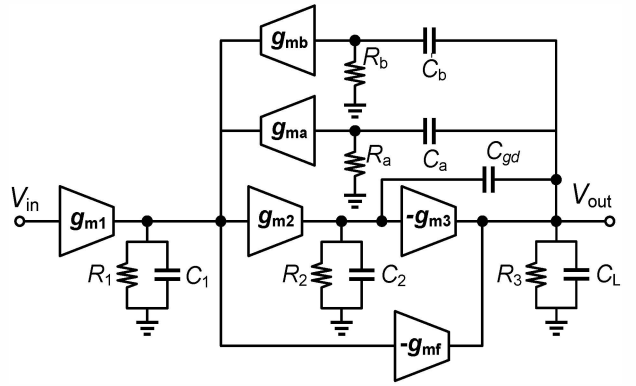

Fig. 2. Small-signal model of the LDO for ac response.

The power MOSFET is modeled as an amplifier stage by defining g_{m3} and R_3 as its transconductance and output resistance, respectively. C_L models the on-chip load capacitance, g_{m1} and g_{m2}, are transconductances, R_1 and R_2 are output resistances, and C_1 and C_2, are output parasitic capacitances of the first and second stages, respectively. Similarly, g_{ma} and g_{mb} represent transconductances, R_a and R_b are input resistances of the feedback current buffers where C_a and C_b model the Miller capacitances. These two feedback paths are chosen to be equal which yields

$$C_a = C_b\ ,\ R_a = R_b = \frac{1}{g_{ma}} = \frac{1}{g_{mb}}\ . \tag{1}$$

Neglecting high frequency poles and zeros, the open-loop transfer function can be described by:

$$A_v(s) = A_{dc}\frac{(1+\frac{s}{\omega_z})^2}{(1+\frac{s}{\omega_{p,dom}})(1+\frac{2\xi}{\omega_n}s+\frac{1}{\omega_n^{\,2}}s^2)(1+\frac{s}{\omega_{p,nd}})} \tag{2}$$

where $A_{dc}(=-g_{m1}g_{m2}g_{m3}R_1R_2R_3)$ is the dc gain of the LDO. Since an LDO regulator is expected to sustain its stability for full load current range, the transfer function is obtained individually for both light load (e.g. I_{Load} = 0 mA) and heavy load (e.g. I_{Load} = 100 mA) conditions. Moreover, the gate-drain parasitic capacitance of large power MOSFET cannot be neglected. The dominant pole, $\omega_{p,dom}$, and the gain-bandwidth product, ω_{GBW} remain almost constant under any loading conditions and are estimated by:

$$\omega_{P,dom} = \frac{1}{2g_{m2}g_{m3}R_1R_2R_3C_a}\quad ,\quad \omega_{GBW} = \frac{g_{m1}}{2C_a}\ . \tag{3}$$

In order to estimate the pole-zero locations in the light load condition, the following assumptions have been made:

$$C_L >> C_2,\ C_a\ ,\ C_{gd} >> C_1 \tag{4}$$

$$\frac{g_{mf}}{g_{m2}},\ g_{m1}R_1,\ g_{m2}R_2,\ g_{m3}R_3 >> 1\ . \tag{5}$$

Based on the above, the poles, zeros and the corresponding natural frequency, ω_n and the damping factor, ξ are given by:

$$\omega_z = \frac{1}{C_aR_a}\ ,\ \omega_{p,nd} = \frac{1}{C_aR_a}\ ,\ \omega_n = \sqrt{\frac{g_{mf}g_{ma}}{C_1C_L}}\ ,$$

$$\xi = \frac{C_1C_L + 2C_a^{\,2}g_{mf}R_a}{4C_ag_{mf}}\sqrt{\frac{g_{mf}g_{ma}}{C_1C_L}}\ . \tag{6}$$

For the heavy load condition, two extra assumptions have to be set up in addition to (4) and (5), described by:

$$g_{m3} >> g_{m1}, g_{m2}, g_{ma}, g_{mf} \tag{7}$$

$$R_3 << R_1, R_2, R_a\ . \tag{8}$$

Based on (4), (5), (7), and (8), the frequencies of the real poles and zeros and also the natural frequency and damping factor of the non-dominant complex poles are obtained, as follows:

$$\omega_z = \frac{1}{C_aR_a}\ ,\ \omega_{p,nd} = \frac{2(C_2+C_{gd})+g_{m3}R_3C_{gd}}{C_aR_a(g_{m3}R_3C_{gd}+C_2)}\ ,$$

$$\omega_n = \sqrt{\frac{g_{m2}g_{ma}}{C_1C_{gd}}}$$

$$\xi = \frac{C_1g_{m3}R_3C_{gd} + 2C_a^{\,2}g_{m2}g_{m3}R_3R_a}{4g_{m2}g_{m3}R_3C_a}\sqrt{\frac{g_{m2}g_{ma}}{C_1C_{gd}}}\ . \tag{9}$$

The idea of frequency compensation is to create a single pole property under the unity gain frequency which can be roughly estimated by the gain-bandwidth product described in (3). To achieve this, non-dominant poles and zeros have to be located beyond the gain-bandwidth product. By considering (6) and (9), placing the zeros over the unity gain frequency, results in the first design constraint, as follows:

$$g_{m1} < 2g_{ma}\ . \tag{10}$$

For complex poles, the natural frequency, ω_n, has to be at least twice the gain-bandwidth product to get a sufficient phase margin, and the damping factor is set to $1/\sqrt{2}$ for an eligible transient response. Lower values of damping factor cause the quality factor to increase which may lead to instability due to the magnitude peaking near the unity gain frequency [4]. Therefore, by setting the damping factor in (6) equal to $1/\sqrt{2}$, another compensation condition can be established, given by:

$$\frac{C_1C_L + 2C_a^{\,2}g_{mf}R_a}{4C_ag_{mf}}\sqrt{\frac{g_{mf}g_{ma}}{C_1C_L}} = \frac{1}{\sqrt{2}}\ . \tag{11}$$

Based on (11), the capacitance, C_a, is obtained and given by:

$$C_a = \frac{1}{2}\sqrt{\frac{2g_{ma}C_1C_L}{g_{mf}}}\ . \tag{12}$$

Similarly, by setting the damping factor in (9) equal to $1/\sqrt{2}$, the capacitance, C_a, can be derived, as given by:

$$C_a = \frac{1}{2}\sqrt{\frac{2g_{ma}C_1C_{gd}}{g_{m2}}}. \quad (13)$$

From (12) and (13), the larger C_a has to be chosen to ensure stability for the worst case stability condition. Giving the minimum value of twice the gain-bandwidth product to obtain natural frequencies in (6) and (9), yields two other design constraints as follows:

$$g_{mf} > \frac{g_{m1}^2 C_1 C_L}{C_a^2 g_{ma}}, \quad g_{ma} > \frac{g_{m1}^2 C_1 C_{gd}}{g_{m2} C_a^2}. \quad (14)$$

2.2 Transient Response Enhancement

As mentioned, the slewing performance of the LDO circuit at the gate of the power transistor is the most significant and determinative parameter in forming the transient response. The circuit shown in Fig. 1 suffers from an asymmetric slew rate which causes large undershoots and prolonged settling time for ascending edge of the load current pulse. In this paper the error amplifier has been designed in a way to constitute a push-pull stage at the gate of the power MOSFET, creating a symmetric slewing behavior. This was achieved by using a fully differential amplifier as the first stage amplifier and splitting the second stage into two equal parallel feedforward paths. The concept of this method is illustrated in Fig. 3, where A_{V1}, A_{V2}, and A_{V3} represent the voltage gains of the first, second, and third stages, respectively. The compensation loop consisting of two parallel current buffers have to be split into four feedback current buffers, two of which are connected to the inverting node of the first differential stage with a polarity opposite to the other two buffers connected to the non-inverting node. For the feedforward path, g_{mf}, the same process is applied. It is evident that the proposed technique is of high practicality and the aim to create a push-pull second stage is fulfilled.

2.3 Circuit Description

The circuit realization of the proposed on-chip LDO regulator is shown in Fig. 4. It employs a three stage configuration to increase the dc gain resulting in better load and line regulations. The first stage is a fully differential folded cascode amplifier which consists of transistors M_1 to M_{11}. The transconductance of the first stage is determined by transistors M_2 and M_3. Transistors M_{12} to M_{15} form the second stage. The transconductance of this stage is determined by M_{12} and M_{15}. It is apparent that $M_{12\text{-}14}$ and M_{15}, are the two parallel paths of the second stage. M_{16} establish the negative feedforward stage. The positive feedforward is realized by M_{17} which is preceded by a voltage inverter formed by M_{24} and M_{25}. A large power MOSFET constitutes the third stage. The shunt feedback is provided by a resistive network including R_{F1} and R_{F2}. C_{a1}, C_{b1}, C_{a2}, and C_{b2} are the Miller compensation capacitors. Transistors M_7 and M_9 form the positive current buffers. Similarly, transistors $M_{18\text{-}23}$, M_6, and M_8, realize the negative current buffers. Transistors $M_{18\text{-}21}$ are used to reduce the dc level of output voltage and M_{22} and M_{23} invert the signal at the output node. Since the first stage is a fully

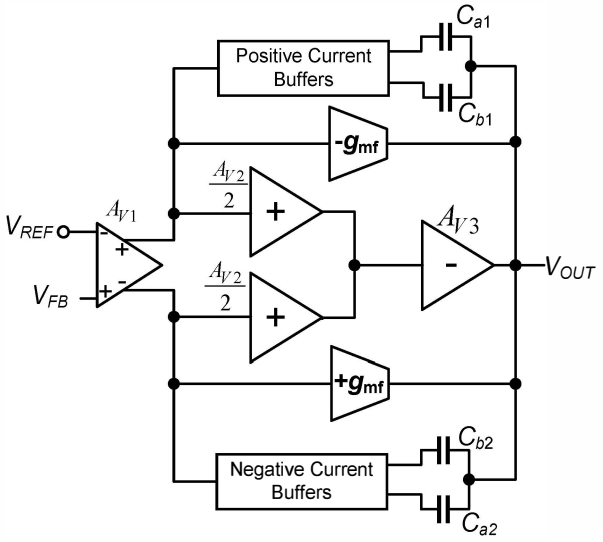

Fig. 3. Block diagram of the proposed LDO.

differential stage, a common mode feedback circuit [6], shown in Fig. 5, has been applied to set the output nodes of the first stage at a fixed dc level.

3. Simulation Results

The presented on-chip LDO regulator is implemented and simulated in a standard 0.35-µm CMOS technology using HSPICE. The LDO specifications are shown in Table I and the results are compared with existing works in Table II. It is clear that comparing the simulation results with experimental measurements is not fair. However, the proposed LDO improves the performance and especially the transient response considerably. The frequency and transient responses are shown in Figs. 6 and 7, respectively. It can be seen that the transient response is almost symmetric and the settling time and the amount of under/overshoots have been reduced.

TABLE I. Proposed LDO Performance Summary.

Supply Voltage	**2 V – 4 V**
Output Voltage	**1.8 V**
Recovery Time **0 mA→120 mA** **120 mA→0 mA**	 **0.7 µs** **0.6 µs**
Minimum Phase Margin	**60 degree**
Loop Gain	**79 - 97 dB**
PSR @ I_{Load}=10 mA	**66 dB @ 1 kHz**

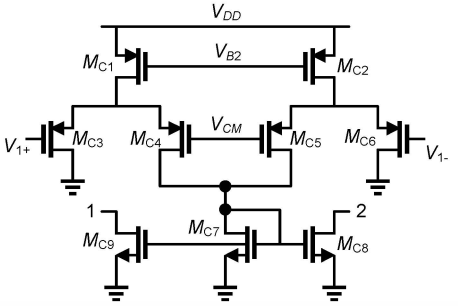

Fig. 5. Common mode feedback circuit.

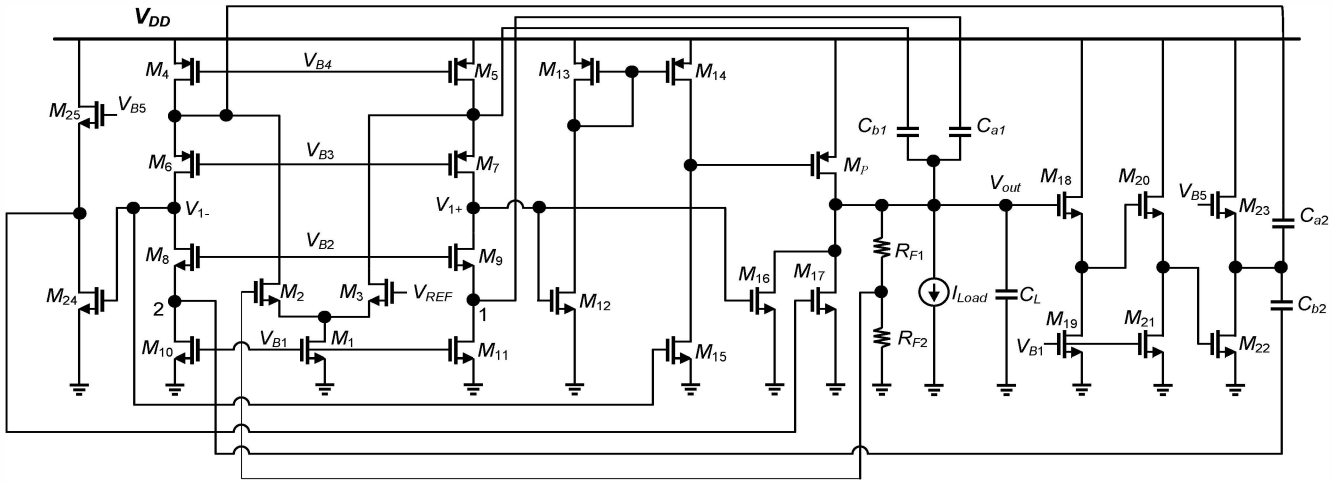

Fig. 4. Circuit realization of the proposed LDO.

TABLE II. COMPARISON OF RESULTS.

	[1] 2007	[2] 2010	[3] 2003	[4] 2007	[7]* 2009	[8] 2010	This work*
Technology (µm)	0.35	0.35	0.6	0.35	0.13	0.5	0.35
$I_{Load,MAX}$ (mA)	50	100	100	100	50	100	120
V_{DROP} (mV)	200	200	200	200	100	200	200
I_Q (mA)	0.065	0.02	0.038	0.1	0.2	0.045	0.045
Recovery Time (µs)	~15	<9	2	30	<0.6	N.A.	<0.7
$C_{on\text{-}chip}$ (pF)	21	7	12	6	<16	65.2	2.8
FOM** (ns)	19.5	1.8	0.76	30	2.4	N.A.	0.26

*Simulation Results.

**FOM=T_R (Recovery time). I_Q / $I_{Load,MAX}$. (The smaller FOM means the better performance)

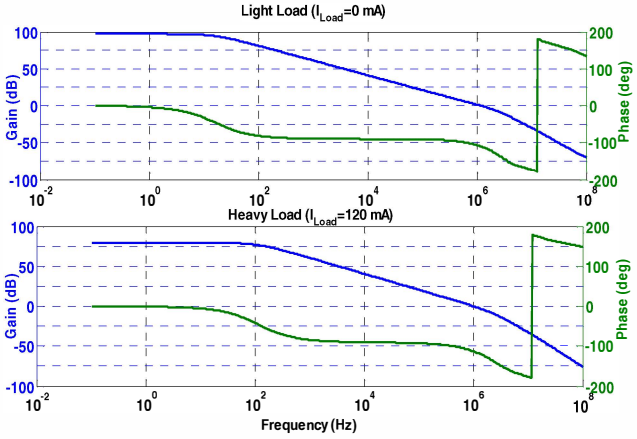

Fig. 6. Frequency Response of the proposed LDO.

4. CONCLUSION

A three stage on-chip LDO regulator with a novel technique to boost the transient performance was proposed. In addition, DAFSMC frequency compensation scheme has been applied to the three stage LDO to improve the gain-bandwidth product and guarantee the stability while reducing the total on-chip compensation capacitance. The simulation results prove high feasibility of the proposed LDO.

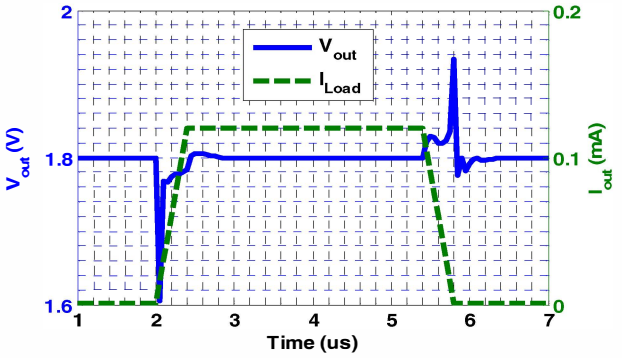

Fig. 7. Simulated transient response with C_L=100 pF @ V_{DD}=2 V for load current pulse from 1 mA to 120 mA with 0.4 µs rise and fall times.

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