A Novel Frequency Compensation Scheme for On-Chip Low-Dropout Voltage Regulators

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***Abstract*—A new frequency compensation scheme for linear low-dropout (LDO) voltage regulators with on-chip applications is presented in this paper. The proposed compensation technique uses a single capacitor of only 70 fF, making it suitable for system-on-chip (SoC) applications. The presented low-dropout regulator operates from a supply voltage of 1.8 V to 3 V with dropout voltage of 200 mV. The maximum output current of this LDO regulator is 100 mA with a quiescent current of 25 µA and it is simulated in a 0.35 µm CMOS technology.**

I. INTRODUCTION

For complex and highly integrated systems, providing a stable, clean and accurate power supply with low dependency to load variations is an inevitable task [1]. Due to increasing trend to system-on-chip (SoC) design solutions, there is a fast-paced development of on-chip voltage regulators. Conventional regulators use an off-chip filtering capacitor ranging from 1 to 10 µF, both to improve the transient response and to guarantee the stability [2]. Clearly, this amount of capacitance cannot be integrated on a single chip. Therefore, new compensation schemes and transient response enhancement techniques have to be developed to allow greater integration capability without degrading the overall performance of the regulator.

For a linear voltage regulator, the dropout voltage refers to the minimum difference between the input supply voltage and the regulated output voltage. The power dissipation of a voltage regulator is dependent on the product of the load current, and the dropout voltage [1]. This means that LDO regulators dissipate less power and as a result they are of increasing popularity in power management systems design, especially for portable and battery operated devices.

Recently, various architectures have been proposed to design an LDO regulator without using the large filtering output capacitor [2]–[5]. Some of these works view an output capacitor-less LDO regulator, as a multi-stage amplifier plus a slew rate enhancement circuitry. Utilizing a slew rate enhancement circuitry boosts the transient time performance of the regulator in terms of amplitude of the under/over shoot and recovery time of the regulated output voltage.

The main focus of this paper is on frequency compensation of output capacitor-less on-chip LDO regulators. For on-chip regulators the output capacitor is small and the dominant pole will no longer be located at output node [2]. Therefore, in order to compensate such a regulator, tens-pF Miller compensation capacitance may be required. The proposed compensation scheme uses a single capacitor of only 70 fF for compensation loop. Also, the presented LDO regulator uses a slew rate enhancement circuitry to improve the transient performance. The designed slew rate enhancement circuit uses a small coupling capacitor of 0.5 pF. Altogether, the total amount of required capacitance for the proposed LDO is small and as a result it is highly appropriate for SoC suited designs.

II. UTILIZED LDO REGULATOR ARCHITECTURE

Fig. 1 shows the structure of a three stage LDO voltage regulator. It consists of a two stage error amplifier, a power MOSFET (M_P) as the output stage, a resistive feedback network (R_{f1} and R_{f2}), frequency compensation loop, and a slew rate enhancement circuitry. The load is modeled by the capacitor C_o, representing the load capacitance and the current source, I_{Load}. Here, V_{ref} is the reference voltage and V_{DD} represents the line voltage.

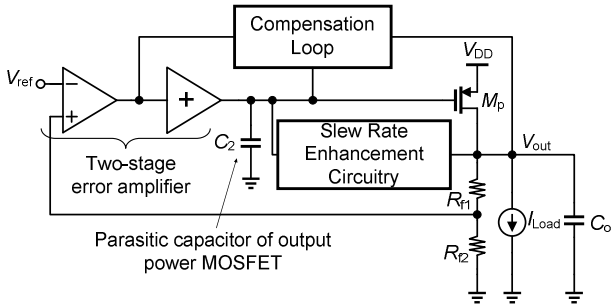

Fig. 1. Utilized LDO voltage regulator architecture.

Since a regulator is expected to provide large amounts of load currents, the power MOSFET is needed to be large in comparison with other transistors in the loop. Therefore, the parasitic capacitance at the gate of the power transistor (C_2) is large. In order to have a better transient performance for the regulator, the slew rate enhancement circuitry is applied to drain extra current from the gate of the power MOSFET during transient times to discharge the large parasitic capacitor of the large output power transistor.

III. CIRCUIT IMPLEMENTATION

Here, the design methodology for the LDO regulator is discussed. The circuit design approach consists of developing a reliable frequency compensation topology and designing an efficient slew rate enhancement circuitry.

A. The ac Response of the Proposed LDO

In order to discuss the ac response of the LDO regulator with newly proposed compensation topology, consider the

block diagram shown in Fig. 2. It models the regulator as a three stage amplifier by considering the output power MOSFET as an amplifier. Therefore, g_{m1}, g_{m2}, and g_{m3}, are the transconductances and R_1, R_2, and R_o are the output resistances of the first, second, and third (output) stages, respectively. Also, C_1 and C_2 represent the parasitic capacitances of the first and second stages, respectively and C_o is the load capacitance. Moreover, it employs a feedback amplifier, A_v, in series with a capacitor, C_m, and a feedforward stage, g_{m4}, all for pole splitting and generating left half plane (LHP) zeros to improve the stability and gain-bandwidth product. Here, R_v is the output resistance and g_v is the transconductance of the feedback amplifier. It should be noticed that due to the large aspect ratio of the output stage (power MOSFET), the effect of parasitic capacitor, C_{gd}, cannot be neglected. Moreover, in this model the slew rate enhancement circuitry is omitted because it basically functions during transients and does not affect the ac response and stability of the LDO regulator.

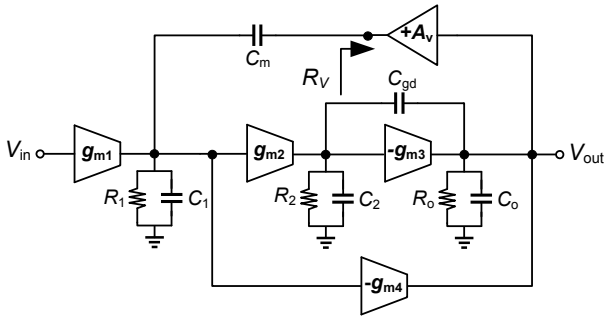

Fig. 2. Block diagram of the LDO for ac response.

The open loop transfer function of the regulator can be derived by analysis the small signal model of the proposed topology shown in Fig. 3 and can be described by:

$$A_V(s) = A_{dc}\frac{1+as+bs^2}{1+cs+ds^2+es^3+fs^4} \tag{1}$$

where $A_{dc}(=-g_{m1}g_{m2}g_{m3}R_1R_2R_o)$ is the dc gain of the LDO.

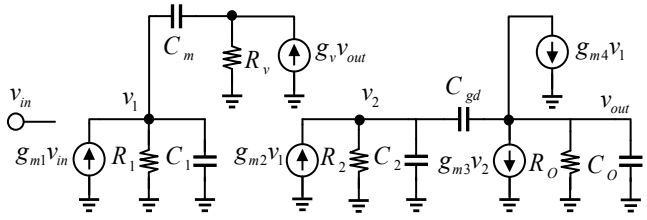

Fig. 3. Small signal model of the proposed compensation topology.

Since an LDO regulator is expected to sustain its stability for full load current range, the transfer function of the system is derived individually for three different operating regions; light load, medium load, and heavy load. The dominant pole for all loading conditions is equal and is estimated by:

$$\omega_{P,dom} = -\frac{1}{g_{m2}g_{m3}R_1R_2R_og_vR_vC_m} \tag{2}$$

In the light load region (e.g. I_{Load} = 0 mA), the output MOSFET is in weak inversion and the constants of the transfer function are approximately given by:

$$a = \frac{g_{m3}C_mR_vg_{m2}+g_{m4}(C_2+C_{gd})}{g_{m2}g_{m3}},\quad b = \frac{g_{m4}R_vC_m(C_2+C_{gd})}{g_{m2}g_{m3}}$$

$$c = g_{m3}R_oC_mR_1g_vR_vg_{m2}R_2,\quad d = R_2C_mR_1g_vR_vg_{m4}R_o(C_{gd}+C_2)$$

$$e = R_2R_oC_oC_mR_1(C_{gd}+C_2),\quad f = R_2R_oC_oC_mR_vC_1R_1C_2. \tag{3}$$

Based on (3), the poles and zeros of the transfer function can be obtained. The zeros and non-dominant poles are given by:

$$\omega_{p,nd1} = -\frac{g_{m3}g_{m2}}{g_{m4}(C_2+C_{gd})},\quad \omega_{p,nd2} = -\frac{g_vR_vg_{m4}}{C_o}$$

$$\omega_{z,nd} = -\frac{g_{m1}g_{m3}}{g_{m4}R_vC_m(C_2+C_{gd})}$$

$$\omega_{z,dom} = -\frac{g_{m2}g_{m3}}{g_{m3}g_{m2}C_mR_v+g_{m4}(C_{gd}+C_2)}. \tag{4}$$

For medium load condition (e.g. I_{Load} = 10 mA), the power MOSFET is in saturation region and the transfer function constants change and can be obtained as follows:

$$a = C_mR_v,\quad b = \frac{C_mR_vg_{m4}(C_2+C_{gd})}{g_{m2}g_{m3}}$$

$$c = g_{m3}R_oC_mR_1g_vR_vg_{m2}R_2,\ d = g_{m3}R_oR_2C_mR_1C_{gd}$$

$$e = g_{m3}R_oR_2C_mR_vC_1R_1C_{gd}+C_2R_2C_oR_oC_mR_1$$

$$f = R_2R_oC_oC_mR_vC_1R_1C_2. \tag{5}$$

Based on the above, the zeros and non-dominant poles for medium load region are given by

$$\omega_{p,nd1} = -\frac{g_{m2}g_vR_v}{C_{gd}},\quad \omega_{p,nd2} = -\frac{g_{m3}R_vC_1C_{gd}}{g_{m3}R_v^2C_1^2C_{gd}+C_2C_o}$$

$$\omega_{z,nd} = -\frac{g_{m2}g_{m3}}{g_{m4}(C_2+C_{gd})},\quad \omega_{z,dom} = -\frac{1}{C_mR_v}. \tag{6}$$

Finally, for the heavy load condition (e.g. I_{Load} = 100 mA), as the load current further increases, the power MOSFET enters the triode region and the constants of the transfer function change and are described by

$$a = C_mR_v,\ b = \frac{g_{m4}C_mR_v(C_2+C_{gd})}{g_{m3}g_{m2}},\quad c = g_{m3}R_oC_mR_1g_vR_vg_{m2}R_2$$

$$d = R_og_{m3}R_2C_mR_1C_{gd}+C_2R_2C_mR_1$$

$$e = R_og_{m3}R_2C_mR_vC_1R_1C_{gd}+C_2R_2C_mR_vC_1R_1$$

$$f = R_2R_oC_oC_mR_vC_1R_1C_2. \tag{7}$$

Therefore, the zeros and non-dominant poles for heavy load condition are estimated as follows:

$$\omega_{p,nd1} = -\frac{g_vg_{m2}g_{m3}R_vR_o}{g_{m3}R_oC_{gd}+C_2},\quad \omega_{p,nd2} = -\frac{1}{C_1R_v}$$

$$\omega_{z,nd} = -\frac{g_{m2}g_{m3}}{g_{m4}(C_2 + C_{gd})}, \qquad \omega_{z,dom} = -\frac{1}{C_m R_v}. \tag{8}$$

The whole idea of the system design is to calculate the pole-zero locations of the open loop small signal transfer function, and to arrange them in a way to optimize the performance such as the gain-bandwidth product and phase margin. As for the uncompensated system there are multiple poles located close to each other and below unity gain frequency, the pole splitting is needed to be applied [6].

The multiplication of low frequency gain by dominant pole frequency yields the gain-bandwidth product given by:

$$\omega_{GBW} = \frac{g_{m1}}{g_v R_v C_m}. \tag{9}$$

It can be seen from (9) that by increasing the feedback amplifier gain ($g_v R_v$), the value of Miller capacitor, C_m, and thus the chip die area and fabrication cost can be reduced. By comparing the dominant pole and non-dominant poles for the three operating regions, it can be concluded that the dominant pole is pushed towards the origin and the non-dominant poles are located at higher frequencies and thus the pole splitting task is accomplished. Since the power MOSFET is large, its gate-source capacitance, C_2, has significant value. Therefore, in (4) by setting g_{m4} large enough, the dominant zero will cancel the first non-dominant pole for the light load condition. It is evident that the pole-zero cancellation is almost complete. Consequently, the effect of a low frequency doublet in transient response is negligible [7]. In case of medium and heavy load operating conditions, according to (6) and (8), the first non-dominant poles are almost equal. To have the first non-dominant pole cancelled with the dominant zero the following constraint has to be satisfied:

$$C_m = \frac{C_{gd}}{g_{m2} g_v {R_v}^2}. \tag{10}$$

It can be investigated that following the above constraint will result in a sufficiently accurate pole-zero cancellation for the full range of the load current. To allow a single pole property below the unity gain frequency, the second non-dominant poles and the non-dominant zeros are needed to be located beyond the unity gain frequency. To achieve this, the worst case among the three loading conditions has to be satisfied. Therefore, from (4), (6), and (8), the second non-dominant pole and the non-dominant zero with the smallest values have to be placed over the unity gain frequency. Here, the second non-dominant pole and the non-dominant zero for the medium and heavy load conditions are closer to origin almost equally. Therefore, other constraints are estimated as:

$$g_v > \frac{g_{m1}C_1}{C_m}, \qquad R_v > \frac{g_{m1}g_{m4}(C_2 + C_{gd})}{g_{m2}g_{m3}g_v C_m}. \tag{11}$$

The circuit implementation of the proposed LDO regulator is shown in Fig. 4. It employs a two stage error amplifier to increase the low frequency gain and hence power supply rejection (PSR) which is complement of supply gain, line, and load regulations. The first stage of the regulator is formed using a folded cascode amplifier which consists of transistors M_1 to M_9. Transistors M_2 and M_3 determine the first stage transconductance. Transistors M_{10} to M_{13} provide the second stage. The third stage is formed by a large PMOS, M_P. Transistor M_{15} acts as the feedforward stage, g_{m4}. Transistors M_{16} to M_{23} establish the feedback amplifier and C_m is the Miller feedback loop capacitor. The shunt negative feedback is provided by a resistive network, including R_{f1} and R_{f2}. As it is previously mentioned, I_{Load} and C_o model the load for the LDO regulator.

B. Transient Response Optimization

As mentioned, to improve the transient response of the regulator, the slew rate enhancement circuitry is applied. By considering Fig. 4, this circuit is formed by transistors M_{14}, M_{24}, M_{25}, resistor R_a, and capacitor C_a (=0.5 pF). At steady state, M_{14} is in cut-off so it does not affect the stability. Whenever undershoot appears at the output voltage, it is amplified by a common source stage including M_{24} and M_{25}. Therefore, the gate- source voltage of transistor M_{14} increases, M_{14} turns on, and it helps discharge the gate parasitic capacitor of M_P and hence improves the settling time of the regulated output voltage.

IV. SIMULATION RESULTS

The proposed on-chip LDO regulator is designed and simulated in standard 0.35 µm CMOS technology using HSPICE. The simulated LDO specifications are shown in Table I. The simulation results are compared with existing works in Table II. It should be noticed that comparing the simulation results with experimental measurements is not fair. However, the newly proposed topology lowers the on-chip capacitance and improves the performance considerably. The frequency characteristics and transient time response are shown in Figs. 5 and 6, respectively.

TABLE I. LDO PERFORMANCE SUMMARY.

Supply Voltage	**1.8 V – 3 V**
Output Voltage	**1.6 V**
Load Regulation	**0.2 mV/100 mA**
Line Regulation	**0.4 mV/1.2 V**
Recovery Time **0 mA→100 mA** **100 mA→0 mA**	 **2.5 µs** **0.6 µs**
Minimum Phase Margin	**60 deg.**
Loop Gain	**81 - 97 dB**
Power Supply Rejection (PSR)* **@ I_{Load}=10 mA**	**83 dB @ 10 Hz** **53 dB @ 100 kHz**

* PSR = $1/A_{IN}$ (A_{IN} (supply gain) = $\Delta V_{OUT}/\Delta V_{DD}$) [1].

V. CONCLUSIONS

A new compensation topology for on-chip LDO regulator has been proposed. This new compensation scheme requires a small amount of capacitance, making it suitable for systems-on-chip (SoCs). Moreover, a slew rate enhancement circuitry is applied to improve the transient response. The presented LDO regulator consumes low quiescent current and boosts the gain-bandwidth product by generating LHP zeroes. This leads to higher power supply rejection and lower recovery time.

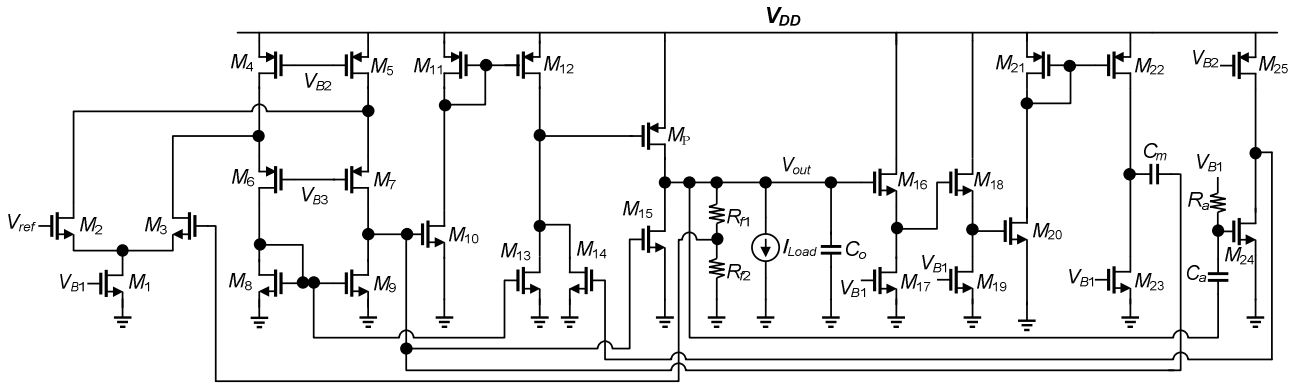

Fig. 4. Circuit realization of the proposed LDO regulator.

TABLE II. COMPARISON OF RESULTS.

	[2] 2010	[3] 2003	[4] 2007	[5] 2007	[8]* 2009	[9] 2010	This work*
Technology (µm)	0.35	0.6	0.35	0.35	0.13	0.5	0.35
$I_{Load,MAX}$ (mA)	100	100	50	100	50	100	100
V_{DROP} (mV)	200	200	200	200	100	200	200
I_Q (mA)	0.02	0.038	0.065	0.1	0.2	0.045	0.025
Recovery Time (µs)	<9	2	~15	30	<0.6	N.A.	2.5
$C_{on\text{-}chip}$ (pF)	7	12	21	6	<16	65.2	0.07 +0.5**
FOM* (ns)**	1.8	0.76	19.5	30	2.4	N.A.	0.625

*Simulation Results.

**0.5 pF is the amount of capacitance required for slew rate enhancement circuitry.

***FOM=T_R (Recovery time). I_Q / $I_{Load,MAX}$. (The smaller FOM means the better performance).

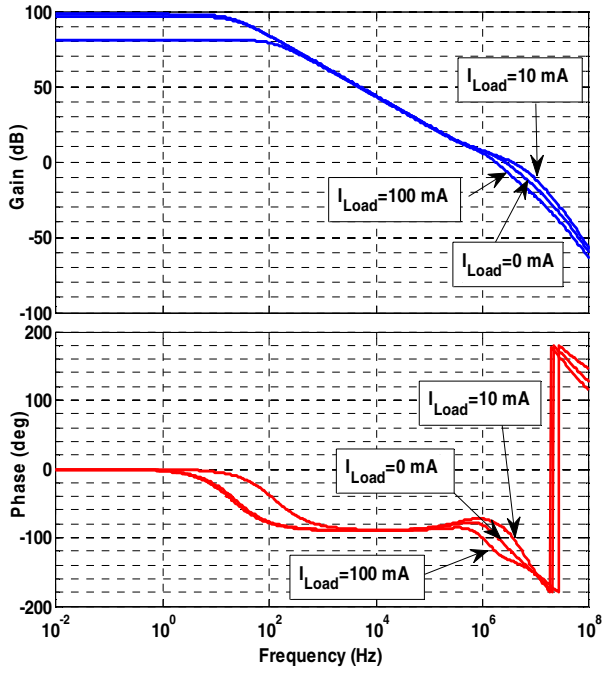

Fig. 5. Frequency response of the proposed LDO.

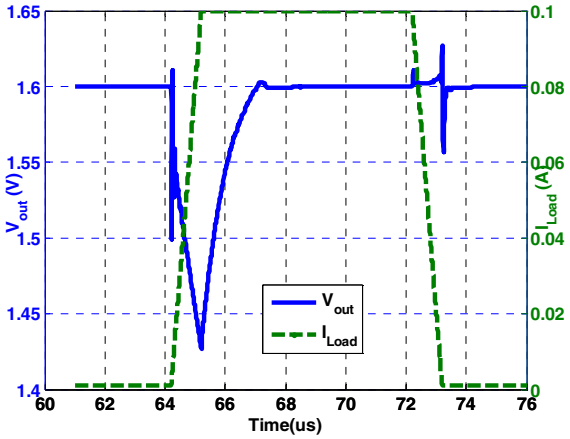

Fig. 6. Simulated load regulation @ V_{DD} =1.8 V with C_O=100 pF for load current from 1 mA to 100 mA and 100 mA to 1 mA.

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