2021 Iranian International Conference on Microelectronics (IICM)

A Low-Power Low-Noise Neural Recording Amplifier With Improved Telescopic-Cascode OTA

Mohammad-Amin Mohtasham-Nia
Department of Electrical Engineering
Amirkabir University of Technology (Tehran Polytechnic)
Tehran, Iran
amin.mn664@aut.ac.ir

Mohammad Yavari
Department of Electrical Engineering
Amirkabir University of Technology (Tehran Polytechnic)
Tehran, Iran
myavari@aut.ac.ir

***Abstract*—In this paper, a fully-differential low-power low-noise neural recording amplifier with a novel recycling telescopic-cascode (RTC) operational transconductance amplifier (OTA) is presented. In the proposed RTC-OTA, the current recycling and positive feedback cross-coupled transistors are utilized to significantly improve the OTA's parameters such as DC gain and unity gain bandwidth. The gain enhancement also improves the linearity in the closed-loop structure. Extensive analytical calculations and simulation results using the 0.18-µm TSMC CMOS process are provided to evaluate the usefulness of the proposed OTA. The simulated neural recording amplifier achieves 4.46 μV_{rms} input-referred noise over 1 Hz-10 kHz bandwidth, 1.82 noise efficiency factor, -46 dB total harmonic distortion (THD) for an 18 mV_{pp}, 1 kHz sinusoidal input. The power consumption is 2.25 µW from a 1.8-V voltage supply.**

Keywords—CMOS operational transconductance amplifiers, low-noise, low-power, neural recording amplifiers, pseudo resistors, biomedical applications.

I. Introduction

Recent advances in the internet of things (IoT) and the need for more neural monitoring of some patients with Parkinson's disease or fainting, or changes in brain function caused by anxiety about the monitoring environment, has made the idea of using implantable bio-chips in the body, more noticeable for the professionals [1, 2]. Favorite signals in neural recording are classified into two categories: Local Field Potentials (LFP) and Action Potentials (AP). LFPs' frequency range is from 1 Hz to 200 Hz with a maximum amplitude of 1 mV and APs' frequency range is from 200 Hz to 10 kHz with a maximum amplitude of 100 µV [2, 3]. The main challenges in designing implantable neural recording systems are low power consumption and low silicon area because they increase battery life and prevent the loss of living tissues.

In order to reduce the area, power consumption and circuit noise, several techniques have been utilized in previous works. In [4], the source degeneration technique is applied to a double recycling folded-cascode to reduce the input-referred noise. But it also reduces the output swing and voltage gain. In [5-8], chopper amplifiers are used with positive feedback in order to achieve noise requirements and also to compensate low input impedance of chopper amplifiers. However, these amplifiers require clock and extra circuits that increase the power consumption and complexity of the amplifier [9]. The open-loop instrumentation amplifier (IA) in [10] has high noise efficiency and common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR). But the open-loop structure in comparison with the closed-loop one has more sensitivity to the process, voltage, and temperature (PVT) variations and degraded linearity. In [11-13], the proposed amplifier is single-ended that results in low linearity and poor CMRR and PSRR [9]. In [14], the fully-differential amplifier consists of IA and programmable gain amplifier (PGA). Due to the asymmetry in the IA structure, the linearity of the amplifier is drastically reduced. This paper proposes a low noise neural recording amplifier with a closed-loop structure.

Recently, several techniques have been proposed to improve the performance of conventional folded-cascode amplifier [14-19]. In this paper, a novel recycling telescopic-cascode amplifier (RTCA) is proposed using current recycling and positive feedback cross-coupled techniques resulting in both improved small signal and large signal characteristics. The proposed OTA has been utilized in a neural recording amplifier.

The rest of the paper is set as follows. In Section II, the overall structure of the neural recording amplifier is presented. The proposed recycling telescopic cascode (PRTC) OTA is introduced and compared with the conventional telescopic-cascode (CTC) amplifier in Sect. III. The simulation results are provided in Sect. IV. Finally, Section V concludes the paper.

II. Neural Recording Amplifier Structure

The architecture of the neural amplifier employing the capacitive feedback [20] is shown in Fig. 1. Transistors M_{p1}-M_{p4} are used to realize a pseudo resistor named R_2 whose value is about one Tera ohm [4]. In this Section, the amplifier main specifications are determined such as the transfer function, input noise, and input impedance.

A. Transfer function

The relation between output and input signals in Fig. 1 is obtained as:

$$\frac{V_{out}}{V_{in}}(s) = -\frac{C_1}{C_2}\frac{1 - s\left(\frac{C_2}{G_m}\right)}{\left(1+\frac{1}{sR_2C_2}\right)\left(1+s\frac{C_LC_1}{G_mC_2}\right)} \quad (1)$$

Equation (1) implies that low cut-off frequency (f_L) is set by R_2 and C_2, the mid-band gain is adjusted by the C_1/C_2 ratio, and finally, the high cut-off frequency (f_H) is the ratio of OTA gain-bandwidth product and the mid-band gain. Also, there is a right-half-plane zero (f_z) but by using the

2021 Iranian International Conference on Microelectronics (IICM) | 978-1-6654-8060-4/21/$31.00 ©2021 IEEE | DOI: 10.1109/IICM55040.2021.9730196

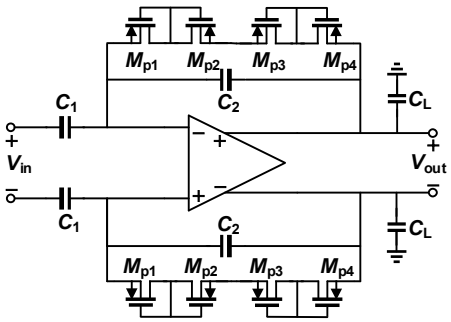

Fig. 1. Neural recording amplifier with capacitive feedback.

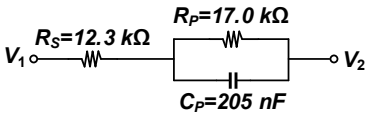

Fig. 2. The electrical model of electrodes.

appropriate value of capacitors and OTA transconductance, this zero will be high enough to have little effect on amplifier performance. For this purpose, the value of capacitors should be selected as [21]:

$$C_2 \approx \sqrt{C_1 C_L} \tag{2}$$

B. Input Impedance

The input impedance of the neural recording amplifier by considering the Miler effect is given by:

$$Z_{input} \approx \frac{2}{\omega C_1} \tag{3}$$

Relation (3) is calculated for an amplifier with a high DC gain and a small input parasitic capacitance. It also shows that the input impedance at mid-band frequency is only dependent on C_1. For the proposed application that we need power efficiency, certain mid-band gain and low cut-off frequency, the input impedance must be extremely greater than the impedance of the electrodes. Fig. 2 shows the electrical model of electrodes [22]. So, the input capacitors must be approximately smaller than 70 pF.

C. Input-Referred Noise

The input-referred noise (IRN) of the neural amplifier shown in Fig. 1 is obtained as [9]:

$$\overline{V_{ni,Amp}^2} = \left(\frac{C_1 + C_2 + C_{in}}{C_1}\right)^2 \left(\overline{V_{ni,OTA}^2} + \overline{V_{nR2}^2}\right) \tag{4}$$

where C_{in} is the input parasitic capacitor of the OTA, $V_{ni,OTA}$ is the OTA IRN and V_{nR2} is the pseudo resistor noise which often can be negligible [21]. As it is seen in (4), C_1 and C_2 size and their ratio have a relative effect on IRN. Therefore, the amplifier needs to have relatively large capacitors, but this reduces the input impedance. An important point that should be considered is the amount of background noise picked up by the electrodes is about 10 μV_{rms} [2]. So, the total input-referred noise of neural amplifier should be smaller than this amount.

III. Proposed Recycling Telescopic-Cascode OTA

In this section, firstly the structure of the proposed OTA is described, then the analysis of OTA characteristics is presented, and eventually a comparison between the conventional OTA and proposed one will be presented.

A. Proposed OTA Structure

Fig. 3 shows the proposed operational transconductance amplifier. The transistors M_0-M_{10} are corresponding transistors in traditional telescopic-cascode OTA. The input transistors are chosen pMOS rather than nMOS, due to lower flicker noise, and are divided into M_1, M_{1a}, M_2, and M_{2a} to reduce the bias current of output transistors and enhance the output impedance. Transistors M_7, M_{7a}, M_8, and M_{8a} are divided to make a two-path amplifier. Transistors M_{5a} and M_{6a} are used to form the wide-swing cascode current mirrors for improved matching. Transistors M_{5b}, M_{6b}, M_{7b}, and M_{8b} are used in a cross-coupled structure instead of the current mirror structure in order to realize a local positive feedback network at M_7 and M_8 gates [19]. A simple common-mode feedback circuit consisting of transistors M_9 and M_{10} transistors is used to control the output common-mode voltage. Finally, the biasing voltages V_{b1}-V_{b3} and input common-mode voltage are provided by a simple constant current biasing network.

In order to achieve low input-referred noise and low power consumption, maximizing the input transistors' transconductance and area is necessary and leading the input transistors into deep sub-threshold region. By this maximizing, mismatch effects are reduced and also, improvement in CMRR, PSRR, and output offset is achieved. k and m are the ratio in current mirrors and they are dependent on each other as follows:

$$k = m + 1 \tag{5}$$

In the following, a detailed analysis of the proposed OTA is provided.

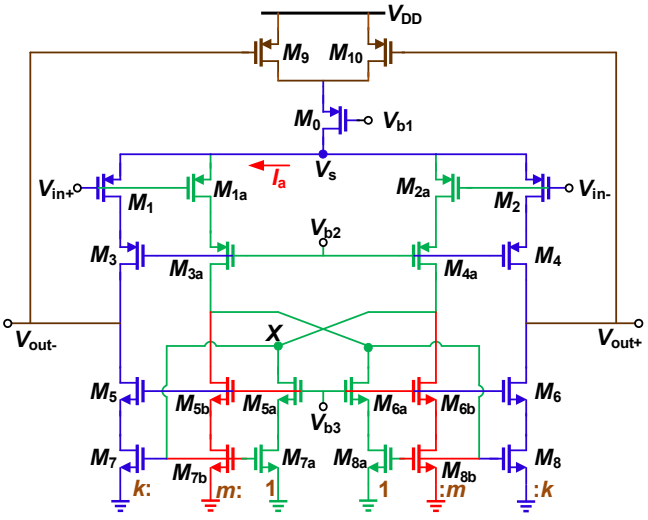

Fig. 3. The proposed recycling telescopic-cascode OTA.

B. Small Signal Transconductance and DC gain

The small-signal transconductance (G_m) of the proposed OTA is examined by finding the ratio between differential output short-circuit current and the input signal, as in the following equations.

$$G_{m,pRTC} = \left(\frac{2}{1-m}\right) g_{m1} \tag{6}$$

where g_{m1} is the small-signal transconductance of M_1. Assuming a dominant pole for amplifier at the output node, the gain-bandwidth product of proposed RTC OTA is obtained as:

$$GBW \approx \frac{G_m}{C_L} \approx \left(\frac{2}{1-m}\right)\frac{g_{m1}}{C_L} \tag{7}$$

The DC gain of the proposed OTA is given by:

$$A_{DC} \approx \left(\frac{2}{1-m}\right) g_{m1} \times \left(g_{m3} r_{ds3} r_{ds1} \parallel g_{m5} r_{ds5} r_{ds7}\right) \tag{8}$$

Where r_{dsi} is the drain-source small-signal resistance.

C. Frequency Poles and Zeros

The frequency poles and zeros of the proposed OTA are obtained as:

$$\omega_{p1} = \frac{1}{R_{out} C_L},\ \omega_{p2} = (1-m)\frac{g_{m7}}{C_X},\ \omega_{z1} = \left(\frac{2}{1-m}\right)\frac{g_{m7}}{C_X} \tag{9}$$

It is clear that by increasing m, the second pole is decreased, resulting in degraded stability. So, there is a trade-off between stability and gain-bandwidth [19].

D. Comparison With Conventional OTA

In this sub-section, the proposed OTA is compared with the conventional telescopic-cascode (CTC) OTA. To make the comparison more tangible, m = 1/3 and k = 4/3 and the same power consumption are assumed in both OTAs. So, the bias current of the input transistors in CTC OTA is twice than that of PRTC OTA.

The G_m of both structures is related as:

$$\frac{G_{m,PRTC}}{G_{m,CTC}} = \frac{g_{m1,PRTC}}{g_{m1,CTC}}\left(\frac{2}{1-m}\right) = 1.5 \tag{10}$$

Where $G_{m,PRTC}$ and G_{mCTC} are the total transconductances of the proposed OTA and the traditional one, respectively. Consequently, the gain-bandwidth product ratio of the OTAs is related as:

$$\frac{GBW_{PRTC}}{GBW_{CTC}} = \frac{G_{m,PRTC}}{G_{m,CTC}}\left(\frac{2}{1-m}\right) = 1.5 \tag{11}$$

Due to the inverse relation between bias current and small-signal resistance in transistors, their DC gain is related as:

$$\frac{A_{DC,PRTC}}{A_{DC,CTC}} \approx \left(\frac{2}{1-m}\right)\frac{g_{m1,PRTC}}{g_{m1,CTC}}\frac{R_{out,PRTC}}{R_{out,CTC}} \approx \left(\frac{2}{1-m}\right) = 3 \tag{12}$$

Where $A_{DC,PRTC}$ and $A_{DC,CTC}$ are corresponding to the proposed OTA and the traditional one, respectively. Nonetheless, the phase margin is degraded because the proposed OTA has more non-dominant poles.

IV. Simulation Results

In this section, firstly, the relations obtained in pervious section are verified by providing the simulation results of both proposed and conventional OTAs in HSPICE using a 0.18-µm TSMC CMOS process. Then the simulation results of the neural recording amplifier are presented. Due to amplifier application, all simulations are done at 37°C.

A. OTA Simulation Results

The PRTC and CTC OTAs were designed for low-power applications with a 1.8 V power supply and the same power consumption. The simulated device sizes are summarized in Table I. The channel length of transistors is chosen long enough to achieve low input-referred noise. As mentioned before, the transistors are in the sub-threshold region to maximize the amplifier transconductance. The biasing circuit (not shown here) is a simple constant current network where the wide-swing cascode current mirrors are used to provide large output signal swing.

In open-loop simulations, C_L is 2.5 pF. The open-loop frequency response is shown in Fig. 4 indicating that DC gain in PRTC and CTC OTAs is 72.8 and 63.3 dB, respectively. The phase margin of the PRTC OTA is lower than the CTC one but as it is obvious from Fig. 5, in the intended application, the PRTC OTA has no instability issue and it is faster than CTC OTA. For total harmonic distortion (THD) and transient response, the simulation is done in a capacitive feedback configuration. The input and feedback capacitors are 50 pF and 0.5 pF, respectively, to have 40 dB gain. For time response, a step signal with 5 mV amplitude and for THD, a sinusoidal signal with 1 kHz frequency and 20 mV_{pp} amplitude is applied to the simulated OTAs. The THD in PRTC OTA is -49 dB and in CTC one, it is -44 dB. To provide a clear view, the simulation results are summarized in Table II.

TABLE I. Device Sizes of The Simulated OTAs.

Device	*M*×*W*(*µm*)/*L*(*µm*)	
	PRTC OTA	CTC OTA
M_0	1 × 12.0/9.0	1 × 12.0/9.0
$M_{1,2}$	20 × 20.0/1.0	20 × 40.0/1.0
$M_{1a,2a}$	20 × 20.0/1.0	-
$M_{3,4}$	10 × 20/10.0	10 × 40.0/1.0
$M_{3a,4a}$	10 × 20/10.0	-
$M_{5,6}$	1 × 8.0/4.5	1 × 16.0/4.5
$M_{5a,6a}$	1 × 6.0/4.5	-
$M_{5a,6a}$	1 × 2.0/4.5	-
$M_{7,8}$	1 × 16.0/12.0	1 × 32.0/12.0
$M_{7a,8a}$	1 × 12.5/12.0	-
$M_{9,10}$	1× 40.0/0.5	1×0.0/0.5

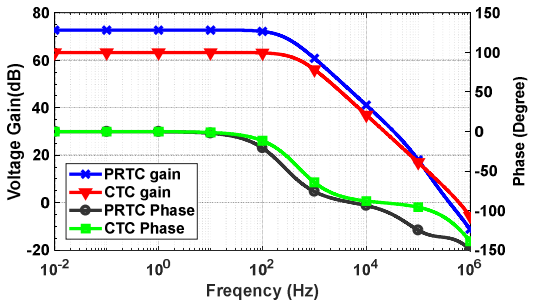

Fig. 4. Open-loop frequency response of the simulated OTAs.

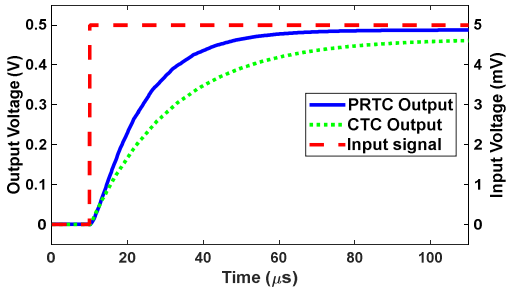

Fig. 5. Closed-loop transient response of the simulated OTAs.

TABLE II. THE OPEN-LOOP SIMULATION RESULTS SUMMARY.

Parameter	PRTC OTA	CTC OTA
Technology	0.18 µm 1P6M TSMC	
Power supply voltage	1.8 V	
Load capacitor	2.5 pF	
Static power consumption	2.252 µW	2.249 µW
DC gain	72.8 dB	63.3 dB
Gain×Bandwidth @ frequency ⩽ 20kHz	1.132 MHz	0.708 MHz
THD @ (20 mV_{pp}, 1 kHz sin input)	-49 dB	-44 dB
IRN (0.1 – 20 kHz)	4.90 µVrms	4.66 µVrms
FOM* (kHz × pF / µW)	1256.7	787.0

* FOM = GBW × C_L / Power

B. *Neural Amplifier Simulation Results*

The proposed neural recording amplifier shown in Fig. 1 is designed and simulated with C_L= 2 pF, C_1 = 100×C_2 = 50 pF and (W/L) = 3.0 µm/20.0 µm for $M_{p1\text{-}p4}$ transistors to make 40 dB gain amplifier with an approximately 1 Hz to 10 kHz bandwidth. The frequency response of neural amplifier in different process corner cases and power supply variations is depicted in Fig. 6. In these simulations, V_{DD} is 1.6 V in SS corner and it is 2 V in FF corner. For typical corner, V_{DD} is 1.8 V. The mid-band gain in TT corner is 39.7 dB in the frequency band of 0.36 Hz-11.8 kHz that covers the bio-signals frequency range.

The input-referred noise of the amplifier is 1.90 µVrms for LFP frequency bandwidth and it is 4.04 µVrms for AP frequency band. The simulated noise power spectral density (PSD) is shown in Fig. 7 in different process corner cases and power supply voltages. The noise efficiency factor (NEF) for the proposed amplifier is 5.49 and 1.66 and the power efficiency factor (PEF) is 54.26 and 4.97 in LFP (1-200 Hz) and AP frequency ranges (0.2-10 kHz), respectively.

The THD is measured when the input signal is 18 mV_{pp}, 1 kHz sinusoidal. The FFT of the output signal is shown in Fig. 8. The amplifier THD at these conditions is -46.0 dB.

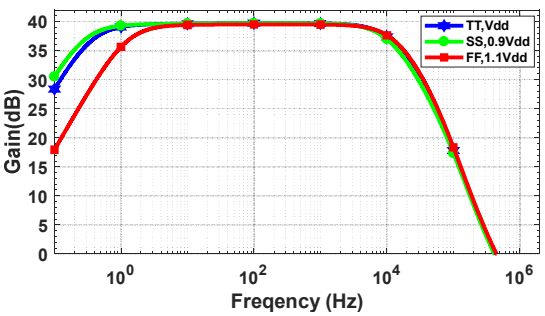

Fig. 6. Simulated frequency response of the proposed neural amplifier.

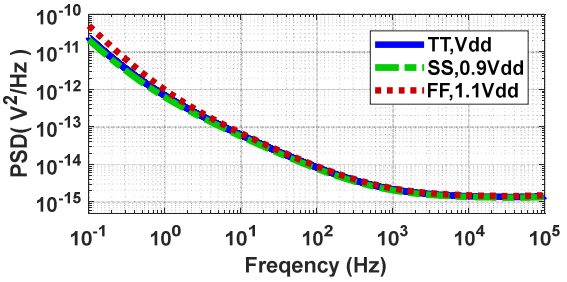

Fig. 7. Simulated input noise density of the proposed neural amplifier.

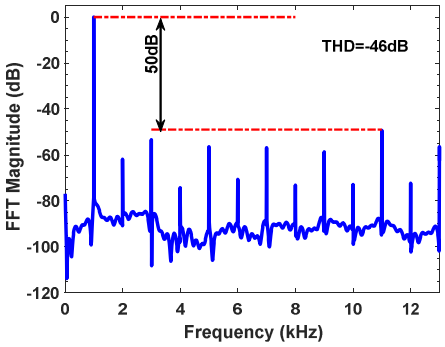

Fig. 8. THD of the neural amplifier for an 18 *mVpp* input.

The statistical distribution of CMRR and PSRR is shown in Fig. 9. The amplifier CMRR in 50 Hz frequency is 62.8 dB and the PSRR is 64.6 dB. The input impedance in typical conditions equals 119.4 MΩ at 50 Hz. Besides, Fig. 10 shows the amplifier stability in different process corner cases and power supply voltages. A summary of the simulation results in different corner cases and the supply voltage is provided in Table III. Also, according to Table IV, the overall performance of the proposed neural recording amplifier is comparable with the best reported designs in literature.

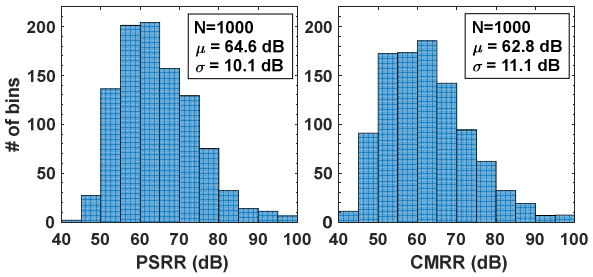

Fig. 9. CMRR and PSRR of the neural amplifier at 50 Hz.

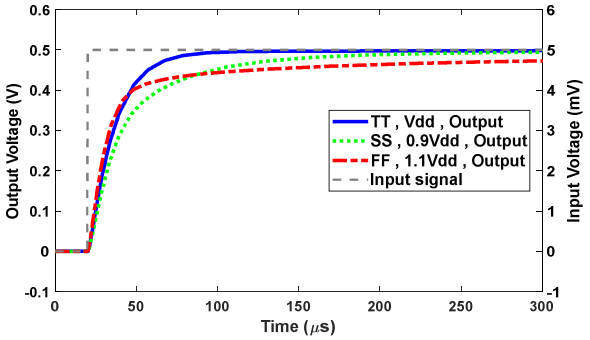

Fig. 10. Step response of proposed amplifier at 37°C.

TABLE III. THE PVT SIMULATION RESULATS.

Parameter	TT V_{DD} = 1.8 V	FF V_{DD} = 2.0 V	SS V_{DD} = 1.6 V
Power consumption (µW)	2.25	2.35	2.15
Mid-band gain (dB)	39.7	39.5	39.7
Bandwidth (Hz)	0.36-11.8 k	1.2-13.6 k	0.27-10.6 k
THD (dB)	-46.0	-43.7	-46.0
IRN (1–10k Hz) (µVrms)	4.46	4.62	4.34
NEF	1.82	1.82	1.83
PEF	5.96	6.65	5.36
Input Impedance (MΩ)	119.4	142.1	105.0

TABLE IV. PERFORMANCE COMPARISON OF THE PROPOSED NEUARAL RECORDING AMPLIFIER WITH THE STATE-OF-THE-ART WORKS (BW ≥ 5KHZ).

Parameter		This work	[2]* JSSC'17	[4] AICSP'20	[5] * SSC-L'19	[6] * JSSC'19	[7] * JSSC'17	[9] AICSP'19	[10] * ISCAS'17	[11] AEU'18	[12] AICSP'18	[13] AICSP'18
Technonlogy (nm)		180	40	180	180	180	40	180	180	65	65	180
V_{DD}(V)		1.8	1.2	1.8	1.2	1.8	1.2	0.6	1.8	1	1	1.8
Power (µW)		2.25	2	1.53	2.6	3.24	2.5	0.72	32.7	1.12	0.6	4.07
Midband gain (dB)		39.7	26	40.02	51-59	40	25.7	39.2	30-40	40	30	39.75
Bandwidth (Hz)	f_L	0.36	0.2	5.69	0.5	0.35	0.12	0.01	0.05	0.66	220	0.3
	f_H	11.8k	5k	5.45k	5k	5.4k	5k	10k	11k	5k	17k	4.4k
IRN	LFP	1.90	2	3.27	2.0	0.65	1.8	4.98	1.34	8.1	7.81	3.19
	AP	4.04	7		3.2	2.14	5.3					
NEF	LFP	5.49	7	1.58	9.9	2.37	7.4	2.13	1.92	4.62	N/A	2.78
	AP	1.66	4.9		3.2	1.56	4.4					
PEF	LFP	54.26	58.8	4.5	N/A	11.1	65.7	2.71	6.63	21.34	N/A	13.9
	AP	4.97	28.8			4.38	23.2					
CMRR (dB)		62.9 @50Hz	N/A	66.55	70	>100	78	77	84	124	65	76
PSRR (dB)		64.6 @50Hz	N/A	54.99	N/A	>70	76	>60	87	88	N/A	77.6
Input Impedance (Ω)		119.1M @50Hz	300M @DC	N/A	3G @DC	440M	1.6G @DC	N/A	N/A	N/A	N/A	N/A
THD		-46.0dB @18mVpp @1kHz (input)	-74dB @40mVpp @1kHz (input)	-40dB @1.2Vpp (output)	-35.6dB @1mVpp @1kHz (input)	-61dB @5mVp @1kHz (input)	-76dB @40mVp @1kHz (input)	-75dB @1mVpp @1kHz (input)	N/A	N/A	IM3= -63dB @ (9.5 & 10.5) kHz	-40dB @15mVpp (input)

*Measurement results

V. CONCLUSIONS

This paper presents a low-power amplifier with a capacitive feedback structure for neural recording systems. By using the local positive feedback network in the proposed recycling telescopic-cascode OTA, the open-loop gain and closed-loop linearity are enhanced without any additional power consumption. The proposed OTA has been designed for a neural amplifier. The simulation results in 0.18-µm CMOS shows the GBW in the proposed OTA is increased about 50% in comparison with the conventional telescopic OTA with the same power consumption,. Besides, it improves DC gain by 2.9 times and the linearity by about 70%. In addition, the neural amplifier has a NEF equal to 5.49 and 1.66 for LFP and AP signals, respectively, which is comparable with the best reported designs for neural recording.

REFRENCES

[1] S. Barati and M. Yavari, "An adaptive continuous-time incremental ΣΔ ADC for neural recording implants," International Journal of Circuit Theory and Applications, vol. 47, no. 2, pp. 187-203, Feb 2019.

[2] H. Chandrakumar and D. Markovic, "A High Dynamic-Range Neural Recording Chopper Amplifier for Simultaneous Neural Recording and Stimulation," IEEE Journal of Solid-State Circuits, vol. 52, no. 3, pp. 645-656, Mar. 2017.

[3] S. Barati and M. Yavari, "An Automatic Action Potential Detector for Neural Recording Implants," Circuits, Systems & Signal Processing, vol. 38, no. 5, pp. 1923-1941, May 2019.

[4] S. R. Venishetty, S. Kumaravel and S, A. Durai, "A power efficient low-noise source degenerated bio-potential amplifier," Analog Integr. Circuits Signal Process, vol. 103, pp. 291–301, May 2020.

[5] A. Samiei and H. Hashemi, "A Chopper Stabilized, Current Feedback, Neural Recording Amplifier," IEEE Solid-State Circuits Letters, vol. 2, no. 3, pp. 17-20, Mar. 2019.

[6] D. Luo, M. Zhang and Z. Wang, "A Low-Noise Chopper Amplifier Designed for Multi-Channel Neural Signal Acquisition," IEEE Journal of Solid-State Circuits, vol. 54, no. 8, pp. 2255-2265, Aug. 2019.

[7] H. Chandrakumar and D. Markovic, "An 80-mVpp Linear-Input Range, 1.6-G Input Impedance, Low-Power Chopper Amplifier for Closed-Loop Neural Recording That Is Tolerant to 650-mV," IEEE Journal of Solid-State Circuits, vol. 52, no. 11, pp. 2811-2827, Nov. 2017.

[8] F. Ansari and M. Yavari, "A High Input Impedance Fully-Differential Chopper Amplifier for Closed-Loop Neural Recording," in 28th Iranian Conference on Electrical Engineering (ICEE), Aug. 2020, pp. 1-5.

[9] X. Zhang, J. Wang and Z. Zhu, "A low-power low-noise amplifier with fully self-biased feedback loop structure for neural recording," Analog Integrated Circuits Signal Process, vol. 99, pp. 199–208, Apr. 2019.

[10] D. M. Das, A. Srivastava, A. Gupta, K. Barot, and M. Shojaei-Baghini, "A Noise-power-area Optimized Novel Programmable Gain and Bandwidth Instrumentation Amplifier for Biomedical Applications," in International Symposium on Circuits and Systems (ISCAS), 2017.

[11] M. Avoli, F. Centurelli, P. Monsurrò, G. Scotti, and A. Trifiletti, "Low power DDA-based instrumentation amplifier for neural recording applications in 65 nm CMOS," International Journal of Electronics and Communications, vol. 92, pp. 30-35, Aug. 2018.

[12] R. Nagulapalli, K. Hayatleh, S. Barker, S. Zourob, and N. Yassine, "An OTA gain enhancement technique for low power biomedical applications," Analog Integrated Circuits Signal Processing, vol. 95, pp. 387-394, Jun. 2018.

[13] R. Sanjay, V. Senthil Rajan and B. Venkataramani, "A low-power low-noise and high swing biopotential amplifier in 0.18 µm CMOS," Analog Integrated Circuits Signal Processing, vol. 96, no. 3, pp. 565-576, Sept. 2018.

[14] Y. Zhao, Z. Shang and Y. Lian, "A 2.55 NEF 76dB CMRR DC-Coupled Fully Differential Difference Amplifier Based Analog Front-end for Wearable Biomedical Sensors," IEEE Transaction Biomedical Circuits and System, vol. 13, no. 5, pp. 918-926, Oct. 2019.

[15] M. Yavari and O. Shoaei, "A Novel Fully-Differential Class AB Folded-Cascode OTA," IEICE Electron. Express, vol. 1, no. 13, pp. 358-362, Oct. 2004.

[16] M. Yavari, "A New Class AB Folded-Cascode Operational Amplifier," IEICE Electron. Express, vol. 6, no. 7, pp. 395-402, Apr. 2009.

[17] R. Assaad and J. Silva-Martinez, "The recycling folded-cascode: a general enhancement of the folded-cascode amplifier," IEEE Journal of Solid-State Circuits, vol. 44, no. 9, pp. 2535-2542, Sept. 2009.

[18] M. Yavari, “Single-Stage Class AB Operational Amplifier for SC Circuits,” IET Electronics Letters, vol. 46, no.14, pp. 977-979, July 2010.
[19] M. Yavari and T. Moosazadeh, “A single-stage operational amplifier with enhanced transconductance and slew rate for switched-capacitor circuits,” Analog Integrated Circuits and Signal Processing, vol. 79, no. 3, p. 589–598, Jun. 2014.
[20] M. Pilar Garde et al., “Super Class-AB Recycling Folded Cascode OTA,” IEEE Journal of Solid-State Circuits, vol. 53, no. 9, pp. 2614-2623, Sept. 2018.
[21] R. R. Harrison, “The Design of Integrated Circuits to Observe Brain Activity,” Proc. IEEE, vol. 96, no. 7, pp. 1203 - 1216, Jul. 2008.
[22] M. Sharma, A. T. Gardner, H. J. Strathman, D. J. Warren, J. Silver, and R. M. Walker, “Acquisition of Neural Action Potentials Using Rapid Multiplexing Directly at the Electrodes,” Micromachines, vol. 9, no. 10, p. 477, Sept. 2018.