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High-Order Sigma-Delta Modulators for Low-Voltage Wideband Applications

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Abstract: *In this paper we have studied high order cascaded sigma-delta modulators that avoid the need of digital filtering in the error cancellation logic. In the proposed structures, a high order single loop modulator is employed in the first stage to achieve higher order noise shaping at low oversampling ratios (OSRs) with more relaxed analog circuit's requirements and without any stability concerns. The proposed topologies are highly tolerant to the quantization noise leakages and robust to the nonlinearity of the circuitry and especially suited for low-voltage implementations. Extensive simulation results are provided to prove the efficiency of the proposed modulator structures.*

Keywords: sigma-delta modulator, MASH structure.

1. Introduction

Delta-sigma modulation is currently a very popular technique for making high-resolution analog-to-digital converters (ADCs) due to their inherent immunity to the circuit non-idealities. In order to employ them in broadband applications, the oversampling ratio (OSR) must be restricted to low values. The single-loop high-order ΣΔ modulators can provide the required resolution with relaxed analog circuit requirements, but they suffer from the stability problems. The multi-stage noise-shaping (MASH) structures guarantee the stable operation, but, they require high accuracy analog integrators to minimize the quantization error leakage resulting from the mismatch between the analog and corresponding digital filters. These integrators are often implemented using power-hungry multistage operational amplifiers and are difficult to implement them in low-voltage implementations [1].

An alternative cascaded ΣΔ modulator that reduces the sensitivity to the noise leakage of traditional MASH structures has been recently proposed in [2] and called the Sturdy MASH (SMASH) modulator. This paper presents high order topologies of ΣΔ SMASH modulators for broadband and low-voltage applications. These structures are composed of feedforward third or fourth-order in first stage and first or second-order in the second stage. For wideband application it is more desirable to spread the noise transfer function (NTF) zeros in the signal passband, and hence this technique is also used in the proposed structures.

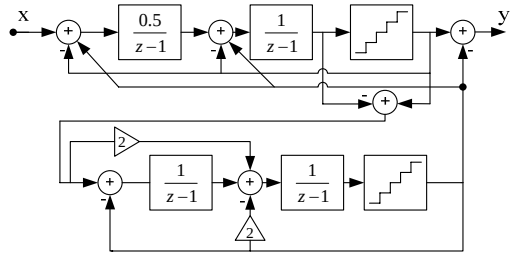

Fig. 1: SMASH 2-2 modulator [2].

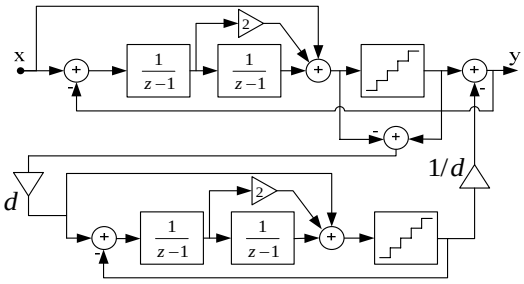

Fig. 2: SMASH 2-2 modulator [4].

The paper is organized as follows. Section II provides the properties of the SMASH structure. Section III presents the topology of the proposed SMASH modulators. Extensive simulation results are provided in section IV to prove the efficiency of the proposed structures and finally conclusions are given in section V.

2. SMASH Structures

The structure of the firstly published SMASH 2-2 modulator is shown in Fig. 1 [2]. In this architecture, the first stage quantization error is used as the input in the second stage, as in traditional MASH structure. But the second stage output is directly subtracted from the output

of the first stage quantizer in the digital domain. The overall output is given by:

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^4 E_1(z) - (1-z^{-1})^4 E_2(z) \quad (1)$$

where $X(z)$ stands for the input signal and $E_1(z)$ and $E_2(z)$ are the quantization error of the first and second stages, respectively. The digital filtering of the stages outputs is eliminated and both quantization errors are fourth-order shaped thanks to the analog filtering only. Nonetheless, this structure needs at least one extra highly linear digital to analog converter (DAC) at the input signal summing node.

In [3] an enhanced version of SMASH 2-2 delta-sigma modulator which reduces the effect of the first stage quantization noise in the overall output has been proposed. The output of this structure is given by:

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^5 E_1(z) - (1-z^{-1})^4 E_2(z) \quad (2)$$

Fig. 2 illustrates the proposed SMASH 2-2 structure in [4]. It has two extensions on the firstly published SMASH 2-2 modulator. It uses the unity signal transfer function (STF) in both modulator stages and locates the digital adder inside the first-stage loop. The output of this modulator is given by:

$$Y(z) = X(z) - \frac{1}{d}(1-z^{-1})^4 E_2(z) \quad (3)$$

where the overall STF equals unity and $E_1(z)$ is completely cancelled, while avoiding any filtering in the digital domain. In Eq. (3), d ($d > 1$) is a scaling factor and used to accommodate the interstage gain and compensated in the digital feedback path from the second stage output to the first input before the digital subtraction of the stages outputs. This scaling factor is used to further decrease the second stage quantization noise in the modulator overall output.

3. Proposed Structures

In the proposed modulator structures, the unity STF is used in both modulator stages, and hence, the effect of the first stage quantization noise in overall modulator's output is completely eliminated.

3.1 SMASH 3-1

For wideband application, it is more desirable to spread the NTF zeros in the signal passband. Figure 3† illustrates the structure of the proposed SMASH 3-1 modulator. This structure employs a feedforward third-order single loop as the first stage and the first-order modulator as the second stage.

The third-order first loop has an FIR NTF which has two complex-conjugate zeros. The overall NTF of the modulator is given by:

$$NTF(z) = (1-z^{-1})^2(1-(2-\delta)z^{-1}+z^{-2})/d \quad (4)$$

†. Here $\int \equiv 1/(1-z^{-1})$ and $D(delay) \equiv z^{-1}$

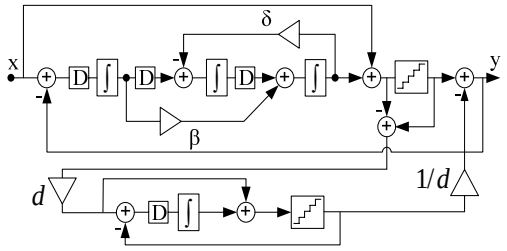

Fig. 3: Proposed SMASH 3-1.

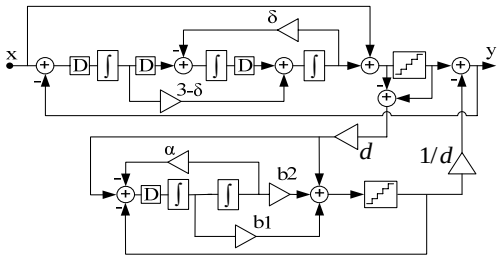

Fig. 4: Proposed SMASH 3-2.

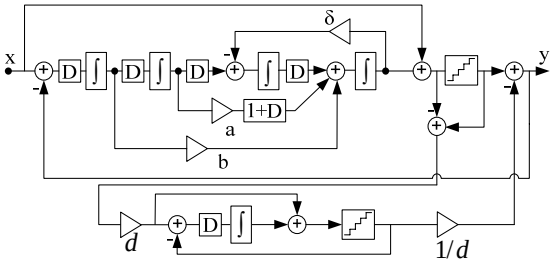

Fig. 5: Proposed SMASH 4-1.

In order to have an FIR NTF, $\beta = 3-\delta$. The value of the coefficient δ is considered in such a way to minimize the inband quantization noise power. Therefore, we have:

$$\delta_{opt} = \arg\min_{\delta} \int_0^{\frac{f_s}{2\times OSR}} \left|(1-z^{-1})^2(1-(2-\delta)z^{-1}+z^{-2})\right|^2 df \quad (5)$$

Assuming $z = e^{j\theta}$ and $\theta = 2\pi f / f_s$, we can find the optimal value by nulling the first derivative, which gives in Eq. (7)

$$\frac{d}{d\delta}\int_0^{\frac{\pi}{OSR}} 4(\cos\theta - 1)^2(2\cos\theta + \delta - 2)^2 d\theta = 0 \quad (6)$$

$$\delta_{opt} = \frac{2\sin\frac{3\pi}{OSR} - 18\sin\frac{2\pi}{OSR} + 90\sin\frac{\pi}{OSR} - \frac{60\pi}{OSR}}{24\sin\frac{\pi}{OSR} - 3\sin\frac{2\pi}{OSR} - \frac{18\pi}{OSR}} \quad (7)$$

The third order first loop reduces the problems with quantization noise leakage from the classical cascade 2-2 or 2-1-1 topologies, leading to the lower amplifier specifications as also stated in [5].

3.2 SMASH 3-2

Figure 4 shows the structure of the proposed SMASH 3-2 modulator. This structure composes of a feedforward third-order in the first stage and a second-order resonator based modulator in the second stage. The first stage is the

same as the proposed SMASH 3-1. In the second stage an FIR based NTF is used in order to enhance the stability of the overall modulator. The coefficients α and δ are used to place the modulator NTF zeros at the inband frequencies in order to shape out the second stage quantization noise more aggressively. The overall NTF of the modulator is given by:

$$NTF(z) = (1-z^{-1})^2(1-(2-\delta)z^{-1}+z^{-2})(1-(2-\alpha)z^{-1}+z^{-2})/d \quad (8)$$

In order to have an FIR NTF, $b_1 = 1$ and $b_2 = 1-\alpha$. The value of the coefficients α and δ are considered in such a way to minimize the inband quantization noise power. By solving the Eq. (10), we found the optimal value of the coefficients α and δ.

$$[\delta_{opt}, \alpha_{opt}] = \arg\min_{\delta,\alpha} \int_0^{\frac{f_s}{2\times OSR}} \left|(1-z^{-1})^2(1-(2-\delta)z^{-1}+z^{-2})(1-(2-\alpha)z^{-1}+z^{-2})\right|^2 df \quad (9)$$

$$\nabla_{(\delta,\alpha)} \int_0^{\frac{\pi}{OSR}} 4(\cos\theta - 1)^2(2\cos\theta + \delta - 2)^2 (2\cos\theta + \alpha - 2)^2 d\theta = 0 \quad (10)$$

As is seen, the overall FIR NTF has four complex-conjugate zeros and one zero on dc. This NTF has high noise shaping ability with sufficient stability margin and hence is more effective for broadband applications.

3.3 SMASH 4-1

The proposed SMASH 4-1 modulator shown in Fig. 5 employs a feedforward fourth-order modulator proposed in [6] as the first stage. One pair of first stage NTF zeros are placed at the inband frequencies to achieve high SNDR. In order to have an FIR NTF $a = 2$ and $b_2 = 4-\delta$. The overall NTF of this structure is given by:

$$NTF(z) = (1-z^{-1})^3(1-(2-\delta)z^{-1}+z^{-2})/d \quad (11)$$

The optimal value of δ is simply calculated by minimizing the inband quantization noise.

$$\delta_{opt} = \arg\min_{\delta} \int_0^{\frac{f_s}{2\times OSR}} \left|(1-z^{-1})^3(1-(2-\delta)z^{-1}+z^{-2})\right|^2 df \quad (12)$$

$$\frac{d}{d\delta} \int_0^{\frac{\pi}{OSR}} 8(1-\cos\theta)^3(2\cos\theta + \delta - 2)^2 d\theta = 0 \quad (13)$$

$$\delta_{opt} = \frac{3\sin\frac{4\pi}{OSR} - 32\sin\frac{3\pi}{OSR} + 168\sin\frac{2\pi}{OSR} - 672\sin\frac{\pi}{OSR} + \frac{420\pi}{OSR}}{-4\sin\frac{3\pi}{OSR} + 36\sin\frac{2\pi}{OSR} - 180\sin\frac{\pi}{OSR} + \frac{120\pi}{OSR}} \quad (14)$$

4. Simulation Results

4.1 4th-Order Modulators

The performance of the proposed SMASH 3-1 (Fig. 3) has been compared to the traditional cascade 2-2, 4th-order feedforward single-loop†, and SMASH 2-2 modulators shown in Figs. 1 and 2 by performing behavioral simulations in MATLAB/Simulink. All topologies operate with an oversampling ratio of 8, 4-bit internal quantizers and 1-V reference voltage and a scaling factor of d = 4. We can calculate the optimal δ for proposed SMASH 3-1 from Eq. (7). For $OSR = 8$, $\delta = 0.109$ and $\beta = 1.891$.

Figure 6 illustrates the signal-to-noise and distortion ratio (SNDR) versus the first integrator dc gain for the five above-mentioned structures. In this simulation, a -6 dBFS sinusoidal input signal was applied. As shown in Fig. 6, for the proposed SMASH 3-1, an SNDR of 91.7dB is achievable with an opamp DC gain of only 30dB.

In Fig. 7 the SNDR versus the input signal amplitude is illustrated. In this simulation, an amplifier dc gain of 50 dB was used for all structures. Note that the overload level of the proposed SMASH is considerably large although it employs a third order modulator in the first stage.

The overload level of the diverse topologies is shown in Table I, together with the output swing requirements of the amplifiers. The combination of unity STFs and multi-bit quantization leads to a remarkable relaxation of the output swing for this structure.

We have studied the sensitivity to noise leakages due to mismatch for the proposed SMASH 3-1 on basis of Monte-Carlo simulation. An input signal amplitude of -6dBFS was used for this simulation. We have done 100 Monte-Carlo simulations in every point and calculated the average result. As shown in Fig. 8, this structure has large immunity to the mismatches.

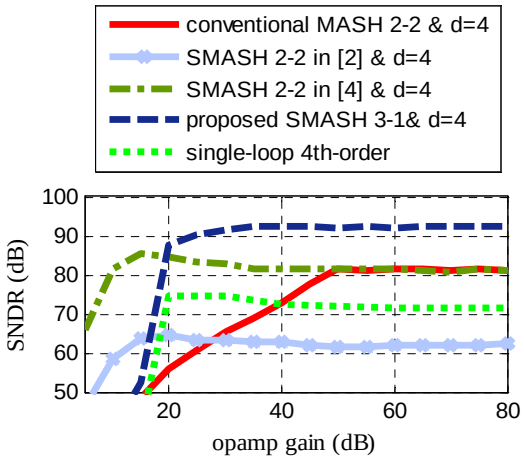

Fig. 6: SNDR against opamp gain

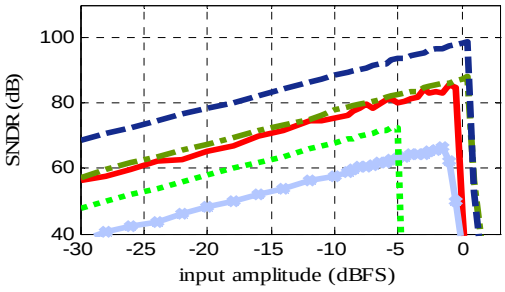

Fig. 7: SNDR against input amplitude

†. Single-loop modulators in this paper are Cascade-of-integrators; feedforward form (CIFF) which discussed in [1].

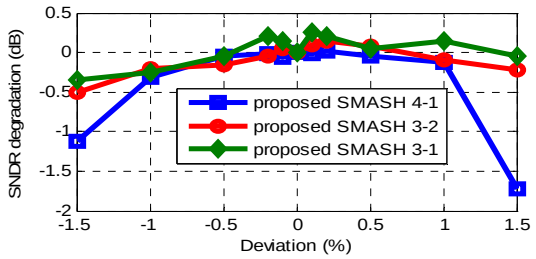

Fig. 8: SNDR degradation due to coefficient mismatch for proposed structures

TABLE I: Overload level and Output Swing Requirements of the 4th-Order Modulator With Various Structures.

Topology	Overload level (dBFS)	Intg. 1	Intg. 2	Intg. 3	Intg. 4
4th-order single loop	-5	0.4	0.23	0.15	0.13
MASH 2-2	-0.5	0.12	0.11	0.12	0.065
SMASH 2-2 in [2]	-1	0.98	1	0.51	0.8
SMASH 2-2 in [4]	0.5	0.11	0.06	0.12	0.06
SMASH 3-1	**0.5**	**0.1**	**0.06**	**0.18**	**0.06**

4.2 5th-Order Modulators

The performance of the proposed fifth order SMASH modulators (Fig. 4 and 5) have also been compared to traditional cascade 2-2-1 and the proposed SMASH^2 in [7] modulators, by performing the behavioral simulations. All topologies operate with an oversampling ratio of 6, 4-bit internal quantizers and 1-V reference voltage and scaling factor of d = 4. We calculate the optimal coefficients δ and α for SMASH 3-2 from Eq. (10). For $OSR = 6$, $\delta = 0.2$ and $\alpha = 0.1$. For SMASH 4-1, the optimal coefficient δ was calculated by Eq. (14). For $OSR = 6$, $\delta = 0.209$

Figure 9 shows the simulated dynamic range. For this simulation, an opamp dc gain of 50 dB was used for all structures. Figure 8 shows the SNDR degradation against the coefficients mismatch for a -6 dBFS input signal. As shown in Fig. 8 the proposed SMASH 3-2 has a very large immunity to the mismatches although it employs a high order modulator in the first stage and achieves fifth order noise shaping for the second stage quantization noise.

Figure 10 illustrates the SNDR against the first integrator dc gain for the four above-mentioned structures. In this simulation, a -6dBFS input signal was applied. As is seen, the proposed SMASH 4-1 and SMASH 3-2, achieve an SNDR of 90 dB and 94dB, respectively, with opamp dc gain of 30dB.

The overload level and the amplifiers' output swing requirements of the diverse topologies are summarized in Table II.

5. Conclusions

Three novel high order SMASH modulators have been investigated. Simulation results verify the effectiveness and robustness of these structures. We have compared them to the traditional MASH 2-2, 2-2-1 and other SMASH structures and also single-loop structure. Our studies illustrated that the SMASH 3-1, 3-2 and 4-1 are more capable to achieve large SNDRs at low oversampling ratios and have very relaxed output swing and gain demands in the amplifiers. These structures also show large immunity to the coefficients mismatch. Therefore we believe that SMASH with high-order first loop is the best candidate for wideband application in low voltage environments.

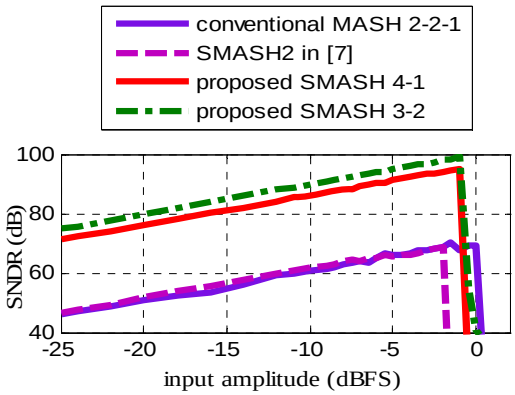

Fig. 9: SNDR against input amplitude.

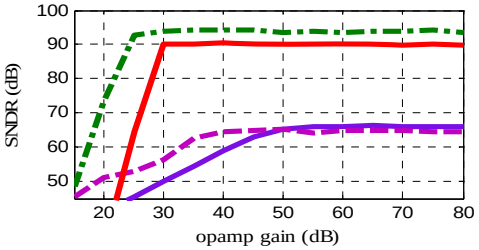

Fig. 10: SNDR against opamp gain.

TABLE II: Overload level and Output Swing Requirements of the 5th-Order Modulator With Various Structures.

Topology	Overload level (dBFS)	Intg 1	Intg 2	Intg 3	Intg 4	Intg 5
MASH 2-2-1	-0.5	0.12	011	0.5	0.25	0.07
SMASH^2 [7]	-2	0.35	0.7	0.55	0.8	1. 2
SMASH 3-2	**-1**	**0.15**	**0.13**	**0.3**	**0.12**	**0.06**
SMASH 4-1	**-1**	**0.2**	**0.1**	**0.06**	**0.36**	**0.07**

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