A linear wideband CMOS LNA for 3-5 GHZ UWB systems

Ali Mirvakili
Department of Electrical Engineering, K.N. Toosi University of Technology, Tehran, Iran
E-mail: amirvakili@ee.kntu.ac.ir

Mohammad Yavari
Department of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran
E-mail: myavari@aut.ac.ir

***Abstract*— A Linear wideband low noise amplifier (LNA) that utilizes distortion canceling is proposed in this paper. It improves the linearity and contemporarily minimizes the effect of 2nd-order interaction. The deteriorating effect of the input matching network on the noise figure is also discussed. The proposed LNA designed in a 0.13*μm* standard RFCMOS technology, targets 3-5 GHZ UWB systems. The 3-dB bandwidth of LNA is 2.88-5.1GHZ. The proposed LNA achieves a power gain of 11dB, better than 10 dB input matching, the minimum noise figure of 1.8 dB, and the input IP3 of +4.4 dBm, while dissipating only 5.2 mW from a single 1.2 V power supply.**

Keywords-UWB LNA; Volterra series; distortion canceling.

I. INTRODUCTION

Recently, the broad application of ultra wide band (UWB) systems has motivated the large group of elites to design unique circuits entailing outstanding traits. According to the FCC, the frequency band of an UWB system is 3.1-10.6 GHZ. Referring to the direct-sequence UWB (DS-UWB) proposal, this 3.1-10.6 GHZ band has divided into two sub bands of 3.1-4.85 GHZ (lower band) and 6.2-9.7 GHZ (upper band). This large bandwidth offers high data rate in the order of several hundred Mbps. Indeed, the intent of UWB is grasping short range and high data rate communications between e.g. two laptops. Inasmuch as the cost and fabrication of CMOS has superior outcomes to other technologies, we have selected CMOS technology for this low noise amplifier (LNA).

LNA, the most prominent part of the receiver's front-end, requires excellent noise performance, high linearity, and low power dissipation. Various topologies for improving the efficiency of LNA have been proposed to work for the lower band of UWB, such as feedback structure [1], differential amplifier [2], [3], on-chip transformer matching [3], [4], and miller effect [5].

The resistive shunt-feedback amplifiers have a desirable wide band matching; however they suffer from poor noise figure (NF) and they are prone to instability. Differential amplifiers show excellent treatment toward second-order harmonics. These LNAs, however, consume extra power likely two times of their single-ended counterparts. Recently, using the band pass filter (BPF) and on-chip transformers in the LNA has offered glorious outputs. Moreover, these techniques provide impeccable wide band matching. The appearance of input matching with band pass filters was proposed in [6] at the favor of UWB LNA. Since then, various architectures utilized this technique and brought new LNAs to the market.

In this paper we have used a valuable technique called distortion canceling for the sake of achieving high linearity. This LNA improves linearity with the best combination of NMOS and PMOS transistors. Adding matching networks in the form of BPF to this structure has created a novel LNA. This paper is organized as follows. In section II, the design trend with noise and linearity analysis of the proposed LNA is briefly introduced and the design equations are discussed. In section III, the simulation results are shown. Finally, the conclusion is presented in section IV.

II. DESIGN OF WIDEBAND AMPLIFIER

A. Input Matching and Gain

Topology of proposed LNA is shows in Fig. 1(a). The input band pass filter is illustrated in Fig. 1(b). It consists of L_{in}, C_{in}, L_1, L_s and C_{eq} in which C_{eq} is the equivalent capacitance seen from the inductor L_1. The equivalent circuit seen from the inductor L_1, is formulated as (1) where g_m is $g_{m1}+g_{m2}$, C_{gs} is $C_{gs1}+C_{gs2}$, $C_{gd}=C_{gd1}+C_{gd2}$, $C_t=C_{gs}+C_p$ and the Z_L is the output load impedance.

$$Y_G = \frac{1}{Z_L + 1/sC_{gd}} + \frac{sC_t}{1+sL_S(g_m+sC_t)} + \frac{g_m}{1+1/sC_{gd}Z_L}\left(\frac{1}{1+sL_S(g_m+sC_t)}\right). \quad (1)$$

It is obvious from (1) that the output impedance, Z_L, and the parasitic capacitor C_{gd}, interposed in the input matching. Moreover, Z_L *and* C_{gd} turned aside this equivalent from that conventional equivalent circuit composed of elements brought in the second term of (1) which is the series RLC circuit of well-known degenerated common source (DCS) amplifier. Inasmuch as the parasitic capacitor C_{gd} can be neglected, this interference to the input matching can be compromised by trivially varying the value of the BPF components. This, however, affects the gain and output matching. In this order, we solved that strict compromise by controlling the size of transistors in a way that these two parts become isolated. Equation (1) with skipping the effect of C_{gd} shows the series combination of L_s, C_{gs}, and the well-known resistor of $L_s/C_{gs}\times g_m$. In this LNA we have used a BPF including these

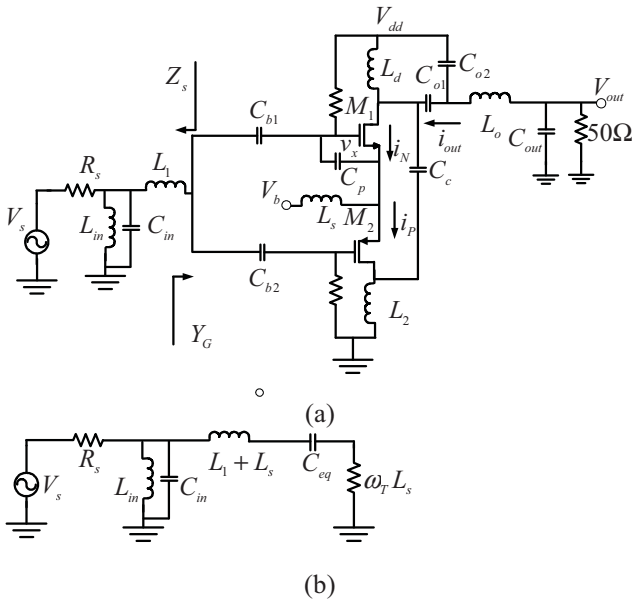

Figure 1. Proposed LN. (a) Schematic of the proposed LNA. (b) Input matching network with Lin=1.41 nH, Cin=1 pF, L1=3.1 nH, Ls=0.5nH, Ceq=0.5 pF.

elements together with L_{in}, C_{in}, and L_1. So it is enough to set $L_s/C_{gs}\times g_m$ equal to 50 ohm. The capacitor C_p is added to achieve extra degree of freedom. It improves the linearity and affects the input matching as well. To analysis the gain of this LNA, we have supposed that the absolute value of the input matching network transfer function is approximately unity in the pass band.

According to the Fig. 1(b), the current passing the equivalent C_{gs} is about $V_s/(2R_s)$ and V_{gs} is calculated as $(V_s/2)/(sR_sC_{gs})$. As a result, the output current is equal to $(g_mV_s/2)/(sR_sC_{gs})$. The gain of this circuit is calculated as (2) where L is equal to $L_d||L_2$, in which we have assumed that the output matching same as the input matching has the absolute value of unity. It is evident from (2) that gain roll-off emanating from the current gain is compensated by L.

$$\frac{V_{out}}{V_s} = \frac{g_m/2}{sR_sC_{gs}} \cdot \frac{sR_L L}{R_L + sL + s^2 R_L LC_{out}} \cdot \tag{2}$$

For output matching, we have used the network of output matching proposed in [5] with a systematic approach. The combination of this network with the L_d and L_s provides the output matching to the 50 ohm load.

B. Noise Analysis

The noise performance of this LNA is related to the losses of the input matching network, which is emanated from poor quality factor Q of the integrated circuits, and the noise of NMOS and PMOS transistors. The small-signal equivalent circuit of the proposed LNA is shown in Fig. 2. The total drain current noise and induced gate noise of this LNA equals to $I_{nd}=I_{nd1}+I_{nd2}$, and $I_{ng}=I_{ng1}+I_{ng2}$ respectively. This figure is identical to that of a conventional DCS LNA. As a result we could use the noise parameters of [6]. These parameters with the previously defined I_{nd} and I_{ng} are still true for the proposed LNA. In other words, the same equations with this assumption

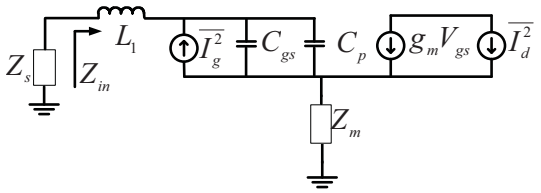

Figure 2. Small-signal equivalent circuit of the proposed LNA.

are valid for the proposed LNA. According to these parameters, it seems that the input referred voltage and current of the proposed LNA are doubled. However, in this design we have set g_{m1}, g_m of NMOS transistor, bigger than that of PMOS to some extent. This is accomplished by controlling sizes and dc currents of both transistors which yield to a NF much smaller than that of two high current transistors. For estimating the effect of non-idealities of the input matching network on the overall noise performance of the LNA, we have modeled those losses as $Z_x=R_x+jX_x$. Having this assumption and following the same procedure as [6], we derived the noise parameters of the proposed LNA with regarding the losses of input network. It is clear that the results of this analysis can be applied to a general DCS amplifier. The correlation impedance and the optimum source impedance of the proposed LNA with the effect of the input network losses are compared in Table I. According to this table, the real part of the correlation impedance of circuit with input network losses not only is zero but also is directly proportional to R_x. Indeed, R_{opt} of such LNA is larger than that of the ideal input network. It offers us to tune the input matching network such that it provides the simultaneous noise and input matching. Moreover, it shows that the losses of the input network could affect the NF and degrade it. Section III gives more information.

According to Fig. 2, Z_{in} is calculated as (3). The condition that allows the simultaneous noise and input matching is $Z_{opt}=Z_{in}^*$. As a result, we must satisfy R_{opt} and X_{opt} as (4).

$$Z_{in} = s(L_s + L_1) + \frac{1}{sC_t} + \frac{g_m L_s}{C_t} \cdot \tag{3}$$

$$R_{opt} = \frac{g_m L_s}{C_t} = \omega_T L_s,\ X_{opt} = -\left(sL_s + \frac{1}{sC_t}\right) \cdot \tag{4}$$

Comparing this formula with those in Table I shows that the simultaneous noise and input matching is provided with this topology. In other words, the value of k in X_{opt} brought in Table I, is around unity, and R_{opt} in this table could be set to $L_s/C_{gs}\times g_m$ [7]. The NF of the proposed LNA is calculated as (5), where $R_c= Re\{Z_c\}$ and Z_c is the correlation impedance brought in Table I. Besides, G_n and R_u are as (6) and (7) respectively where σ is defined in Table I. Moreover, p, α, γ, χ and c are the transistor noise parameters, [6]. It is obvious from these equations that nonlinearities of the input matching network (R_x) degrade the NF.

$$F = 1 + R_u/R_s + (R_s + R_c)^2 . G_n/R_s \cdot \tag{5}$$

$$G_n = \left(\gamma/\alpha^2 g_{do}\right) \cdot \omega^2 C_t^2 \sigma \cdot \tag{6}$$

TABLE I. NOISE PARAMETERS

Noise Parameters of CS circuit [6]	Noise Parameters regarding the losses of input matching network
$i_n = i_{ng} + \frac{j\omega C_t}{g_m} i_{nd}\ ,\ e_n = j\omega L_s i_{ng} + \left(1-\omega^2 C_t L_s\right)\frac{i_{nd}}{g_m}$	$i_n = i_{ng} + \frac{j\omega C_t}{g_m} i_{nd}\ ,\ e_n = Z_x i_{ng} + \left(1+sC_t Z_x\right)\frac{i_{nd}}{g_m}$
$Z_c = sL_s + \frac{1}{s\kappa C_t}, \kappa = \frac{\sigma}{1+\lvert c\rvert p\alpha\chi}, \sigma = 1+2\lvert c\rvert p\alpha\chi + p^2\alpha^2\chi^2$	$Z_c = \left(X_x + \omega L_s - \frac{1+\lvert c\rvert p\alpha\chi}{\omega C_t \sigma}\right)j + R_x\frac{1+p^2\alpha^2\chi^2}{\sigma}$
$R_{opt} = \sqrt{\frac{R_u}{G_n}} = \frac{p\alpha\chi\sqrt{1-\lvert c\rvert^2}}{\omega C_t\sigma}$	$R_{opt} = \sqrt{\frac{R_u}{G_n}+R_c^2} = \sqrt{\frac{p^2\alpha^2\chi^2\left(1-\lvert c\rvert^2\right)}{\omega^2 C_t^2\sigma^2}+R_x^2}$
$X_{opt} = -\left(sL_s + \frac{1}{s\kappa C_t}\right)$	$X_{opt} = -\left(sL_s + jX_x + \frac{1}{s\kappa C_t}\right),\ Z_x = R_x + jX_x + j\omega L_s$

$$R_u = \frac{\gamma}{\alpha^2 g_{do}}\frac{1}{\sigma}\cdot\left(p^2\alpha^2\chi^2\left(1-\lvert c\rvert^2\right)\right) + \frac{\gamma}{\alpha^2 g_{do}}\frac{1}{\sigma}\cdot \left[\omega^2 C_t^2 R_x^2\left(4\lvert c\rvert\alpha p\chi\right)\left(1+\lvert c\rvert\alpha p\chi + p^2\alpha^2\chi^2\right)\right]. \quad (7)$$

C. Linearity Analysis

Achieving high input-referred 3rd-order intercept point (IIP3) in MOSFETs is dependent on large amount of dc-currents and therefore high power consumption. Therefore, the design of low power circuits motivates us to utilize linearization techniques. For this reason we have used the proposed design which provides a good IIP3 together with omission of 2nd-order interaction. The distortion of the LNA is caused by the nonlinear transistor drain current since the output matching is composed of all passive linear elements. Regarding these facts, we have only analyzed the Volterra series of the output current i_{out} in Fig. 1(a). According to this Figure, we have

$$i_N = g_{m1}v_x + \frac{g'_{m1}}{2}v_x^2 + \frac{g''_{m1}}{6}v_x^3 \cdot \quad (8)$$

$$i_P = -g_{m2}v_x + \frac{g'_{m2}}{2}v_x^2 - \frac{g''_{m2}}{6}v_x^3 \cdot \quad (9)$$

Then, the output equivalent current is calculated as (10) where g_2 and g_3 is defined as (11). The term g_2 indicates the reduction of 2nd-order interaction.

$$i_{out} = i_N - i_P = g_m v_x + g_2 v_x^2 + g_3 v_x^3 \cdot \quad (10)$$

$$g_2 = \left(g'_{m1} - g'_{m2}\right)/2, g_3 = \left(g''_{m1} + g''_{m2}\right)/6 \cdot \quad (11)$$

If we ignore the coefficients of order higher than 3, the Volterra series expression of output current, i_{out}, is defined as

$$i_{out} = C_1(s)oV_s + C_2(s_1,s_2)oV_s^2 + C_3(s_1,s_2,s_3)oV_s^3 \cdot \quad (12)$$

TABLE II. DESIGN VALUES OF THE LNA

Transistor size	$(W/L)_1$	$(W/L)_2$	
	80/0.13	64/0.13	
Inductor Value	L_d	L_2	L_o
	7.7nH	3.3nH	3.1nH
Capacitor Value	C_p, C_{o2}, C_{out}	C_c	C_{o1}
	0.2pF	5 pF	0.4 pF

To find the transfer functions of i_{out}, we used the harmonic input and nonlinear current method. After some math calculations we derived IIP3 as (13), where Z_m=sL_s, and also the $\varepsilon(\Delta s,2s)$ and $A_1(s)$ defined as (14) and (15) respectively.

$$IIP3 = \frac{1}{6\,\mathrm{Re}\{Z_s(s)\}}\cdot \frac{g_m}{\lvert A_1(s)\rvert^2\left(1-\frac{g_m Z_m(s)}{A_1(s)}\right)\cdot\left(g_3 - \frac{2}{3}g_2^2\varepsilon(\Delta s,2s)\right)}\cdot \quad (13)$$

$$\varepsilon(\Delta s,2s) = \frac{2Z_m(\Delta s)}{d(\Delta s)+g_m Z_m(\Delta s)} + \frac{Z_m(2s)}{d(2s)+g_m Z_m(2s)}\cdot \quad (14)$$

$$A_1(s) = \frac{1}{d(s)+g_m Z_m(s)},\ d(s) = 1+sC_t(Z_s+Z_m)\cdot \quad (15)$$

If we set $g_m Z_m(s) = A_1(s)$, then we may achieve a high value of IIP3. This forces us to set $Z_s(s)$ as (16).

$$Z_s(s) = -\left[\left(\frac{1}{\omega^2 C_t g_m L_s} + \frac{g_m L_s}{C_t}\right) + \left(\frac{1}{sC_t} + sL_s\right)\right]\cdot \quad (16)$$

The imaginary part of Z_s for distortion canceling is in a good accord to that of the noise cancellation and input matching in (4). However, this is not true for the real part. For increasing the IIP3 in (13) we could minimize $\varepsilon(\Delta s,2s)$ by decreasing $A_1(s)$. As a case in point, it is achieved by increasing the value of L_s. The other way is choosing a topology by which we could equal g_3 to $(2g_2^2\varepsilon(\Delta s,2s)/3)$. One trend is a method called modified DS [8]. This method used the tapped degeneration inductor by which the amplitude and phase of g_3 has changed and set to $(2g_2^2\varepsilon(\Delta s,2s)/3)$.

In this LNA, we have tried to minimize g_2 using the combination of NMOS and PMOS transistors. Since the FET in strong inversion has a negative g_3, therefore with minimizing g_2 which we grasp by setting g_2 as (11), the IIP3 increases to some extent. For high linearity, it is recommended to use

TABLE III. LNA'S PERFORMANCE ON EXTREME CORNER CASES

	S11 dB	S21 dB	S22 dB	NF dB	IIP3 dBm	P_{dc} mW
TT, 27°	<-11	10.8	<-10	1.8-2.5	4.4	5.2
SS, 85°	<-9.8	9.4	<-10.5	2.5-3.5	3	3.25
TT, -40°	<-10	12.3	<-10.2	1.1-2	5.65	8.15

TABLE IV. COMPARISON OF WIDE BAND CMOS LNA PERFORMANCES

Ref.	S11 dB	Gain dB	NF dB	IIP3 dBm	Power mW	FOM	Tech. μm
[1]	<-10	9.5*	3.5	-0.8	16.5	0.36	0.13
[2]	<-9	9.8*	2.3	-7	12.6	0.22	0.18
[3]	<-10.5	16	1.8	-9	7.7	1.27	0.18
[5]	<-11	16.2	2.8	-8.5	6.7	0.97	0.13
This Work^	<-10	11	1.8	+4.4	5.2	13	0.13

*Approximately 6 dB loss due to the buffer. ^Simulation result

transistors with high g_m, and to add a capacitor in parallel to the gate-source of the transistor [9], both of which are evident in (13) and applied to the proposed LNA.

III. SIMULATION RESULTS

The proposed LNA shown in Fig. 1(a) was designed in a 0.13 μm standard RFCMOS technology. Simulations of this LNA were performed with the HSPICE RF tools. Fig. 3 shows the NF of LNA which varies from 1.8 to 2.8 dB. It also shows the NF of the proposed LNA with the ideal input network. It is evident that the losses of the input network degrade the NF. This result is in a good accord to the derived noise parameters of Table I. S_{21}, S_{11}, and S_{22} are depicted in Fig. 4.

Two-tone RF signals that dispersed around 4 GHZ are used to simulate the linearity performance of the LNA. Fig. 5 shows the IIP3, which is +4.4 dBm. The total circuit consumes

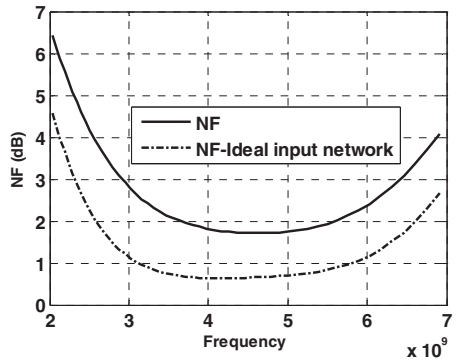

Figure 3. Simulated NF of UWB LNA.

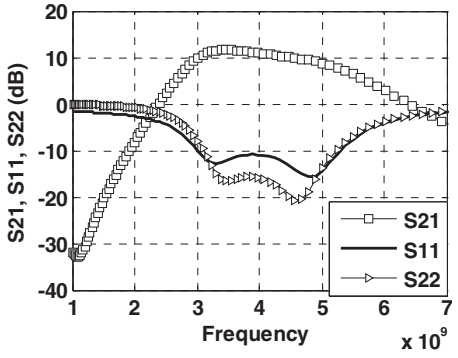

Figure 4. Simulated power gain and input/output return loss of UWB LNA.

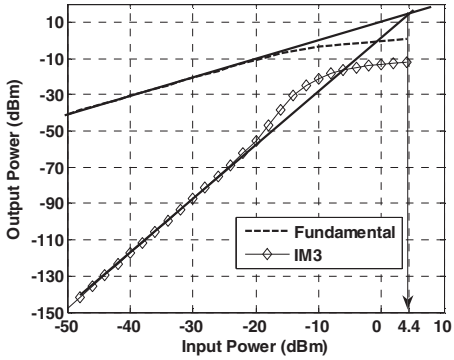

Figure 5. Simulated IIP3 at 4 GHZ.

5.2mW from a 1.2V power supply. Design parameters are illustrated in Table II. The simulation results for extreme corner cases are shown in Table III. To compare the proposed LNA with other previously reported LNAs, we used the Figure of merit, *FOM*, defined as $FOM=OIP3/\{(F-1)P_{dc}\}$, [8]. Table IV shows the comparison results. As is seen the proposed LNA achieves a good *FOM* among other circuits.

IV. CONCLUSIONS

A new topology for LNA, designed in a 0.13 μm standard RFCMOS technology for 3-5 GHZ UWB receivers was reported. The LNA utilizes the combined NMOS and PMOS CS architecture which entails the technique of distortion canceling. Besides, the deterioration of NF due to the input matching circuit was discussed. Simulation results show that the proposed LNA has a minimum NF of 1.8 dB in the whole -3 dB bandwidth of 2.8-5.1 GHZ. It also shows that S_{11} is less than -10 dB, and the S_{21} is 11 dB. The IIP3 of this LNA is +4.4 dBm. The power dissipation of this circuit which has a power supply of 1.2 V is approximately 5.2 mW.

REFERENCES

[1] C.-W. Kim, M.-S. Kang, P. T. Anh, H.-T. Kim and S.-G. Lee, "An ultra-wideband CMOS low noise amplifier for 3–5-GHz UWB system," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 544-547, Feb. 2005.

[2] A. Bevilacqua, C. Sandner, A. Gerosa, and A. Neviani, "A fully integrated differential CMOS LNA for 3–5-GHz ultrawideband wireless receivers," *IEEE Microw. Wireless Comp. Lett*., vol. 16, no. 3, pp. 134-136, Mar. 2006.

[3] Andrea Bevilacqua et al., "A 0.13µm CMOS LNA with integrated balun and notch filter for 3-to-5GHz UWB receivers", in *IEEE Int. Solid-State Circuits Conf.*, Feb. 2007.

[4] D. H. Shin, J. Park, and C. P. Yue, "A low-power, 3–5-GHz CMOS UWB LNA using transformer matching technique," in *IEEE Asian Solid-State Circuits Conf*., Nov. 2007, pp. 95-98.

[5] H.-J. Lee, D. S. Ha, and S. S. Choi, "A 3 to 5GHz CMOS UWB LNA with input matching using miller effect," in *IEEE Int. Solid-State Circuits Conf.*, Feb. 2006, pp 731-740.

[6] A. Bevilacqua and A. M. Niknejad, "An ultrawideband CMOS low-noise amplifier for 3.1–10.6-GHz wireless receivers," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2259-2268, Dec 2004.

[7] T. K. Nguyen, C.-H. Kim, G.-J. Ihm, M.-S. Yang, and S.-G. Lee, "CMOS low-noise amplifier design optimization techniques," *IEEE Trans. Microw. Theory Tech*., vol. 52, no. 5, pp. 1433-1442, May 2004.

[8] V. Aparin and L. E. Larson, "Modified derivative superposition method for linearizing FET low-noise amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 2, pp. 571-581, Feb. 2005.

[9] R. A. Baki, T. K. K. Tsang, M. N. El-Gamal, "Distortion in RF CMOS short-channel low-noise amplifiers," *IEEE Trans. Microw. Theory tech*., vol. 54, no. 1, pp. 46 - 56, Jan. 2006.