A Noise-Canceling CMOS LNA Design for the Upper Band of UWB DS-CDMA Receivers

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***Abstract*— A wide band 5.8-10.6 GHz low-noise amplifier (LNA) employing a common-gate stage for wideband input matching is presented in this paper. This LNA is used to work for the upper band of ultra wide band (UWB) wireless receivers according to the DS-CDMA proposal. The feedback technique is used to achieve a large bandwidth around 4 GHz. Moreover, this topology helps to cancel the noise of the input matching transistor and partially remove the nonlinear distortions as well. Simulated in a 0.13-µm RF CMOS technology, the proposed LNA achieves a power gain of 12.4 dB and the input and output return loss of less than 10 dB. The IIP3 is about -3 dBm and the noise figure (NF) ranges from 2.88-3 dB over the band of interest. The proposed LNA consumes 13.5 mW from a single 1.2-V power supply voltage.**

I. INTRODUCTION

Two competing standards of multi band orthogonal frequency division multiplexing (MB-OFDM) and impulse based direct sequence code division multiple access (DS-CDMA) have been proposed to exploit the large 7.5 GHz bandwidth of ultra wide band (UWB) technology [1]. The MB-OFDM proposal divide the full band of 3.1-10.6 GHz into 14 sub-bands each of them with 528 MHz width while the DS-CDMA proposal divide this full band into two distinct parts of lower band (3.1 GHz- 4.85GHz) and upper band (5.8GHz-10.6GHz). The outstanding feature of this technology which is high date rate communication, inspired multifarious applications mostly related to the communications market needs. Low noise amplifier (LNA), the inevitable component of a wireless receiver is then required to provide adequate gain, wideband input and output matching and low noise figure (NF). Its linearity is also a great concern in broadband RFIC design. Moreover, the battery life limitations forced designers to deliver very low power LNAs. Various UWB LNA topologies like the distributed, feedback [1] and common gate (CG) [2] amplifiers have been reported to meet the aforementioned needs of a desired system. Embedding a bandpass filter (BPF) in the input of LNA for wideband impedance matching that is reported in [3] is another way of UWB implementing. Currently the design trend is toward the noise and distortion canceling [4, 5]. In this paper, we have designed the proposed LNA using the noise canceling trend which is also capable of partially removing the circuit's nonlinear distortions. For input matching, we have used the CG amplifier due to its wideband input matching. Moreover, the feedback technique is used to achieve a wideband behavior with an approximately flat NF response. This paper focuses on the design of an LNA for UWB applications based on the standard RF CMOS technology. The paper is organized as follows. Design concepts of the proposed UWB LNA which are composed of the gain, noise and linearity analysis are discussed in section II. Simulation results and performance summary are demonstrated in section III. Finally, conclusions are given in section IV.

II. PROPOSED WIDE BAND UWB LNA

A. Gain Analysis

The proposed noise-canceling UWB LNA is shown in Fig. 1. The simplified equivalent circuit of this LNA is depicted in Fig. 2. The equivalent impedance was seen from the drain of transistor M_1 called Z_{d1} is calculated as $(R_{L1}+sL_{L1}) \parallel (r_{o1}+R_s(1+g_{m1}r_{o1})) \parallel (R_F+Z_{d3})/(1+g_{m3}Z_{d3})$ where R_s is the source resistance and Z_{d3} is the load impedance of transistor M_3 that is calculated as $sL \parallel r_{o3} \parallel (r_{o2}+R_{L2})$ in which L is the parallel inductance of L_{L2} and L_B. We have also defined Z_{dx} as $sL \parallel r_{o3} \parallel (R_F+Z_{L1})/(1+g_{m3}Z_{L1})$ and Z_{d2} as $(r_{o2}Z_{dx})/(r_{o2}+R_{L2}+Z_{dx})$ where Z_{L1} is calculated as $(R_{L1}+sL_{L1}) \parallel (r_{o1}+R_s(1+g_{m1}r_{o1}))$. The voltage gain of the output buffer, β, is $R_{out}/(R_{out}+1/g_{m4})$, where R_{out} is the 50Ω load resistor. We have also defined R_o as $(R_{out} \parallel 1/g_{m4})$. According to these assumptions, the voltage gain of this circuit is calculated as:

$$A_v = -\frac{1}{2}\left(\begin{array}{l}\beta g_{m2}Z_{d2} + \beta g_{m1}\left(g_{m3} - 1/R_F\right) \\ \cdot\left(R_F \| Z_{d3}\right)Z_{d1} + g_{m1}g_{m5}R_oZ_{d1}\end{array}\right). \qquad (1)$$

For input matching, L_{in} is used to cancel the degrading effect of the gate-source capacitances of transistors M_1 and M_2. In deep sub-micron technologies, due to the low output resistance of the transistor, the input impedance of a CG

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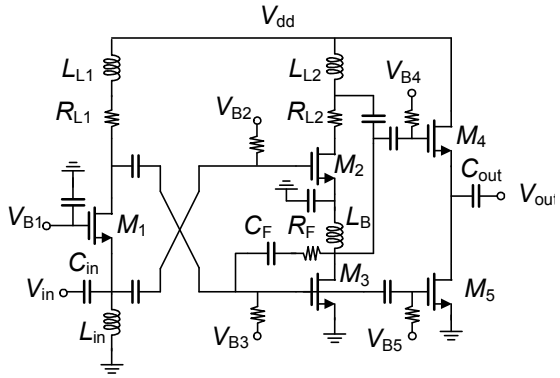

Figure 1: The proposed noise-canceling UWB LNA.

amplifier is deviated from the conventional value of $1/g_m$. This, however, could be useful for isolating the conditions of input matching with noise cancellation by importing one degree of freedom that is the load impedance in satisfying the input matching condition. This formula is brought in (2).

$$R_{in} = \frac{1}{s\left(C_{gs1} + C_{gs2}\right)} \left\| sL_{in} \right\| \frac{Z_{d1} + r_{o1}}{1 + g_{m1} r_{o1}}. \tag{2}$$

For output matching to the 50 Ω load, we have used transistor M_4 as a buffer. In other words, we have set $1/g_{m4}$=50 Ω by controlling its dc current to achieve a broadband output matching.

B. Noise Canceling Trend

We have used the technique of noise-canceling. In this technique the noise of the input transistor after passing from two different paths, i.e. transistor M_2 and M_3 in Fig. 2, is cancelled at the output while the input signal is boosted. In other words, the different sign of induced voltage at the drain and source of the input transistor due to the drain noise current which is supposed to be the dominant transistor M_1's noise is responsible for such an outcome [4, 5]. After calculating and setting zero the output noise, noise cancellation criterion is summarized as (3) in which we have neglected $1/R_F$ due to the high value of feedback resistor in our design. Moreover, we could also neglect its effect on the total NF.

$$\beta R_s g_{m2} Z_{d2} = Z_{d1}\left[g_{m5} R_o + \beta g_{m3}\left(R_F \| Z_{d3}\right)\right] \tag{3}$$

Besides, based on the current-reused topology of this circuit the transconductances of transistors M_2 and M_3 are equal together. For satisfying (3), we have set R_{L1} in the vicinity of R_s, then we have tuned Z_{d2} and Z_{d3} impedances. In addition, the value of R_{L2} is designed much less than r_{o2} which makes the value of Z_{d2} and Z_{d3} comparable. Furthermore, the low value of $R_o g_{m5}$ lets us to disregard it.

Having these assumptions together with exerting previously mentioned noise canceling condition, the NF corresponding to the R_{L1}, transistor M_2 and transistor M_3 is calculated as (4), (5) and (6) respectively. For the sake of simplicity, we have also supposed that R_s=$1/g_{m1}$.

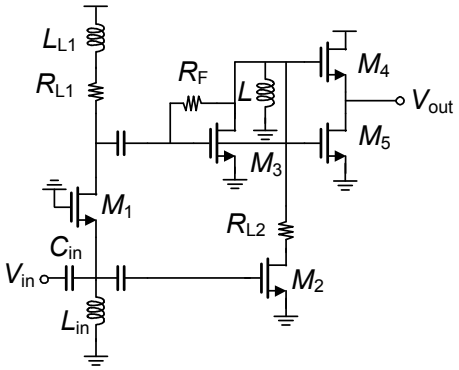

Figure 2: Simplified schematic of the proposed UWB LNA.

$$NF\big|_{R_{L1}} = \frac{4kTR_{L1}}{4kTR_s A_v^2}\left[\begin{matrix}\beta^2 g_{m3}^2 \left(R_F \| Z_{d3}\right)^2 \\ + g_{m5}^2 R_o^2\end{matrix}\right] \cong \frac{R_{L1} R_s}{\left|Z_{d1}\right|^2}. \tag{4}$$

$$NF\big|_{M_2} = \frac{4kTg_{m2}\beta^2 Z_{d2}^2}{4kTR_s A_v^2}\frac{\gamma}{\alpha} = \frac{1}{g_{m2} R_s}\frac{\gamma}{\alpha}. \tag{5}$$

$$NF\big|_{M_3} = \frac{4kTg_{m3}\beta^2 \left(Z_{dx} \| r_{o2} + R_{L2}\right)^2}{4kTR_s A_v^2}\frac{\gamma}{\alpha} = \frac{1}{g_{m3} R_s}\frac{\gamma}{\alpha}. \tag{6}$$

Eventually, the total NF of the proposed LNA is given by:

$$NF = \frac{R_{L1} R_s}{\left|Z_{d1}\right|^2} + \frac{2}{g_{m2} R_s}\frac{\gamma}{\alpha}. \tag{7}$$

C. Distortion Analysis

Linearity of a circuit is determined by a factor called 3rd-order intercept point (IP3) and used as the input IP3 (IIP3) or the output IP3 (OIP3). For calculating the IIP3 of this LNA we have used the guidelines from [5, 6]. First, we have considered the CG input stage which brought individually in Fig. 3. In this circuit, C_1 and C_2 are modeled as the total capacitances of drain and source of transistor M_1 respectively.

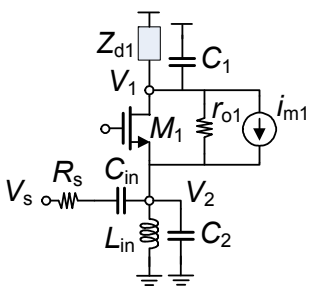

Figure 3: The equivalent input stage of UWB LNA for linearity analysis.

We have assumed that the major source of nonlinearity in this figure is emanated from the current of transistor M_1 brought in equation (8).

$$i_{m1} = g_{m1}(-V_2) + \frac{g'_{m1}}{2}V_2^2 - \frac{g''_{m1}}{6}V_2^3. \quad (8)$$

Then, by solving KCL equations in drain and source nodes of transistor M_1 using the harmonic input and nonlinear current methods, we have computed the nonlinear transfer functions of V_1 and V_2 voltages which their Volterra series are defined as (9) and (10), respectively

$$V_1 = A_1(s)oV_s + A_2(s_1, s_2)oV_s^2 + A_3(s_1, s_2, s_3)oV_s^3. \quad (9)$$

$$V_2 = B_1(s)oV_s + B_2(s_1, s_2)oV_s^2 + B_3(s_1, s_2, s_3)oV_s^3. \quad (10)$$

The output voltage of this LNA can be expressed as the following Volterra series, where V_s is the excitation voltage.

$$V_{out} = C_1(s)oV_s + C_2(s_1, s_2)oV_s^2 + C_3(s_1, s_2, s_3)oV_s^3. \quad (11)$$

For a two tone excitation $V_s = A\{cos(\omega_a t) + \cos(\omega_b t)\}$, the IIP3 is defined as (12), [6].

$$IIP_3(2\omega_b - \omega_a) = \frac{1}{6\,\mathrm{Re}(Z_s(s))}\left|\frac{C_1(s_a)}{C_3(s_b, s_b, -s_a)}\right|. \quad (12)$$

According to [6] $s_1 = s_2 = s_b$ and $s_3 = -s_a$ in that $s_a \sim s_b \sim s$ which results in $Z_{d3}(s_1+s_2+s_3) \sim Z_{d3}(s)$. Based on these facts, the fundamental term and the third order nonlinearity of the output voltage are calculated as follows:

$$C_1(s) = (\beta Z_{d3} g_{m3} + R_o g_{m5})(A_1 o V_s) + \beta Z_{d2} g_{m2}(B_1 o V_s). \quad (13)$$

$$C_{3-Part1}(s) = (\beta Z_{d3} g_{m3} + R_o g_{m5})(A_3 o V_s^3) + \beta Z_{d2} g_{m2}(B_3 o V_s^3). \quad (14)$$

$$C_{3-Part2}(s) = (\beta Z_{d3} g'_{m3} + R_o g'_{m5})(\overline{A_1 A_2}) + \beta Z_{d2} g'_{m2}(\overline{B_1 B_2}). \quad (15)$$

$$C_{3-Part3}(s) = \frac{1}{6}\left[\begin{matrix}(\beta Z_{d3} g''_{m3} + R_o g''_{m5})(A_1 o V_s)^3 \\ + \beta Z_{d2} g''_{m2}(B_1 o V_s)^3\end{matrix}\right]. \quad (16)$$

According to the IIP3 formula, a good linearity demands a low value of third order nonlinearity, C_3. In this design we could omit the first part of this term which brought in (14). The derived equation for the ratio of B_3/A_3 after some math calculations is approximated as $(-R_s/Z_{d1})$. Consequently, the condition for neutralizing (14) is summarized as (17) that is exactly the condition for noise cancellation of the input transistor.

$$\frac{\beta g_{m3}(R_F \| Z_{d3}) + g_{m5} R_o}{\beta g_{m2} Z_{d2}} = \frac{R_s}{Z_{d1}}. \quad (17)$$

We have also cancelled some components of (15) which brought in (18) in view of the fact that the value of $B_2(-s_a, s_b)$ which is proportional to $(sL_{in} \| 1/sC_2)$ is zero.

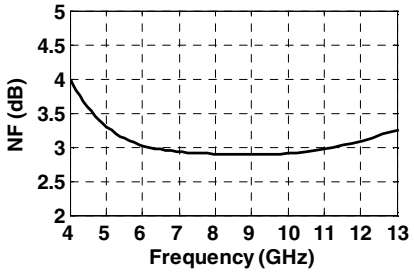

Figure 4: Simulated NF of UWB LNA.

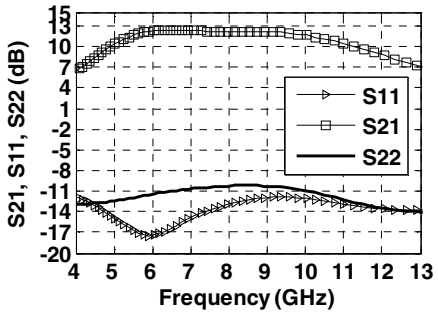

Figure 5: Simulated power gain and input/output return loss of UWB LNA.

$$\overline{B_1 B_2} = \frac{1}{3}\left[B_1(-s_a)B_2(s_b, s_b) + 2B_1(s_b)B_2(-s_a, s_b)\right] \quad (18)$$

One way to achieve a good linearity is placing a weak inversion (WI) biased transistor in the output by which the (16) term cancels [5, 6].

III. Simulation Results

The proposed LNA shown in Fig. 1 is designed in a 0.13μm standard RFCMOS technology. The simulation of this LNA is performed with the HSPICE RF tools. Fig. 4 shows the NF of LNA which varies from 2.88 to 3 dB in the whole band. Fig. 5 indicates that the input and output return loss is less than 10 dB, and the power gain is 12.4 dB. Table I shows the design values of the proposed LNA. Simulation results of different corner cases are summarized in Table II. Two-tone RF signals that dispersed around 8 GHz are used to simulate

TABLE I. Design Values of the Proposed LNA

Transistor size	$(W/L)_1$	$(W/L)_2$	$(W/L)_3$	$(W/L)_4$	$(W/L)_5$
	39/0.13	30/0.13	26/0.13	39/0.13	36/0.13
Inductor Value	L_{in}	L_{L1}	L_{L2}	L_B	
	2.5 nH	4.5 nH	1.7 nH	3.6nH	
Resistor Value	R_{L1}		R_{L2}	R_F	
	65 Ω		50 Ω	2.5 kΩ	

TABLE II. LNA's Performance on Extreme Corner Cases.

Corner Case Degree	S_{11} (dB)	S_{21} (dB)	S_{22} (dB)	NF (dB)	Pdc (mW)	IP3 (dBm)
FF, -40	<-9.5	15	<-8	1.8-2	16.5	-3.2
TT, 27	<-11.9	12.4	<-10.2	2.88-3	13.5	-3
SS, 85	<-13.6	9.6	<-12.6	4.2-4.4	11.5	-2.5

TABLE III. COMPARISON OF VARIOUS LNAS WITH THE PROPOSED UWB LNA

Ref.	3dB B.W. GHZ	S_{11} dB	Power mW	Gain dB	NF dB	IIP3 dBm	FOM	Technology Year
[1]	3.1-10.6	<-9.9	9	15.1±1.4	2.5±0.43	-5.1	2.6223	0.13 µm 2007
[2]	0.4-10	<-10	12	12.4	4.4-6.5	-6	0.2074	0.18 µm 2007
[4]	1.2-11.9	<-11	20	9.7-7.5	4.5-5.1	-6.2	0.0616	0.18 µm 2007
[7]	2-9.6	<-8.3	19	11	3.6-4.8	-7.2*	0.0978	0.13 µm 2007
[8]	1.3-12.1	<-17.5	10.68	7.92±0.23	2.5-4.56	-4*	0.3128	0.18 µm 2008
[9] +	4.7-10.5	<-9	7.2	12	3.9-5.6	-12	0.0955	0.18 µm 2006
[10]	7.2-9.1	<-9	16	10	3.9-4.7	2	0.6809	0.18 µm 2007
This Work+	4.7-11.7	<-11.9	13.5	12.4	2.88-3	-3	0.6857	0.13 µm

*At 6GHZ, , + Simulation Results

the linearity performance of this LNA. Fig. 6 shows the simulated IIP3, which is around -3 dBm. Fig. 7 shows the role of feedback path in widening the frequency spectrum of our design. The whole circuit consumes 13.5 mW from a 1.2 V power supply. To compare the proposed LNA with other reported LNAs, we have used the figure of merit, *FOM*, defined as *FOM*=*OIP*3/{(*F*-1).*Pdc*}, where *OIP3* is the output 3rd-order intercept point, *OIP3*=Power gain. *IP3*, *F* is the noise factor, and *Pdc* is the dc power consumption [6]. This result is compared in Table III.

IV. CONCLUSIONS

A noise-canceling LNA has been proposed in a 0.13µm standard RFCMOS technology. The CG input stage is used with the favor of attaining a good input matching without deteriorating the NF of the circuit. The derived Volterra series expressions proved that this noise-canceling LNA is also capable of partially canceling the nonlinear distortions. Moreover, the combination of the feedback and current-reused techniques has produced the wide bandwidth together with approximately flat NF response. The simulation results show that this LNA has a minimum NF of 2.88 dB in the whole band with only 0.12 dB variation. It also shows that the S_{11} is less than 10 dB and the IIP3 of this LNA is about -3 dBm. It achieved an approximately smooth power gain of 12.4 dB in the upper band of 5.8-10.6 GHz. The power dissipation of this circuit which has a power supply of 1.2 V is approximately 13.5 mW.

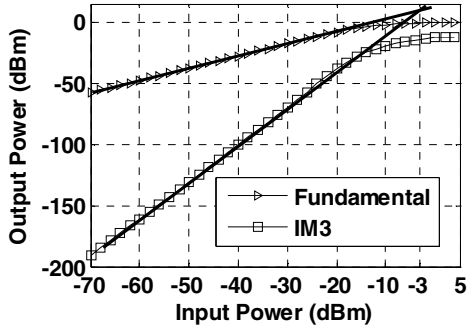

Figure 6: Simulated IIP3 at 8 GHz.

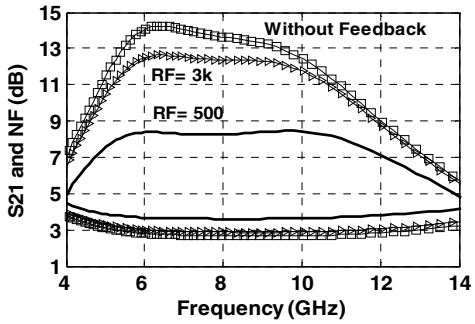

Figure 7: Simulated S_{21} and NF with different feedback values.

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