A Low Power UWB Very Low Noise Amplifier Using An Improved Noise Reduction Technique

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***Abstract*— A single-ended ultra wideband (UWB) low noise amplifier (LNA) employing an improved noise reduction (INR) technique is presented. The INR consists of three main components encompassing active positive feedback, input matching extender and transformer. The input matching extender helps to preserve the input return loss (S11) less than -10 dB over entire bandwidth from 2 to 7.6 GHz. Using active positive feedback and transformer reduces the noise figure (NF) significantly. Moreover, compare to the version with no transformer and with the same gain, with the aim of transformer power consumption is reduced to about half. Simulated in a 0.13-µm RF CMOS technology, the proposed LNA achieves a power gain of 13.8 dB with only 0.7 dB variation and the NF is between 1.85-2.1 dB over whole bandwidth while consumes only 2.15 mW dc power from a 1.1 V supply voltage.**

I. INTRODUCTION

Demand for high data transferring rate wireless multi propose receivers with consideration of die aria and power consumption resulted in ultra wideband (UWB) technology [1]. One key challenge in UWB receiver design is to provide an appropriate input matching over entire bandwidth (BW) for low noise amplifier (LNA) as the first block. In this regard common gate (CG) structure due to its simplicity, robustness and high linearity is the most admired technique [2]. Nevertheless, the CG input matching structure is not perfect and suffers from poor noise performance. This deficiency is owing to the limited g_m of CG transistor to 20 mA/V. A popular method for reducing the noise figure (NF) is the noise canceling structure which eliminates the channel thermal noise of the CG transistor by using an additional common source (CS) transistor [3]. Nevertheless, this several branches structure consumes considerable dc power. Furthermore, the common source (CS) transistor degrades the linearity. Therefore, in applications with high linearity requirements some distortion cancellation methods must be applied [4], [5]. Another approach is to reduce the contribution of CG thermal channel noise with increasing its transconductance. But due to input matching consideration it seems to be impossible. Indeed, there is a state of the art technique to overcome this tradeoff, which is based on positive feedback [6], [7]. The proposed structure in [6] is differential so needs additional component before LNA. Moreover it is designed for narrow band applications. In contrast [7] is single-ended and adapted for UWB applications. With the aim of this technique it is possible to increase the transconductance of the CG transistor to any arbitrary value without input matching degradation. As a result of this degree of freedom, the thermal channel noise of the CG transistor reduces considerably. Besides, due to the gain enhancement the noise contribution of the later stages are reduced. But, the implemented technique in [7] suffers from large parasitic capacitance and high dc current of the CG transistor.

In this paper a single-ended, low power, ultra wideband very low noise amplifier is introduced which uses an improved noise reduction (INR) technique. With the aim of INR the power consumption and NF, simultaneously, are significantly lower than that of state of the art designs. Section II describes the components of INR technique encompassing active positive feedback, input matching extender and transformer. Section III introduces the proposed LNA. Simulation results and conclusions are presented in Sects. IV and V, respectively.

II. IMPROVED NOISE REDUCTION TECHNIQUE

A. Active Positive Feedback

This idea is based on increasing the input impedance by using positive feedback. Figure 1(a) illustrates the conceptual idea. The expression for input impedance can be written as $Z_{in}=Z_{inA} / (1 - G_{loop})$ [6] where Z_{in} and Z_{inA} are the closed loop and open loop input impedances, respectively. $G_{loop} = AB$ must be positive and presents the loop gain, where A and B are the feedforward and feedback paths gain, respectively. Both feedforward and feedback paths are designed by transistor as shown in Fig. 1(b) [7]. In Fig. 1(b), $A = g_{m1}Z_1$, $B = (R_S||g_{m1}^{-1}) / (R_S||g_{m1}^{-1}+g_{m2}^{-1})$ and $Z_{inA} = g_{m1}^{-1}$. Input impedance is given by [7]

$$Z_{in} = \frac{1}{g_{m1} - g_{m2}(g_{m1}Z_1 - 1)} \qquad (1)$$

According to (1) with adjusting g_{m2} and Z_1, g_{m1} can be increased to any arbitrary value with out any changes in Z_{in}.

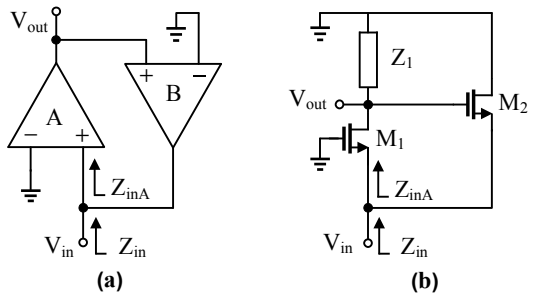

Figure 1: (a) Conceptual idea of increasing input impedance by using positive feedback, and (b) design by transistor (bias circuits are not shown).

This increment in g_{m1} reduces the contribution of M_1's channel thermal noise. If the input impedance be matched to the source, the noise factor (F) is given by [7]

$$F = 1 + \frac{\gamma}{\alpha}\frac{1}{g_{m1}R_S} + \frac{4R_1}{R_S g_{m1}^2 |Z_1|^2} + \frac{\gamma}{\alpha} g_{m2} R_S \qquad (2)$$

where γ and α are the process dependent parameters, R_1 is the resistance part of Z_1 and R_S is the source resistance. The second and third terms represent the thermal noise of M_1 and Z_1, respectively. The last term shows the thermal noise contribution of M_2 and it is negligible due to M_2's small size [7] and lower transconductance. Equation (2) shows that by increasing g_{m1} the noise factor is reduced.

B. *Input Matching Extender*

Equation (1) shows that the input impedance is a function of frequency. At first it may be seem that by obtaining constant output impedance, e.g. with a bandwidth extension technique, the input impedance will remain constant. To examine this theory Z_1 in (1) is replaced by $R_1(\omega) + jI_1(\omega)$ where R_1 and I_1 are the real and imaginary parts of Z_1, respectively. As the sake of input matching, $|Z_{in}|$ must be equal to the source resistance. This parameter is extracted from (1) as:

$$|Z_{in}| = \frac{1}{\sqrt{(g_{m1} + g_{m2} - g_{m1}g_{m2}R_1(\omega))^2 + (g_{m1}g_{m2}I_1(\omega))^2}} \qquad (3)$$

In bandwidth extension techniques a constant $|Z_1|$ is desirable which is equal to a constant $(R_1^2(\omega) + I_1^2(\omega))^{1/2}$. In general bandwidth extension techniques the variations of $R_1(\omega)$ and $I_1(\omega)$ are in reverse directions over the bandwidth. Therefore, these variations cancel each other and a constant $|Z_1|$ will be obtained. But, the relation (3) shows that for a constant $|Z_{in}|$, $R_1(\omega)$ and $I_1(\omega)$ must rise or fall, simultaneously, which will degrade the $|Z_1|$ and consequently the voltage gain. So, both the real and imaginary parts must be constant and a usual bandwidth extension technique is not proper in this case. On the other hand, preserving both $R_1(\omega)$ and $I_1(\omega)$ constant over a bandwidth of several GHz, even if to be possible, undoubtedly needs a very high order filter with several inductors resulting in a huge die area.

The INR method focuses on feedback path instead of Z_1. As Fig. 2(a) illustrates an impedance network (Z_2) is added to M_2's drain so that follows the same pattern as Z_1. Z_2 with considering M_2's output resistance (r_{o2}), modifies the loop gain as:

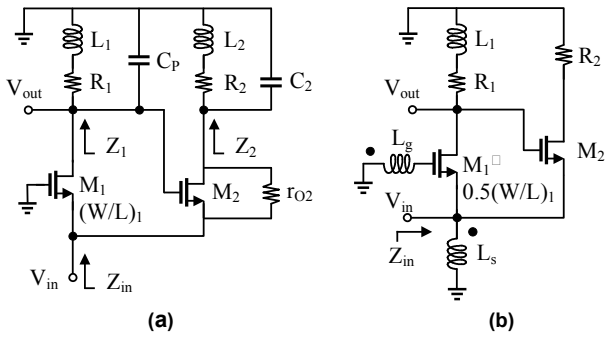

Figure 2: (a) Input matching extender, and (b) complete INR (bias circuits in both *a*, *b* are not shown for simplicity).

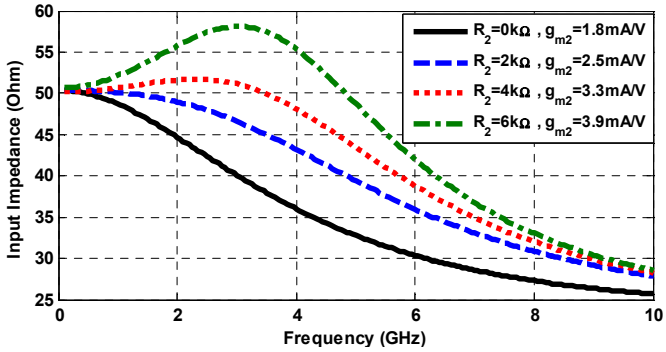

Figure 3: $|Z_{in}|$ with different R_2 and g_{m2} at g_{m1} = 40 mA/V, R_1 = 300 Ω, L_1 = 3 nH, L_2 = 0, C_P = 100 fF, C_2 = 5fF, r_{o2} = 3 KΩ.

$$G_{loop} \approx g_{m1}g_{m2}r_{o2}\left(\frac{1}{g_{m1}} \| R_S\right)\frac{Z_1}{r_{o2} + Z_2} \qquad (4)$$

where r_{o2} is the drain-source resistance of M_2, $Z_1 = (R_1 + j\omega L_1) \| 1/j\omega C_P$ and $Z_2 = (R_2 + j\omega L_2) \| 1/j\omega C_2$. Equation (4) shows that if Z_2 to be comparable to r_{o2} and varies with frequency like Z_1, then G_{loop} almost remains constant. As mentioned Z_2 must be comparable to r_{o2}, therefore R_2 can sized up to several kilo ohms. In this condition an effective L_2 must be very large. So, due to the die area, in final design it is not used. Another design consideration is about C_2. Since R_2 is very larger than R_1, for the sake of same time constant C_2 must be very smaller than C_P. As a rule of thumb C_2/C_P must be 0.8 of R_1/R_2. This relation is obtained by several simulations. A key point here is that C_P is the sum of parasitic capacitances at M_1's drain encompassing M_1's drain-source, M_1's drain-gate, M_2's gate source and buffer's capacitances (not shown in Fig. 2(a)). C_2 can be implemented by M_2's parasitic capacitance. Figure 3 demonstrates Z_{in} for different values of R_2 and g_{m2} at g_{m1} = 40 mA/V, R_1 = 300 Ω, L_1 = 3 nH, L_2 = 0, C_P = 100 fF, C_2 = 5 fF and r_{o2} = 3 kΩ. As it shows and was expected, increasing R_2 results in better input matching extension. Of course R_2 is limited by two main design considerations. The first one is related to C_2 which can not be smaller than M_2's drain parasitic capacitance. The second one is according to the headroom voltage which limits the dropped dc voltage over R_2. Finally as shown in Fig. 3 it is worth mentioning that for the sake of good input matching at lower frequencies, the value of g_{m2} should be enhanced as R_2 is increased.

C. Transformer

As it was mentioned the implemented technique in [7] has two unfavorable side effects. The first one is large parasitic capacitances due to large M_1's gate area which degrade the performance at high frequencies. So the proposed structure in [7] is proper for lower band of UWB technology. The second negative effect of high transconductance is high dc current of the CG transistor, which drops a significant dc voltage on the output resistance. Therefore, the aforementioned circuit is inutile in low voltage applications. In INR scheme, as shown in Fig. 2(b), a transformer is used which duplicates the small signal voltage over the gate-source of M_1. So this transformer boosts the transconductance of the LNA. Consequently the performance of an LNA including 1:1 transformer and M_1 with 0.5(W/L) is similar to an LNA that using M_1 with (W/L), where W and L are the channel width and length, respectively. This improvement results in reducing M_1's dc current without lowering the gain. As a result, with the aim of transformer it is possible to decrease the voltage supply and dc current without any degradation in gain and NF at the cost of the increased chip area.

III. Proposed Low Power Very Low Noise Amplifier

Figure 4 shows the final scheme of the proposed single-ended low-power UWB very low noise amplifier. A cascode CG structure including M_1 and M_2 is used as the feedforward path. This cascode structure results in better input-output isolation. The feedback path is designed by M_3. As mentioned in the previous section, R_{D3} is added as the sake of input matching extension. The inductor L_C and the parasitic capacitances at drain of M_1 and source of M_2 form a π network. Proper choice of L_C partially cancels the effect of the parasitic capacitances. Under this condition, the nonlinearity and noise of M_2 can be neglected [2]. Moreover, it prevents from the voltage gain reduction at high frequencies. Therefore, the noise contribution of R_{D1} and buffer becomes negligible. The input impedance expression is given by:

$$Z_{in} = \frac{r_{o3} + Z_{D3}}{g_{m1}(1+k)(r_{o3} + Z_{D3}) + g_{m3} r_{o3}[1 - g_{m1}(1+k) Z_{D2}]} \quad (5)$$

where k is the magnetic coupling factor, r_{o3} is M_3's the drain-source resistance, $Z_{D2} = (R_{D2}+j\omega L_{D2}) \,||\, 1/j\omega C_{P2}$ *and* $Z_{D3} = R_{D3} \,||\, 1/j\omega C_{P3}$. Here $C_{P2} = C_{gs4} + C_{dg2} + C_{ds2} + C_{gd3}(1 + g_{m3}|Z_{D3}|) + C_{gs3}$ and $C_{P3} = C_{ds3} + C_{dg3}$. The voltage gain and noise factor can be formulated as:

$$A_v = \frac{|Z_{in}|}{|Z_{in}| + R_S}(1+k) g_{m1} |Z_{D2}| \quad (6)$$

$$F = 1 + \frac{1}{4}\frac{\gamma}{\alpha}\left(\frac{1 - g_{m3}R_s}{1 + R_S/Z_{in}}\right)^2 \frac{1}{(1+k)^2 g_{m1} R_S} + \frac{4R_{D2}}{R_S(1+k)^2 g_{m1}^2 |Z_{D2}|^2} + \frac{\gamma}{\alpha} g_{m3} R_S \quad (7)$$

In relation (7), the second and third terms represent the thermal noise of M_1 and R_{D2}, respectively. The last term shows the thermal noise contribution of M_3. If the circuit to be matched to the source ($|Z_{in}|=R_S$) and because $g_{m3}R_S << 1$, (6) and (7) are simplified to:

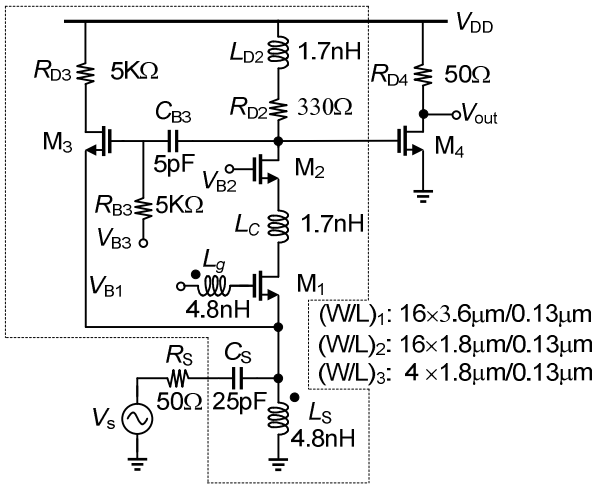

Figure 4: Complete LNA schematic; within the dashed box is the core.

$$A_v = 0.5(1+k) g_{m1} |Z_{D2}| \quad (8)$$

$$F = 1 + \frac{\gamma}{\alpha}\frac{1}{(1+k)^2 g_{m1} R_S} + \frac{4R_{D2}}{R_S(1+k)^2 g_{m1}^2 |Z_{D2}|^2} + \frac{\gamma}{\alpha} g_{m3} R_S \quad (9)$$

Without transformer and input matching extender ($k = 0$, $Z_{D3} = 0$), the relations (8) and (9) will turn into (1) and (2), respectively.

IV. Simulation Results

The circuit level simulations were performed with Spectre RF using a 0.13 μm standard RF-CMOS technology. Figure 5 demonstrates the input matching before using the positive feedback, after using the feedback and after using the input matching extender. It shows that with the aim of input matching extender, the frequency range with S11<-10 dB has a 52% increase. The power gain and noise figure are depicted in Fig. 6. With the aim of L_C and cascode structure a flat 13.8 dB gain with only 0.7 dB variation over entire BW is obtained. Moreover, as Fig. 6 illustrates, the inductor L_C by cancelling the parasitic capacitances and power gain compensation prevents from the NF rising at high frequencies. Therefore the proposed LNA achieves a state of the art 1.85-2.1 dB NF over 2.5-10 GHz. To examine linearity a two tone test with 100 MHz spacing at 5.2 GHz is performed and as Fig. 7 exhibits, the proposed LNA achieves -15.2 dBm IIP3, which can be improved by some distortion cancellation methods [4], [5]. The performance results of the simulated LNA and a few prior published state-of-the-art wideband LNAs are summarized in Table I. As is seen, the proposed LNA achieves better NF with much less power consumption than the previously reported best noise figures in [5], [7] and [9]. This superior performance shows the high efficiency of the proposed INR technique. To compare the proposed LNA with different topologies, a figure of merit (FOM) defined in [2] is utilized in Table I

$$FoM = \frac{Gain_{average}[abs] \times BW[GHz]}{(F_{average} - 1) \times P_{dc}[mW]} \quad (10)$$

TABLE I. PERFORMANCE COMPARISION.

Ref.	CMOS Process	BW (GHz)	S11 (dB)	S21** (dB)	NF (dB)	IIP3 (dBm)	V_{DD} (V)	Core Power (mW)	FOM
This Work*	0.13 µm	2-7.6	< -10	13.1-13.8	1.85-2.1	-15.2	1.1	2.15	105.1
[2]	0.13 µm	1.5-8.1	< -9	8.6-11.7	3.6-6	11.7-14.1	1.3	2.62	12.9
[3]	0.18 µm	1.2-11.9	< -11	6.7-9.7	4.5-5.1	-6.2	1.8	20	1.9
[4]	65 nm	0.2-5.2	< -14	7-9.6	2.9-3.5	> 0	1.2	14	2.3
[5]	0.13 µm	0.8-2.1	< -8.5	8.5-11.5	2.6	16	1.5	17.4	1
[7]*	0.18 µm	2-6.5	< -10	8-11	2.5-2.7	3.4	1.8	7.6	6.9
[8]	90 nm	3.1-13.9	< -10	7.8-12.3	2.7-3.3	-6.4	1.0	2.5	49.7
[9]	0.13 µm	0.2-3.8	< -9	10-13	2.8-3.4	-4.2	1	5.7	9

*Simulation results ** All results are with output matching.

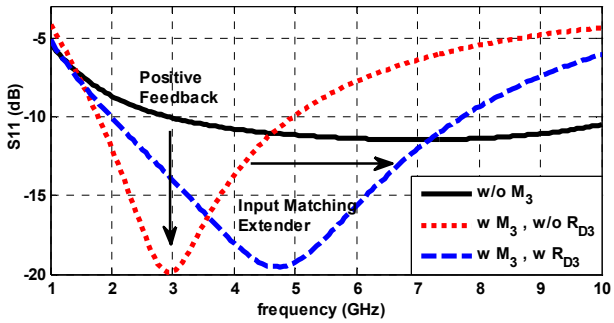

Figure 5: Input matching before and after INR.

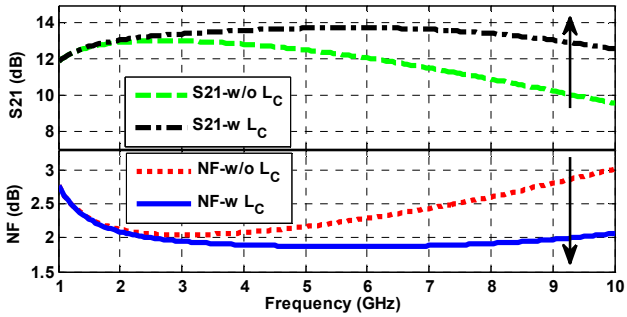

Figure 6: Power gain and noise fiqure.

where $Gain_{average}$ is the average power gain, $F_{average}$ is the average noise factor over the frequency range and P_{dc} is the power consumption of the LNA core. From Table I our proposed LNA exhibits much better FoM compared to the other reported state-of-the-art wideband LNAs.

V. CONCLUSION

In this paper a noise reduction technique for UWB LNAs is presented which is called the improved noise reduction (INR) technique. A single-ended UWB LNA is designed, which with the aim of INR achieves very low noise figure while consumes very low dc power. The proposed UWB LNA was designed and simulated in a 0.13 µm RF-CMOS technology. Comparison with the prior published state-of-the-art noise canceling wideband LNAs, the proposed LNA achieves excellent NF with much less power consumption.

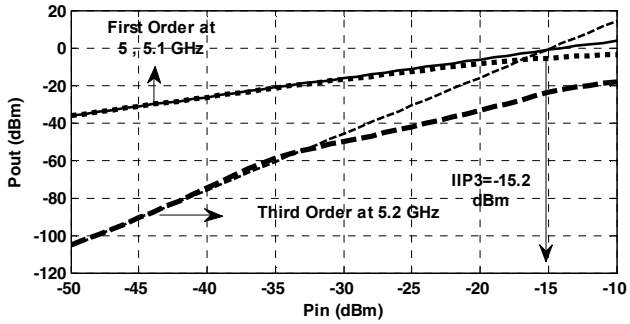

Figure 7: Simulated IIP3 at 5.2 GHz.

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