A Noise Reduction Technique for Wideband LNAs in Low-Power Digital TV applications

Mohammad Sadegh Mehrjoo, Amirhossein Ansari Bozorg, and Mohammad Yavari
Integrated Circuits Design Laboratory, Department of Electrical Engineering, Amirkabir University of Technology
Tehran, Iran
E-mail: a.h.ansari@aut.ac.ir, myavari@aut.ac.ir

***Abstract**: A low power ultra wideband very low noise amplifier is presented. The proposed LNA scheme uses two parallel nMOS and pMOS cascode common gate (CG) branches, an active positive feedback and input matching extender. Compared to the CG structure, the proposed LNA results in improved noise figure and input matching over a wide bandwidth with the same power consumption. Circuit level analysis and simulation results are provided to verify the effectiveness of the proposed LNA scheme. Simulated in a 0.18μm RF CMOS technology, the proposed LNA achieves a noise figure of 2.2 to 2.5 dB and input return loss (S_{11}) less than -10 dB over whole bandwidth while consumes only 2.7 mW power from a 1.8 V power supply. The -3 dB power gain (S_{21}) is 19.7 dB and maximum values of IIP3 and IIP2 are -6 dBm and 15 dBm, respectively.*

1. Introduction

Very low noise figure (NF) RF front-end receivers are highly demanded in terrestrial digital video broadcasting [1]. The low noise amplifier (LNA), as the first block of a receiver, plays the most important role in the overall NF. The common gate (CG) structure is the most admirable wideband LNA scheme since it achieves good wideband input matching [2]. Figure 1 illustrates the ordinary cascode CG LNA. The noise factor of this LNA is given by $F=1+(\gamma/\alpha)\times(1/g_{m1}R_S)+4/g_{m1}R_D$ [2], where γ and α are the process dependent parameters and g_{m1} is the M_1's transconductance. This equation shows that enhancing g_{m1} results in decreasing the noise factor. But, increasing g_{m1} is impossible because it degrades the input matching and needs more bias current resulting in more voltage drop on R_D. Therefore, the noise canceling technique has been applied to the CG structure to reduce the overall noise factor [3]. However, this technique owing to its multi branches structure suffers from high power consumption.

Another scheme to improve the noise performance in CG structure is to utilize the positive feedback network [4]. Nonetheless, this structure needs a differential input signal which imposes a differential antenna or balun and hence suffers from the input signal loss, input signal amplitude and phase error, and high power consumption. Moreover, the proposed LNA in [4] is narrowband and uses the positive feedback to implement a sharp filter. In this paper, a new low power LNA is presented which considerably improves the noise and gain performance of CG structure with the same power consumption. The proposed technique can be used in both single-ended and differential LNAs as well. Section II describes the concepts of the proposed wideband LNA which are composed of the gain, noise, input matching and linearity. Section III describes the simulation results and performance summary. Finally, conclusions are presented in Sect. IV.

2. Circuit Analysis and Design

The proposed LNA is shown in Fig. 2. The main path is designed by two parallel pMOS and nMOS cascode CG branches, $M_{N1,2}$ and $M_{P1,2}$ in order to reduce the channel noise of CG transistor with low power dissipation and also improve the IIP3. The value of R_{LOUD} is selected large in order to have high power gain, S_{21}, and also reduce its thermal noise. Source inductors are used to cancel the degrading effect of the parasitic capacitances of transistors $M_{N1,2}$ and $M_{P1,2}$. Moreover, their value is considered very large to have input matching in low frequencies so they are off-chip components. To compensate the input impedance, a positive feedback network comprising of M_F is employed [5]. In addition, the transistor M_B as a buffer is used at the output. Finally, a common mode feedback is used for precluding the variation of output voltage.

2.1 DC Analysis

In this structure, the bias voltages are made by simple current sources. Moreover, source inductors are applied in order to provide DC path for the bias current. Since in practice the bias currents of pMOS and nMOS branches may not be equal so it causes the output voltage has a significant variation. This means that the transistors may work in the linear region. So, a common-mode feedback circuit is utilized to define the drain dc voltage of transistors M_{N2} and M_{p2}. This circuit realized by transistors M_{F1}-M_{F5} shown in Fig. 2.

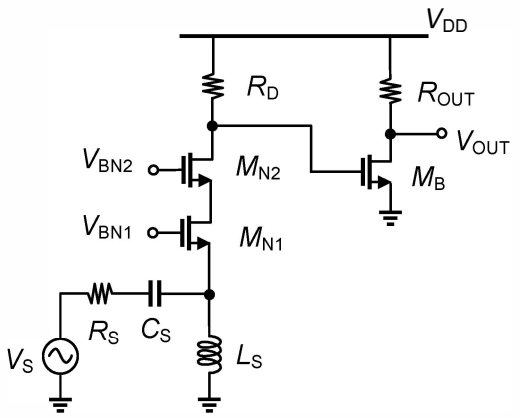

Fig. 1: Cascode CG LNA.

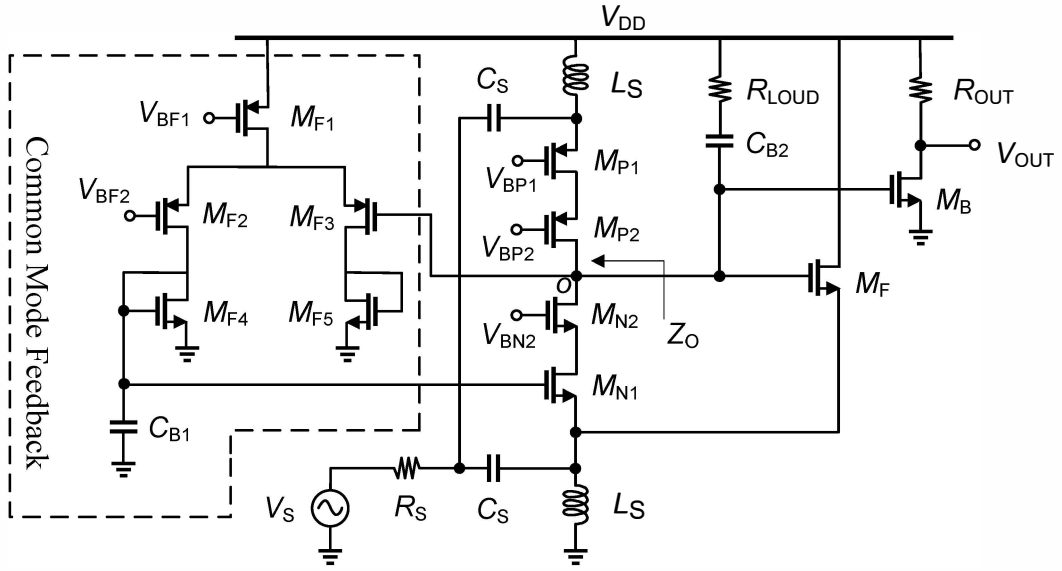

Fig. 2**:** Proposed LNA.

2.2 Input Matching and Gain Analysis

Increasing the transconductance of input transistors decreases the input impedance. To compensate the input impedance, a positive active feedback network comprising of M_F is employed. In contrast to [4], due to M_F's connection manner the proposed structure does not need a differential input signal. The loop gain (G_{loop}) is given by:

$$G_{loop} = \frac{g_{mT} g_{mF} R_S}{1+(g_{mT}+g_{mF})R_S} Z_{OUT} \tag{1}$$

where g_{mT} is $g_{mN1}+g_{mP1}$. g_{mN1}, g_{mP1} and g_{mF} are the transconductance of M_{1N}, M_{1P} and M_F, respectively. R_S is the source resistor. Z_{OUT} is the output impedance which is $R_{LOAD}\|1/j\omega C_{OUT}$, where C_{OUT} is the sum of capacitors at the output node. Equation (1) reveals that any variation in Z_{OUT} with frequency affects G_{loop} directly.

The expression for input impedance is $Z_{in} \approx g_{mT}^{-1} / (1 - G_{loop})$. Therefore, any variation in G_{loop} degrades Z_{in}. While G_{loop} is given by equation (1), the magnitude of corresponding input impedance is:

$$|Z_{in}| = \frac{1}{\sqrt{(g_{mT}+g_{mF}-g_{mT}g_{mF}Z_{OUT-R})^2+(g_{mT}g_{mF}Z_{OUT-I})^2}} \tag{2}$$

where Z_{OUT-R} and Z_{OUT-I} are the real and imaginary parts of Z_{OUT}, respectively. Equation (2) shows that for the sake of constant $|Z_{in}|$, Z_{OUT-R} and Z_{OUT-I}, due to different signs, should vary in a same manner or should be constant. The first solution is not proper because it degrades the voltage gain and the second solution is not practical because for wideband applications it needs a high order filter with several inductors and hence huge die area.

Because of using positive feedback in this structure, for having stability, the gain loop should be $G_{loop}<1$, so, $g_{mT} g_{mF} R_S Z_{OUT}<1+(g_{mT}+ g_{mF})R_S$. For simplifying, we assumed $g_{mF} << g_{mT}$. This assumption causes to reduce the power consumption and also the noise effect of M_F, as a result, $g_{mF} Z_{OUT}<1$, and also, if the real part of Z_{in} is positive, the circuit is stable [6]. Z_{OUT} is defined as the output impedance which is calculated as $(g_{mP1}r_{dsmP1}r_{dsmP2})\|(g_{mN1}r_{dsN1}r_{dsN2})\|R_{LOUD}\|1/sC_{OUT}$ where g_{mP1} and g_{mN1} are the transconductance of M_{P1} and M_{N1} respectively, and R_{LOUD} is the load resistor which can be selected high enough by using the common mode feedback and C_{OUT} is the parasitic capacitance at the output node. According this assumption, the voltage gain of this circuit is calculated as:

$$A_V = \left|\frac{Z_{in}}{Z_{in}+R_S}\right| \frac{g_{mT}Z_{OUT}}{1-G_{Loop}}, \quad Z_{in} = R_S, \left(1-G_{Loop}\right) \approx 1 \\ = 0.5 g_{mT} Z_{OUT} \tag{3}$$

2.3 Noise Analysis

In CG structure the most important source of noise is channel noise of input transistor and it is equal to $(\gamma/\alpha g_m R_S)$, where γ and α are the process dependent parameters, for decreasing NF of CG structure we should increase the transconductances of main transistor. Since g_m of input transistor is constrained by input matching condition, so the increasing of it ruins the input matching, of course, increasing in g_m leads to consume rather power. In the proposed LNA, increasing g_m is used and positive feedback is applied in order to solve the problem of reducing input matching [5]. In addition, two parallel nMOS and pMOS cascode structure is used for decreasing power consumption. This structure compared to ordinary CG LNA, Fig.2, results in twice transconductance and hence reduces the NF with the same power consumption. The sources of noise in the proposed LNA are thermal noise of R_{LOUD}, channel noise of M_F and channel noise of M_{P1} and M_{N1}. They are calculated as (4), (5) and (6) respectively.

$$NF_{R_{LOUD}} = \frac{4kTR_{LOUD}Z_O^{\,2}}{4kTR_S\left(Z_O+R_{LOUD}\right)^2 A_V^{\,2}} \\ \approx \frac{4R_{LOUD}}{R_S g_{mT}^{\,2}\left|Z_{OUT}\right|^2} \approx \frac{4}{R_S g_{mT}^{\,2} R_{LOUD}} \tag{4}$$

In equation (4), we assumed $g_{mF} \ll 1$ so $G_{Loop} \ll 1$ and $(1-G_{Loop}) \approx 1$ and also according Fig. 1, $Z_O \approx (g_{mP1} r_{dsmP1} r_{dsmP2}) \| (g_{mN1} r_{dsN1} r_{dsN2})$ that it is larger than R_{LOUD} so $(Z_O + R_{LOUD}) \approx Z_O$

$$NF_{M_F} = \frac{4kTg_{mF}R_S^2}{4kTR_S}.\frac{\gamma}{\alpha} \approx \frac{\gamma}{\alpha} g_{mF} R_S \qquad (5)$$

Where γ and α are the process dependent parameters.

$$NF_{M_{(N1,P1)}} = \frac{4kTg_{mT}|Z_{OUT}|^2}{4kTR_S A_V^2}.\frac{\gamma}{\alpha} \approx \frac{\gamma}{\alpha}\frac{1}{g_{mT}R_S} \qquad (6)$$

Finally, under input matching condition, i.e. $|Z_{in}| = R_S$, the noise factor is given by:

$$F = 1 + \frac{\gamma}{\alpha}\frac{1}{g_{mT}R_S} + \frac{4}{R_S g_{mT}^2 R_{LOUD}} + \frac{\gamma}{\alpha} g_{mF} R_S \qquad (7)$$

The second and third terms represent the channel and thermal noise contribution of $M_{1N,\ P}$ and R_{LOUD}, respectively. These terms, in contrast to CG structure, can be decreased by increasing the value of g_{mT}. The last term shows the channel noise contribution of M_F which is negligible due to using a very low g_{mF}.

2.4 Non Linearity

IIP3 in this structure is destroyed because of two reasons; firstly, IIP2 which is produced in the direct signal path by second order non-linear component of positive feedback transistor, M_F, is turned to IIP3. Secondly, the third order non-linear component of positive feedback transistor produces IIP3. In the proposed LNA, two techniques are used simultaneously in order to improving linearity.

First, the input pMOS and nMOS transistor is biased in way that each transistor expunges IIP2 of other one [7]. It means that the second order non-linearity of transconductance of nMOS transistor is omitted by the second order non-linearity of transconductance of pMOS transistor, so IIP2 summation of these two transistors counteract each other effects in range of voltage bias. Second, since M_F transistor is main reason for deteriorating linearity, M_F transistor is biased in high gate-source voltage so its IIP2 and IIP3 is improved [8]. Although this way causes to increase current consumption, the size of M_F transistor is very small so its current does not increase dramatically.

3. Simulation Results

The circuit level simulations of the proposed and cascode CG LNAs, Fig. 2, are performed with Spectre RF using a 0.18-µm RF-CMOS technology. For depicting the effect of proposed technique in this structure on NF, in Fig. 3, noise figure of proposed LNA is compared with NF of CG structure, as shown in Fig.1, which its component is as same as proposed LNA except output resistance, R_D. the maximum deal of R_D is selected in order to achieving the best NF, according to Fig. 3, the proposed LNA achieves a

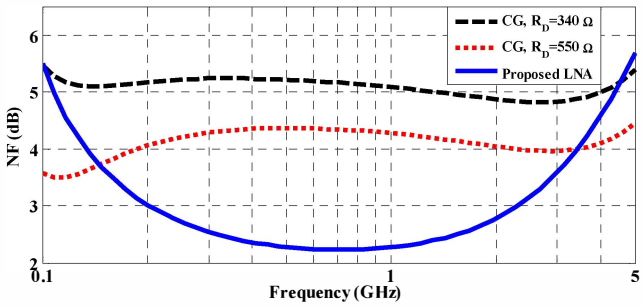

Fig. 3: Simulated NF.

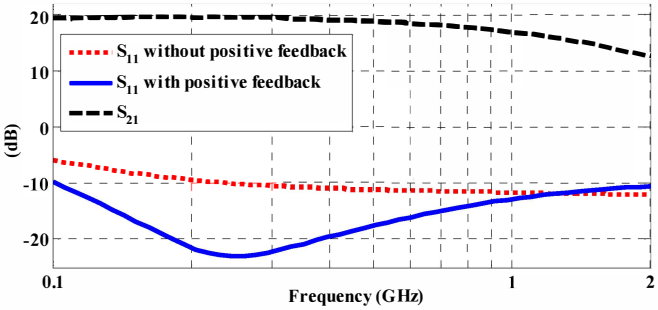

Fig. 4: Simulated input return losa,S_{11}, and powr gain, S_{21}.

state-of-the-art NF of 2.2 dB which is 2.9 and 2.1 dB less than the minimum NF in cascode CG LNA with different value of R_D, 340Ω and 550Ω , respectively.

The cascode CG LNA consumes 2.9 mW and the proposed LNA only consumes 2.8 mW and also, the NF of CG LNA is 50% more than that of the proposed one. Fig. 4 shows the effects of proposed LNA components on S_{11}. As is seen, the LNA before using the positive feedback owing to high g_{mT} dose not have an acceptable input matching, especially in low frequencies. According Fig.4, the proposed LNA due to using a high transconductance and large output resistance achieved 19.7 dB S_{21} which is 7 dB more than the cascode CG one. Nonetheless, the CG LNA structure has inherently high linearity [1]. Tow-tone RF signal, which sweep from 100MHz up to 2GHz, are used to simulate the linearity performance of this LNA, Fig. 5 shows that IIP3 is varied from -12 dBm to -6 dBm and also IIP2 variation is between 1-15 dBm. In addition, the designed values of proposed LNA are shown in table I.

To compare the proposed LNA with previous topologies, we have used two figures of merit (FOM) defined in [2], thereupon, this result is compared in Table II.

$$FOM_1 = \frac{Gain[abs] \times BW[GHz] \times IIP3[mW]}{(F-1) \times P_{dc}[mW]}. \qquad (8)$$

TABLE I. DESIGNED VALUES OF THE LNA.

Capacitor		Resistor		Transistor size	
C_S	30pF	R_{LOUD}	600Ω	$(W/L)_{N1}$	(17×6.5)µm/180µm
				$(W/L)_{N2}$	(6×6.5) µm/180µm
C_{B1}	20pF	R_{OUT}	55 Ω	$(W/L)_{P1}$	(56×6.5)µm/180µm
				$(W/L)_{P2}$	(19×6.5)µm/180µm
C_{B2}	20pF	R_D	340 Ω	$(W/L)_B$	(6×6.5)µm/180µm
				$(W/L)_{F1}$	(6×1.5) µm/180 µm
Inductor		supply		$(W/L)_{F2,F3}$	(3×1.5) µm/180 µm
L_S	150nH	V_{DD}	1.8V	$(W/L)_{F,F4,F5}$	(1×1.5)µm/180µm

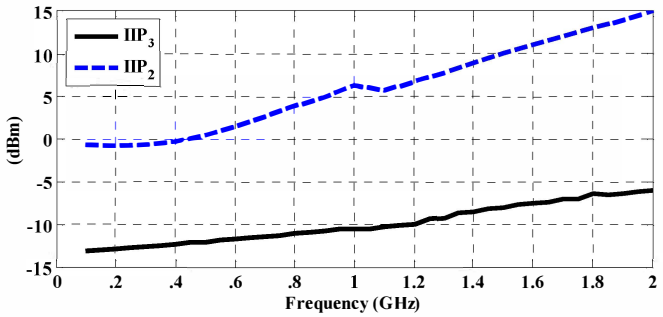

Fig. 5: IIP2, IIP3.

$$FOM_2 = \frac{Gain_{average}[abs] \times BW[GHz]}{\left(F_{average} - 1\right) \times P_{dc}[mW]}. \quad (9)$$

Where $Gain_{average}$ is the average power gain, $F_{average}$ is the average noise factor over the frequency range, IIP3 is the input 3rd-order intercept point and P_{dc} is the power consumption. According to Table II, this structure can achieve a very low noise figure and has very low power consumption by using two parallel pMOS and nMOS cascode CG branches and positive feedback. Although this structure does not have good linearity, its low power and NF and high gain cause this structure has good performance.

4. Conclusion

A novel low-power UWB technique using the positive feedback to reduce the NF in CG LNAs was presented and also, a common mode feedback is used for biasing output voltage and preventing it from variation. The aforementioned scheme can be used in both single-ended and differential LNAs. The proposed LNA achieves the noise performance as well as the noise cancelling LNAs with much less power consumption since there is only one main branch consuming the power in the proposed LNA approach.

References

[1] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004H. Zhang et al., "A low-power, linearized, ultra-wideband LNA design technique," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 320-330, Feb. 2009.

[2] H. Zhang, X. Fan, and E. Sanchez, "A low-power, linearized, ultra-wideband LNA design technique," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 320-330, Feb. 2009

[3] C.-F. Liao and S.-I. Liu, "A broadband noise-canceling MOS LNA for 3.1–10.6-GHz UWB receiver," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 329–339, Feb. 2007.

[4] A. Liscidini et al., "A 0.13 µm CMOS front-End, for DCS 1800/UMTS/802.11b-g with multiband positive feedback low-noise amplifier," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 981–989, Apr. 2006.

[5] M. S. Mehrjoo and M. Yavari, "A low power UWB very low noise amplifier using an improved noise reduction technique," *in Proc. IEEE International Symposium on Circuits and Systems* (*ISCAS*), Rio de Janeiro, Brazil, pp. 277-280, May 2011

[6] B. Razavi, *RF microelectronics*, Prentice Hall, Upper Saddle River, New Jersey, 1998.

[7] W.-H. Chen, G. Liu, B. Zdravko, and A. M. Niknejad, "A highly linear broadband CMOS LNA employing noise and distortion cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1164–1176, May 2008.

[8] H. Zhang, X. Fan, and E. Sanchez, "Linearization techniques for CMOS low noise amplifiers: a tutorial," *IEEE Trans. Circuits Syst.I*, vol. 58, no. 1, pp. 22-36, Jan. 2011.

[9] D. Im, I. Nam, H.-T. kim, and K. Lee, "A wideband CMOS low noise amplifier employing noise and IM2 distortion cancellation for digital TV tuner," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 686–698, Mar. 2009.

[10] Y.-H. Yu, Y.-S. Yang, and Y.-J. Emery Chen, "A compact wideband CMOS low noise amplifier with gain flatness enhancement," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 502-509, Mar. 2010.

[11] D. Im, I. Nam, H.-T. kim, and K. Lee, "A CMOS active feedback balun-LNA with high IIP2 for wideband digital TV receivers," *IEEE Transaction on Microwave Theory and Technique*, vol. 58, no. 12, pp. 3566–3579, Dec. 2010.

[12] S. B. T. Wang, A. M. Niknejad, and R. W. Brodersen, "Design of a sub-mW 960-MHz UWB CMOS LNA," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2449–2456, Nov. 2006.

[13] T. W. Kim, H. Muthali, S. Sengupta, K. Barnett, and J. Jaffee, "Multi-standard mobile broadcast receiver LNA with integrated selectivity and novel wideband impedance matching technique," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 675–685, Mar. 2009.

TABLE II. DESIGNED VALUES OF THE LNA.

Ref.	3dB B. W. GHz	NF (dB)	S_{11} (dB)	S_{21} (dB)	IIP3 (dBm)	IIP2 (dBm)	Power (mW)	FOM_1	FOM_2	Technology
[1]	0.002-1.6	1.9-2	-8	13.7	0(2)	12(3)	35	1.9	1.9	0.25 µm
[9]	0.048-1.6	3-3.2	-9	11-14	+3(4)	44(5)	34.8	1.6	0.8	0.18 µm
[10]	0.04-1.2	2.1-3.4	-10	13.4-16.4	-1- 0	NA	14.4	5.7	5.7	0.18 µm
[11]	0.05-1.5	2.5-3	-8.5	15-18	-0.5(6)	29.5(7)	30	3.5	3.9	0.13 µm
[12]	0.1-0.93	3.6-4.8	-10	10-13	-10	NA	0.72	1.7	17.7	0.13 µm
[13]	0.47-0.856	1.6-1.8	-6	25	-1	NA	46	4.7	5.9	0.18 µm
This work	0.1-1.1	2.2-2.5(1)	-10	16.7-19.7	-12.9- -9.5	-0.5- 6	2.8	5.6	50.5	0.18 µm

(1) FROM 250MHZ UP TO 1.1GHZ, (2) AT 900MHZ, (3) F_1, F_2= 200, 300MHZ, (4) AT 100MHZ, (5) F_1, F_2= 400, 450 MHZ, (6) AT 400MHZ, (7) F_1, F_2= 400, 406 MHZ