A Low-Power Noise Reduction Technique for Broadband CMOS Low-Noise Amplifiers

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***Abstract*— A broadband input matching technique for low noise amplifiers (LNAs) is presented which exploits an active feedback network to achieve better noise performance. The presented matching scheme is compared to the common-gate and conventional noise canceling structures. The noise performance of the presented technique is similar to that of the conventional noise canceling technique with much less power consumption. In contrast to the traditional noise cancellation circuit, the proposed LNA does not degrade the linearity and its IIP3 is similar to the simple common-gate LNA. The proposed technique is applied to an LNA operating in 2~6.5 GHz bandwidth. The circuit is designed in a 0.18 µm RF CMOS technology with a 1.8 V power supply. This LNA achieves an IIP3 of +5.4 dBm, 17 dB voltage gain, and 2.5 dB noise figure while consuming 7.6 mW power.**

Keywords- Ultra wideband (UWB), low noise amplifier, noise cancellation, low power.

I. INTRODUCTION

The need for multi-purpose receivers instead of a few narrow-band receivers calls for wideband design in order to lower the overall power and area in use. The LNA as the first block of the receiver must provide good input matching, low noise figure (NF), high linearity, and a reasonable gain over the whole bandwidth. Besides, the power consumption should also be considered.

Several CMOS wideband LNAs such as the feedback and common-gate (CG) amplifiers have been reported [1]. The common-gate structure is a well-known method to provide a wideband input matching. But, this robust matching network suffers from poor noise performance owing to limited g_m of the CG transistor to 20 mA/V. The shunt feedback amplifiers provide wideband input matching and low noise figure (NF) at the cost of high power dissipation and the stability problems. A rather new method for lowering the noise figure is to utilize a noise cancellation technique which usually includes two different paths with similar polarity for signal and different polarity for channel noise of CG transistor. This results in cancellation of the CG transistor channel thermal noise at the summation point. Both, paths are usually designed by active elements, i.e. transistors [2-4]. The overall output noise in these designs is limited to other transistors in the signal path. They also consume relatively high power.

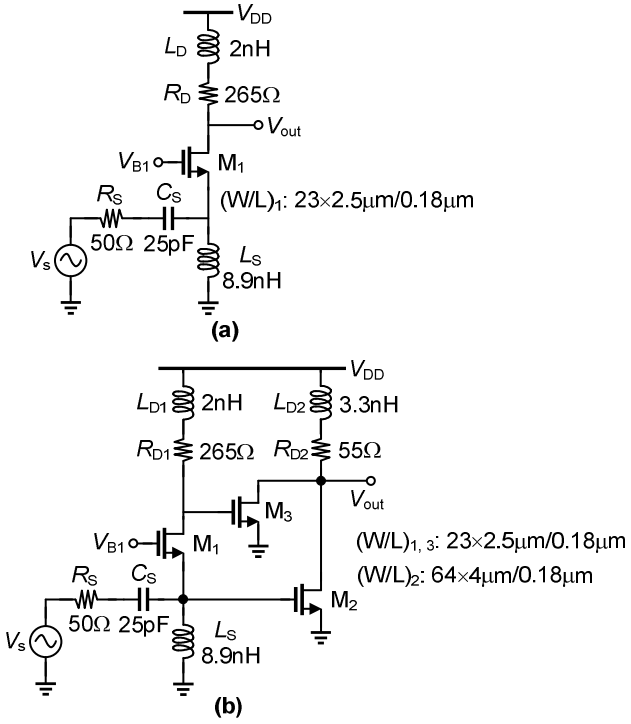

Figure 1: (a) Common gate LNA and (b) conventional noise cancellation technique (the bias circuits of M_2 and M_3 not shown).

In this paper, a new wideband input matching technique is presented. This structure employs an active feedback in the conventional CG LNA to reduce the NF as well as to achieve the wideband input matching. It is shown that by using this method the input impedance of the proposed LNA stays in matching with the 50 Ω antenna while increasing the g_m of the CG transistor as high as desired. As a result, the channel noise of the CG transistor is significantly reduced. So, this technique focuses on the noise reduction instead of noise cancellation.

This paper is organized as follows. Section 2 reviews two conventional CG and noise canceling structures. The proposed LNA is described in Section 3. The simulation results and conclusions are presented in Sections 4 and 5, respectively.

II. THE CG LNA AND NOISE CANCELLATION TECHNIQUE

A. Common gate LNA

Figure 1(a) shows the common-gate low noise amplifier. This structure is suitable for providing wideband input matching. The input impedance of this circuit is g_m^{-1}. At complete input matching (g_m^{-1} is set equal to the source impedance, R_S), the gain and noise factor of this circuit are given by (1) and (2), respectively.

$$A_v = 0.5 g_{m1} |Z_D| \tag{1}$$

$$F = 1 + \frac{\gamma}{\alpha} + \frac{4R_D}{g_{m1}|Z_D|^2} \tag{2}$$

where $Z_D=R_D+j\omega L_D$, γ and α are process dependant parameters and for a CMOS technology with minimum channel length of 0.18 μm they are about 1.3 and 1, respectively [5]. The second term in (2) is the dominant one which represents the channel noise of M1. The third term belongs to the thermal noise of the output resistor, R_1. According to (2), even when the output impedance is high enough to make the third term negligible, the noise figure would still be more than 3.6 dB. In practice, due to limited voltage head-room, such conditions won't be satisfied and the noise figure will be about 4.5 dB.

B. Traditional noise cancellation

Figure 1(b) shows the traditional noise canceling structure [4]. The input impedance of this structure is similar to that of the simple CG. The channel noise of M1 has different polarities on two paths. Therefore, with appropriate choice of RD1 and device sizes, this channel noise can be cancelled out. Equations (3) and (4) show the voltage gain and noise factor of this structure when the input node is fully matched with the antenna ($g_{m1}^{-1}=R_S$), respectively.

$$A_v = -0.5(g_{m1}g_{m3}|Z_{D1}| + g_{m2})|Z_{D2}| \tag{3}$$

$$F = 1 + \frac{(g_{m3}|Z_{D1}| - g_{m2}R_S)^2}{R_S(g_{m1}g_{m3}|Z_{D1}| + g_{m2})^2}\frac{\gamma}{\alpha}g_{m1} + \frac{g_{m2}|Z_{D2}|^2}{A_v^2 R_S}\frac{\gamma}{\alpha} + \frac{(g_{m3}|Z_{D2}|)^2}{A_v^2}\frac{R_{D1}}{R_S} \tag{4}$$

where $Z_{D1}=R_{D1}+j\omega L_{D1}$ and $Z_{D2}=R_{D2}+j\omega L_{D2}$. The three last terms in (4) represent the thermal noise of M1, M2, and R_{D1}, respectively. Other sources of noise are considered to be negligible. As Eq. (4) clearly reveals if the criterion $g_{m3}|Z_{D1}|=g_{m3}R_S$ is completely satisfied, the channel noise of M1 will be suppressed. This structure has a high power consumption and poor linearity in comparison with the CG structure. In applications with high linearity requirements, some distortion cancellation methods must be applied [2].

III. PROPOSED LNA

Figure 2 shows the proposed LNA structure. The transistor M1 is responsible for signal amplification and M2 is an active feedback network. The input impedance of this circuit is:

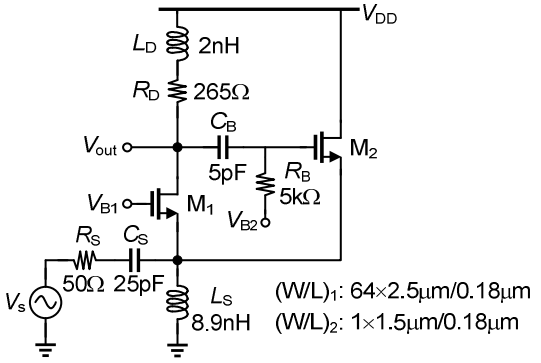

Figure 2: Proposed LNA.

$$Z_{in} = \frac{1}{g_{m1} - g_{m2}(g_{m1}Z_D - 1)} \tag{5}$$

Where $Z_D=R_D+j\omega L_D$. According to relation (5), for appropriately chosen values of g_{m2} and Z_D, g_{m1} can be chosen up to any arbitrary value and the input matching criterion ($|Z_{in}|=R_S$) will be still satisfied. This increment in g_{m1} will reduce the contribution of M1's channel noise. The voltage gain is given by:

$$A_v = \frac{g_{m1}|Z_D|}{1 + (g_{m1} - g_{m2}(g_{m1}|Z_D| - 1))R_S} \tag{6}$$

When the circuit is matched to the source, the (6) will be simplified to (7) and the noise factor can be calculated as (8).

$$A_v = \frac{g_{m1}|Z_D|}{1 + R_s R_{in}^{-1}} = 0.5 g_{m1}|Z_D| \tag{7}$$

$$F = 1 + \frac{\gamma}{\alpha}\frac{1}{g_{m1}R_s} + \frac{4R_D}{R_s g_{m1}^2 |Z_D|^2} + \frac{\gamma}{\alpha}g_{m2}R_S \tag{8}$$

Equations (7) and (1) look similar. But, in (1) the value of g_{m1} is set to 20 mA/V while in (7) it can be chosen arbitrarily. In relation (8), the second and third terms represent the thermal noise of M1 and R_D, respectively. The fourth term shows the thermal channel noise of M2. This term is negligible regarding to small sizing of M2. The power consumption of M2 is also rather small. As is seen, by increasing g_{m1} the noise factor of the amplifier is reduced. Of course, g_{m1} is limited by the power considerations. In this design, g_{m1} and g_{m2} are set to 50 mA/V and 2 mA/V, respectively. According to device sizes shown in Fig. 2, the second to fourth terms of relation (8) are 0.52, 0.07 and 0.13, respectively, resulting in total NF of 2.3 dB. These terms were calculated at 5 GHz.

Since the proposed circuit utilizes a feedback network, its stability needs to be considered. To maintain stability over the frequency range of interest, the real part of the input impedance must remain positive [6]. In this structure, according to equation (5), for not appropriately chosen values of elements negative input impedance could appear. Nonetheless, when the size of M2 and the value of R_D are chosen so as to provide the input matching, the negative input resistance won't occur and the circuit will be stable as shown later.

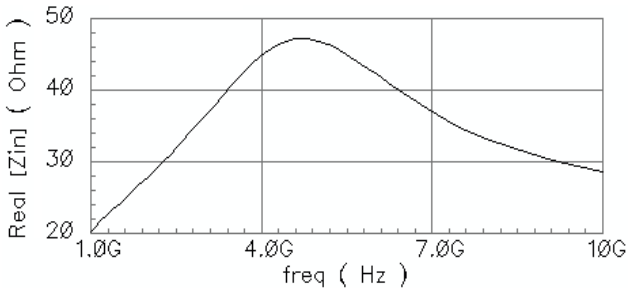

Figure 3: Real part of input impedance.

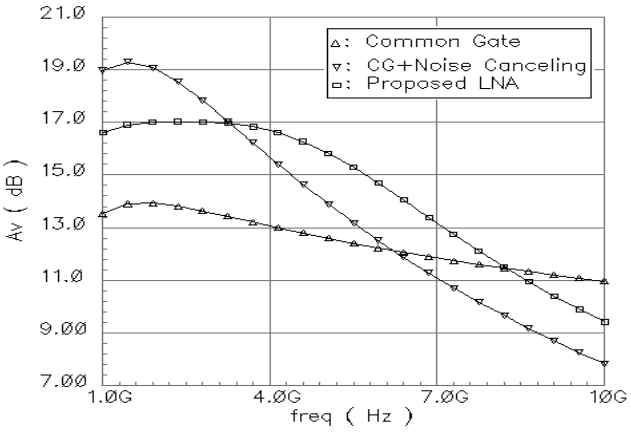

Figure 4: Voltage gain.

IV. Simulation Results

To prove the usefulness of the proposed LNA, the circuit level simulations were performed with Spectre RF using a 0.18 µm RF CMOS technology. Both conventional CG amplifier and the CG structure with noise cancellation technique shown in Fig. 1 were also simulated to provide a fair comparison. The design is targeted to achieve a lower NF and power consumption over a very wide bandwidth from 2-6.5 GHz. Firstly, to examine the stability of the proposed LNA, the simulated real part of the input impedance is shown over a wide frequency range in Fig. 3. As is clear, the real part of Zin is positive over the whole bandwidth. Figure 4 illustrates the voltage gain of the simulated amplifiers. A maximum voltage gain of 17 dB is achieved for the proposed LNA. In the noise cancellation LNA, the large parasitic capacitances of CS transistor degrade the BW. So, this scheme with 1.4~3.7 GHz has the lowest BW. The simple CG LNA with 8.2 GHz BW (1.8-10 GHz) has the maximum BW. Its voltage gain is the minimum one owing to its lower g_m.

The input matching of simulated LNAs is shown in Figure 5. The proposed LNA achieves S11 < -10 dB over 2-10 GHz bandwidth. The simple CG and noise cancellation LNAs, respectively, achieve S11 < -11 dB and S11 < -7.5 dB over -3 dB BW. In the noise cancellation LNA, the large parasitic capacitances of CS transistor degrade the S11 dramatically when frequency rises. As shown in Figure 6, the NF of the proposed LNA is about 2.5 dB with a variation less than 0.2 dB over 2-10 GHz. It follows the calculation results very well. This state-of-the-art NF is achieved with only 7.6 mW power

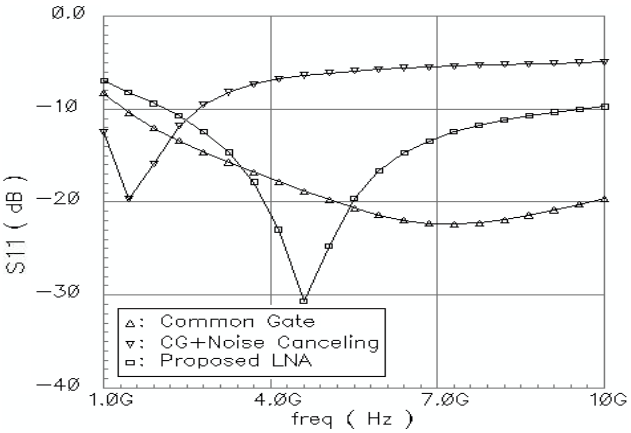

Figure 5: S_{11} of simulated LNAs.

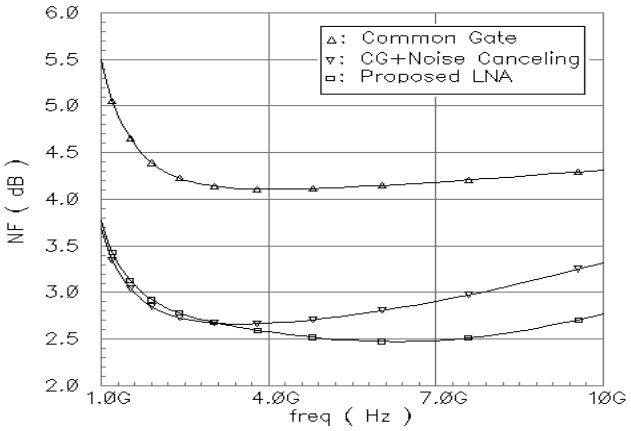

Figure 6: Noise figure.

consumption. As it was calculated the NF of the proposed structure is about 1.7 dB less than the simple CG amplifier. The minimum NF of the noise cancellation LNA over its -3 dB BW is 0.1 dB better than proposed LNA over the same frequency range, while it consumes three times more power than the proposed one. Figure 7 shows that the proposed LNA achieves IIP3 = +3.4 dBm when two sinusoidal tones at 3 GHZ and 3.1 GHz have been used. In UWB applications, the IIP3 must be examined over whole BW and a single point simulation is not enough. So a sweeping two tones test with -20 dBm input power and 100 MHz frequency spacing is performed over 1~10 GHz frequency range. Figure 8 indicates the IIP3 of three simulated structures versus intermodulation frequency. The IIP3 of proposed LNA over -3 dB BW is in the range of +3.6~+6.5 dBm. In the worst case, it is just 2.1 dBm less than the simple CG. Figure 8 also shows in contrast to the proposed LNA, the traditional noise cancellation structure suffers from poor linearity performance. Its IIP3 falls to -5.6 dBm over -3 dB BW. The sharp increase of IIP3 in noise cancellation LNA is according to voltage gain rapid fall (Fig. 4). This happening in simple CG and the proposed LNA is less considerable than the noise cancellation one. The performance results of simulated LNAs and a few prior published state-of-the-art broadband LNAs are summarized in Table 1. As is seen, the proposed LNA achieves better NF with much less power consumption than the previously reported best NF in [2]. This

TABLE I. PERFORMANCE COMPARISON OF WIDEBAND VERY LOW NOISE AMPLIFIERS.

Reference	Technology	BW [GHz]	S_{11} [dB]	A_V [dB]	NF [dB]	IIP3 [dBm]	V_{DD} [V]	Power
Proposed LNA	0.18 µm	3.0~6.5	< -10	17	2.5~2.7	3.4~5.4	1.8	7.6 mW
CG	0.18 µm	1.8~10	< -11	14	4.1~4.8	5.2~6.3	1.8	4.6 mW
Noise Canceling	0.18 µm	1.4~3.7	< -7.5	19	2.7~3.5	-5.6~1.1	1.8	21.6 mW
[1]	0.18 µm	0.4-10	< -10	18.4*	4.4~6.5	-6	1.8	12 mW
[2]	0.13 µm	0.8~2.1	< -8.5	20.5*	2.6	16	1.5	17.4 mW
[3]	65 nm	0.2~5.2	< -14	15.6	< 3.5	> 0	1.2	21 mW
[4]	0.18 µm	1.2~11.9	< -11	15.7*	4.5~5.1	-6.2	1.8	20 mW
[7] LNA I	0.13 µm	0.2~3.8	< -9	19	2.8~3.4	-4.2	1	5.7 mW
[7] LNA II	0.13 µm	0.2~3.8	< -9	14.8	3.5~4.1	-3.8	0.85	3.2 mW
[8]	0.13 µm	2~9.6	< -9.5	17*	3.6~4.8	-7.2	1.5	19 mW

* The power gain was reported. Here the insertion loss (6 dB) from the buffer is deembedded.

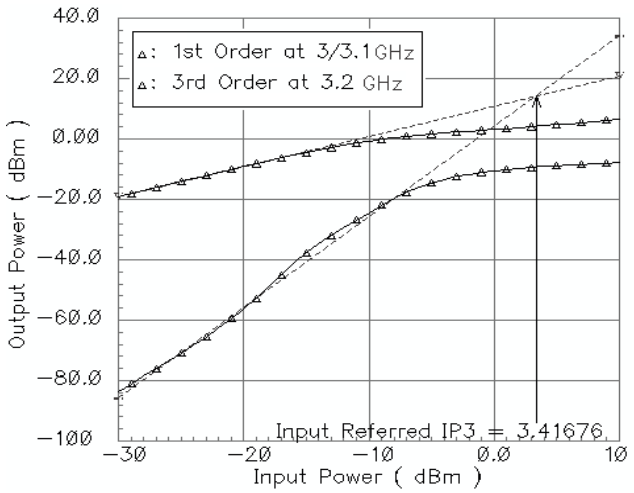

Figure 7: The IIP3 of proposed LNA at 3.2 GHz with 100 MHz frequency spacing.

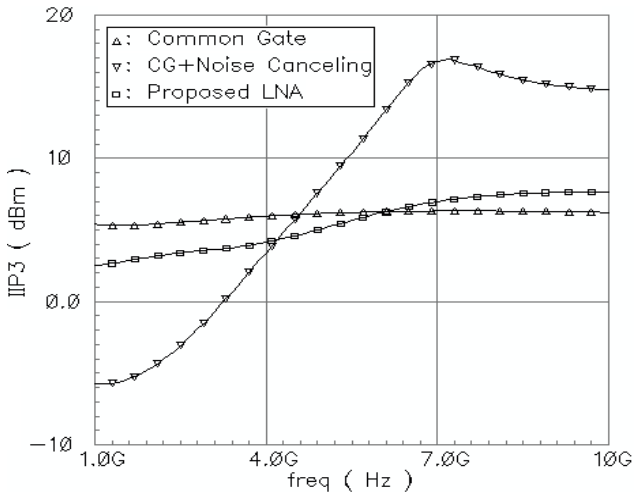

Figure 8: The IIP3 of simulated LNAs using 100 MHz frequency spacing two tones with -20 dBm input power level.

is mainly due to the simple structure used to reduce the NF instead of a two path structure for noise cancellation. Although the power consumption of LNAs presented in [7] is less than the proposed LNA, however, the NF and IIP3 of the proposed LNA are superior to those reported in [7].

V. CONCLUSIONS

A new wideband LNA design technique was proposed. In this technique the noise is reduced instead of being cancelled. It was demonstrated that the noise performance of the proposed LNA rubs shoulder with that of noise canceling LNA, while the noise canceling technique consumes much more power than the proposed LNA. Comparison of the NF and power consumption with prior published state-of-the-art noise cancellation LNAs confirms it too. The proposed LNA was designed and simulated in a 0.18 µm RF CMOS technology. Its voltage gain variation over lower UWB band is just 1 dB. The NF of the proposed LNA is between 2.5 and 2.7 dB over the -3 dB BW, while consumes only 7.6 mW.

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