A 2.6-13.7 GHz Highly Linear CMOS Low Noise Amplifier for UWB Applications

Babak Mazhabjafari and Mohammad Yavari
Integrated Circuit Design Laboratory, Department of Electrical Engineering,
Amirkabir University of Technology, Tehran, Iran
Emails: babak.mazhabjafari@aut.ac.ir, myavari@aut.ac.ir

Abstract—**In this paper a highly linear differential CMOS low noise amplifier (LNA) for ultra-wideband (UWB) applications is proposed. The proposed LNA uses a linearization technique to improve both input second- and third-order intercept points (IIP2 and IIP3), simultaneously. The linearity is improved by canceling the common-mode part of all intermodulation (IM) components from the output current. Analysis and simulation results using a 90 nm RF-CMOS process with Spectre-RF show that the IIP3 and IIP2 are improved more than 11 and 35 dB, respectively, at the expense of increasing the noise figure only about 0.2 dB respected to the conventional differential common-gate (CG) LNA.**

Key words: Ultra wideband; CMOS low noise amplifier; noise figure; distortion cancellation; common-mode current; IIP3; IIP2

I. INTRODUCTION

The increasingly pervasive interest and use of wireless broadband technologies especially UWB is due to its low power and high data rate transmission capability [1]. A UWB RF designer should deal with severe challenges due to requirement of operating with a low power in an ultra-wide frequency range. As the first and a critical block in a wideband receiver, an LNA must provide good input matching, high linearity, low noise figure (NF), and adequate and flat gain over a wide frequency range to obtain a high dynamic range for a highly sensitive wideband receiver with low power consumption [2].

In an RF transceiver, the power of interferers and intermodulations which are generated from blockers or transmitter leakages, are not reduced by preceding filters. Furthermore, while f_T increases and noise performance and bandwidth of CMOS LNAs are improved with technology scaling, the linearity degrades due to lower supply voltage and high-field mobility effects [3]. Thus, achieving the stringent linearity requirement in deep-submicron CMOS processes is a big challenge for UWB applications. Therefore, in order to maximize linearity/power, a linearity improvement technique should be employed [3]. Several LNA linearization methods reported before, are either for narrowband applications or only concentrated on input third-order intercept point (IIP3), while in wideband applications, the input second-order intercept point (IIP2) is important as well as IIP3. Therefore, the differential topologies are more attractive due to their symmetry to reject second-order components and improve IIP2.

This paper presents a CMOS differential LNA using a new linearization technique to improve both input second- and third-order intercept points (IIP2 and IIP3), simultaneously, which is called the common-mode current canceling (CMCC) technique. The CMCC technique improves linearity by canceling the common-mode part of output current and attenuating second- and third-order intermodulation components (IM2 and IM3).

The paper is organized as follows. Section 2 describes the concept of the proposed linearity improvement technique. The structure of the proposed LNA and its circuit analysis, considering input matching, gain, noise, and linearity analysis are provided in Sect. 3. In Sect. 4, the circuit level simulation results are presented. Finally, Sect. 5 concludes the paper.

II. PROPOSED LINEARITY IMPROVEMENT TECHNIQUE

In differential topologies all small-signal currents can be decomposed into common-mode and differential parts as $i = i_{diff} + i_{cm}$. The CMCC technique cancels the common-mode part from the output current by an auxiliary pair which generates an equal i_{cm} to the main pair with the opposite sign. Canceling the common-mode current at all frequencies decreases both IM2 and IM3 currents, simultaneously. Figure 1 shows the conceptual schematic of the CMCC technique.

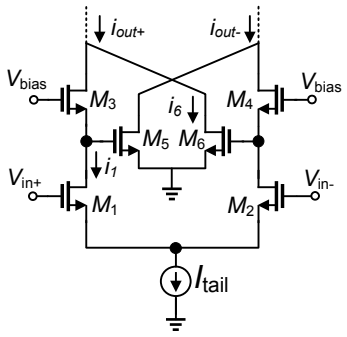

Figure 1. Conceptual scheme of the proposed CMCC technique.

According to Fig. 1, if $M_{3,4}$ and $M_{5,6}$ are designed properly to have equal transconductance (g_m), the main and auxiliary pairs will have equal v_{gs} with an opposite sign. Thus, according to (1) and (2), i_{cm} will be attenuated considerably in each left and right branch currents (i_{out+} and i_{out-}) and the output current will has no i_{cm}.

$$i_{out+} = i_1 + i_6 = i_{diff}\left(1+\frac{g_{m6}}{g_{m4}}\right)+i_{cm}\left(1-\frac{g_{m6}}{g_{m4}}\right) \qquad (1)$$

$$i_{out-} = i_2 + i_5 = -i_{diff}\left(1+\frac{g_{m5}}{g_{m3}}\right)+i_{cm}\left(1-\frac{g_{m5}}{g_{m3}}\right) \qquad (2)$$

where g_{mi} is the total transconductance of M_i. The currents of i_5 and i_6 are calculated by assuming $v_{gs5,6} = -i_{1,2}/g_{m3,4}$.

III. Proposed LNA Structure

The proposed highly linear UWB LNA with the CMCC linearization technique is shown in Fig. 2. A differential cascode CG structure including $M_{1\text{-}4}$ is used as the main amplifier. M_5 and M_6 form an auxiliary path to generate the same common-mode current to the main amplifier with the opposite sign to improve the linearity. R_L in parallel with L_D and output parasitic capacitance form a passive *RLC* Load. Inductor L_S is utilized to compensate the capacitive part of the input impedance. L_B and C_{pad} are the bond-wire inductor and input pad parasitic capacitance, respectively. The inductor L_C and the parasitic capacitances at drain of $M_{1,2}$ and source of $M_{3,4}$ form a π network. Proper choice of L_C partially cancels the effect of the parasitic capacitances and prevents from the voltage gain reduction at high frequencies. Under this condition, the nonlinearity and noise of $M_{3,4}$ can be neglected [4] and the noise contribution of R_D becomes negligible [5].

Also to have a fair comparison of linearity improvement a conventional CG LNA is designed and simulated in a 90 nm RF-CMOS process. A proper biasing circuit is used to generate the bias voltages in the proposed LNA which is not shown in Fig. 2 for simplicity.

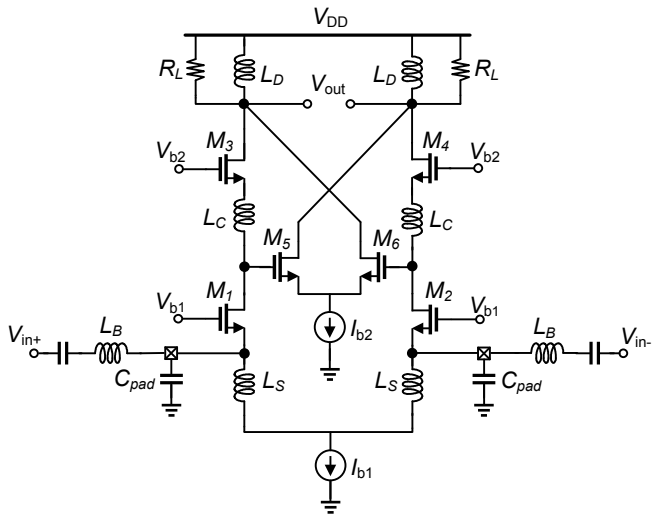

Figure 2. Proposed UWB LNA.

A. Balun Circuitry

As mentioned in the previous section, the LNA is the first block in the RF receiver and its input signal comes most often from the antenna. Thus, neither it has to be a single-ended input or utilizing of a bulky and noisy balun to convert the single-ended input to a differential one. By canceling the common-mode current in the fundamental frequency, the proposed LNA does not need any balun. Therefore, it is possible to use of a differential LNA structure for a single-ended input coming from the antenna [6]. The proposed CMCC technique eliminates the need of balun due to canceling the common-mode parts of the output current at all frequencies.

B. Input Matching

Equation (3) defines the input impedance of the proposed CG LNA by assuming $g_m r_{ds} >> 1$.

$$Z_{in}(s) \approx \frac{1}{sC_{pad}} \| \left[sL_B + \left(\frac{1}{g_{m1}} \| sL_S \| \frac{1}{sC_{P1}} \right) \right] \qquad (3)$$

where C_{P1} is the total parasitic capacitance at the source of M_1 including C_{gs1} and C_{sb1}.

Inductor L_S is designed to resonate with C_{P1} at the center frequency of bandwidth. It remains a series *L*-match network at the input of the proposed LNA including C_{pad}, L_B and $1/g_{m1}$. Thus, the matching condition is simplified as:

$$g_{m1,eff} R_S = 1 \qquad (4)$$

where $g_{m1,eff} = g_{m1}/(1 + Q_L^2)$. Q_L is the quality factor of the *L*-match network and is equal to $\omega_0 L_B g_{m1}$. Equation (4) indicates that g_{m1} should be greater than the conventional one to satisfy the input matching condition which has good effects on NF at the expense of increasing the power consumption.

C. Gain

According to Fig. 2, the total output current of the proposed LNA can be calculated as (5), if it is assumed that i_j stands for the small-signal current of transistor M_j and i_{out+} and i_{out-} represent the output currents of the proposed LNA, respectively.

$$i_{out} = i_{out+} - i_{out-} = (i_1 + i_6) - (i_2 + i_5) = 2G_m v_{in} \qquad (5)$$

where $G_m = g_{m1} + g_{m6}$, represents the total transconductance.

The body effect is ignored for simplicity. So, the total output current of the proposed LNA is increased compared to the conventional counterpart. Therefore in order to achieve the same gain for a fair comparison of noise and linearity, the proposed LNA consumes less power.

D. Noise

To estimate the added noise, it should be noticed that at the output of the LNA, the thermal noise is only important and so the flicker noise ($1/f$ noise) is neglected. According to Fig. 2 the proposed CMCC technique increases the output noise current. The noise of M_5 and M_6 is added at the output directly. Also, the auxiliary pair amplifies the voltage noise of nodes *A* and *B* created by the noise current of M_1 and M_2, respectively. Figure 3 shows that the thermal noise of M_2 transferred to the output through M_1 and $M_{3,4}$ by a factor of $0.5(1+g_{m5}/g_{m3})$. Also the noise current of M_3 and M_4 passes through itself since $1/g_{m3,4} << R_{D1}$, where $R_{D1} = [r_{ds1} + (1+g_{m1,eff} r_{ds1}) R_S] \approx 2r_{ds}$. Thus, the noise factor of the proposed LNA half circuit can be approximated by (6), when the input impedance is fully matched.

$$F = 1 + \frac{\gamma}{\alpha} + 4g_{m5}R_S \frac{\gamma}{\alpha} A^2 + \frac{4R_S}{R_L} A^2 \qquad (6)$$

where $A=g_{m3}/(g_{m3}+g_{m5})$. The second and third terms of (6) represent the thermal noise M_1 and M_5, respectively. The last term shows the thermal noise contribution of R_L in the total noise factor. The total noise factor of the proposed LNA is twice than of (6) due to its differential topology.

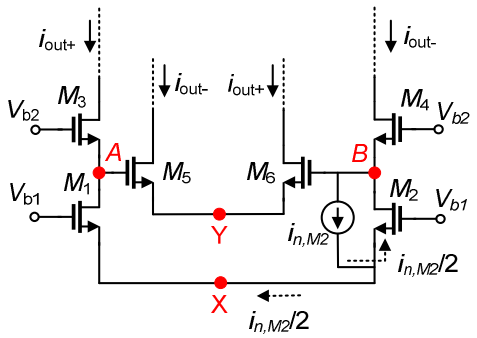

Figure 3. Equivalent circuit for calculating the noise of M_2.

E. Linearity

The proposed technique improves the linearity especially IIP2 which is improved because i_{cm} is the dominant part in IM2 current [8]. The IM3 originates from the MOSFET intrinsic third-order nonlinearity, g_m'', and interaction between the fundamental tone and other distortion components especially IM2 and second-order harmonic distortion (HD2). Because the IM3 is often the largest in-band component, canceling its common-mode part has more effect on the LNA linearity performance [6]. Also the proposed LNA has a negligible second-order interaction effect due to canceling the IM2 component. Also using a cascode topology attenuates the IM components of M_1 and M_2 which contributes at the output through auxiliary transistors (M_5 and M_6) by a factor of $1/g_{m3,4}$.

IV. Simulation Results

To confirm the effectiveness of the proposed linearization technique, the proposed UWB LNA is simulated in worst corner cases in a standard 90 nm RF-CMOS process using Spectre-RF simulator. Figure 4 shows the input matching coefficient (S_{11}) of the proposed LNA. According to this figure, the S_{11} is below -10 from 2.6 GHz to 13.7 GHz. Figure 5 shows that the flat S_{21} of 11 dB with only 0.7 dB variation over entire bandwidth is obtained with the aim of L_C and cascode structure. Moreover as it is clear in Fig. 5, the inductor L_C prevents from NF rising at high frequencies by canceling the parasitic capacitances of nodes A and B in the proposed LNA which compensates the power gain falling at these frequencies. Thus, the proposed LNA achieves a flat NF about 3.8 dB in the whole frequency range.

To examine the linearity improvement a two-tone test with 20 MHz spacing at 6.5 GHz is performed. As Fig. 6 exhibits, the proposed LNA achieves +4.6 dBm IIP3. So, the proposed CMCC technique improves IIP3 more than 11 dB compared to conventional counterpart. The CMCC effect on IIP2 is tested by another two-tone test with 20 MHz spacing at 4.5 GHZ which generate an IM2 tone at the frequency of 9.02 GHz. for IIP2 simulation an intentional 2% mismatch is considered in the passive elements and for transistors, a random mismatch in the aspect ratio of the corresponding MOSFETs is given by the value of 1%. Several simulations are performed and as Fig. 7 shows, the proposed LNA achieves an IIP2 of +66.4 dBm.

A comparison between the proposed LNA and some of the prior state of the art LNAs is performed in Table I. As is seen, the proposed LNA achieves better IIP3 with much less power consumption than the previously reported ones especially in [8] and [11]. Also the circuit simulation results of the proposed LNA in worst process corner cases are summarized in Table II. As it is clear, the CMCC linearization technique is effective in all corner cases and the proposed LNA has good robustness against PVT variations.

To have a better comparison a figure of merit (FoM) defined as (8) is utilized [5] in Table I.

$$FoM = \frac{Gain[\text{abs}]\times IIP3[\text{mW}]\times BW[\text{GHz}]}{(F-1)\times P_{dc}[mW]} \qquad (7)$$

where Gain is the maximum absolute power gain, F is the magnitude of the minimum noise factor over the whole frequency range and P_{dc} is the power consumption of the LNA.

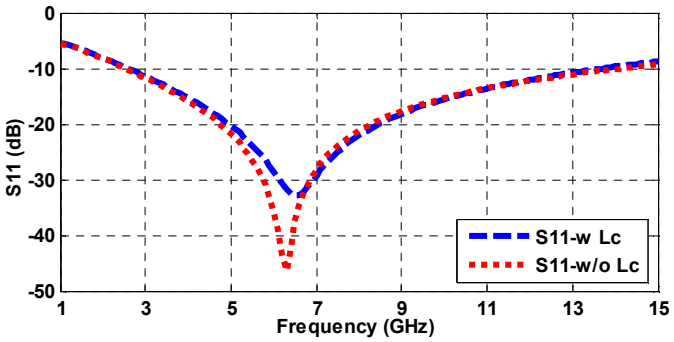

Figure 4. Input matching with and without L_C.

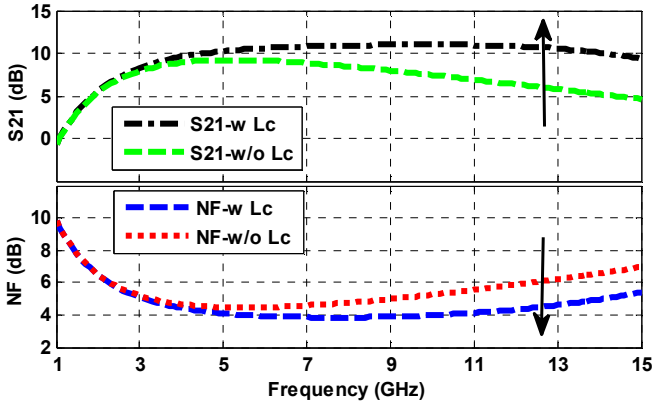

Figure 5. Simulated power gain and NF of the proposed LNA.

TABLE I. PERFORMANCE COMPARISON.

Ref.	CMOS Process	BW(GHz)	S_{11}(dB)	S_{21}*(dB)	NF**(dB)	IIP3(dBm)	IIP2(dBm)	V_{DD}(V)	Power(mW)	FoM
[8]†	130 nm	4.7-11.7	< -11.9	12.4	2.9	-3	-	1.2	13.5	4.8
[9]†	180 nm	2-6.5	< -10	11	2.7	+4.4	-	1.8	7.6	21
[10]	90 nm	2.6-10.2	< -9	12.5	3	-2.4	-	1.2	7.2	10.9
[11]†	180 nm	3.1-10.6	< -10	12.6	2.9	-4.6	-	1.8	15.2	2.3
[12]	65 nm	0.1-10	< -11.7	24	2.6	-13.5	+5	1.2	8.6	15.8
This work†	90 nm	2.6-13.7	< -10	11	3.8	+4.6	+69.3	1.2	12	24

† Simulation Result * Maximum S_{21} in BW ** Minimum NF in BW

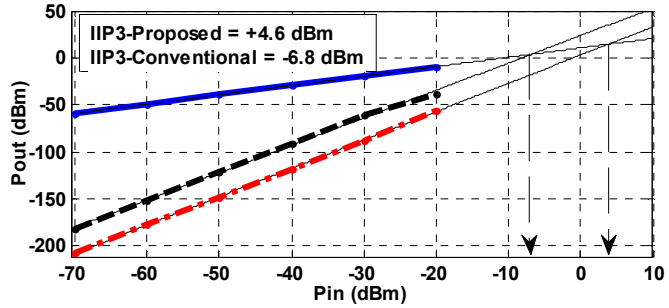

Figure 6. Simulated IIP3 at 6.5 GHz.

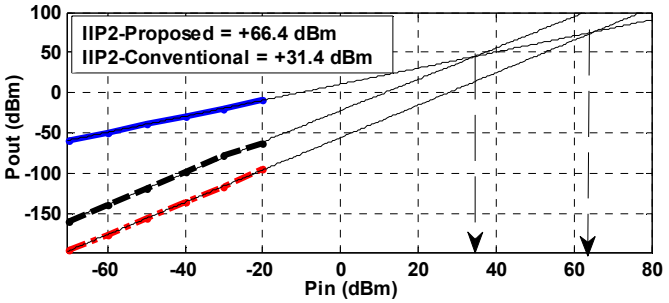

Figure 7. Simulated IIP2 at 4.5 GHz.

TABLE II. CORNER CASE SIMULATION RESULTS.

Corner Case	TT @ 27 °C	FF @ -40 °C	SS @ 85 °C
BW (GHz)	2.6-13.7	2.6-14.8	2.7-12.2
S11 (dB)	< -10	< -10	< -10
S21 (dB)	11	13.5	9.2
NF (dB)	3.8	2.6	5
IIP3 (dBm)	+4.6	+3.8	+5
IIP2 (dBm)	+66.4	+63.2	+69.8
Power (mW)	12.1	12.1	12

V. CONCLUSION

This paper presents a highly linear UWB LNA using a new linearity improvement technique to improve both linearity terms (IIP2 and IIP3) and gain without more power consumption. The proposed UWB LNA is designed and simulated in a 90 nm RF-CMOS technology. Corner case simulation results confirm the effectiveness of the proposed technique which is also proved by analysis. Compared with the prior state of the art UWB LNAs, the proposed LNA achieves good IIP2 and IIP3 without excess power consumption at the expense of slightly increased NF.

REFERENCES

[1] R. F. Ye, *et al*, "Two CMOS Dual-Feedback Common-Gate Low-Noise Amplifiers With Wideband Input and Noise Matching," *IEEE Trans. Microw. Theory Tech.,* vol. 61, pp. 3690-3699, July. 2013.

[2] M. T. Reiha and J. R. Long, "A 1.2 V reactive-feedback 3.1–10.6 GHz low-noise amplifier in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1023–1033, May. 2007.

[3] K. Lee, *et al*, "The impact of semiconductor technology scaling on CMOS RF and digital circuits for wireless application," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1415–1422, Jul. 2005.

[4] H. Zhang, X. Fan, and E. Sánchez-Sinencio, "A low-power, linearized, ultra-wideband LNA design technique," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 320–330, Feb. 2009.

[5] M. S. Mehrjoo and M. Yavari, "A Low Power UWB Very Low Noise Amplifier Using An Improved Noise Reduction Technique," *IEEE Int. Circuits Syst. Symp.,* pp. 277-280, May 2011.

[6] M. Barati, B. Mazhabjafari, and M. Yavari "A New Linearization Technique for CMOS Low Noise Amplifiers with Balun Circuitry," 21th *Iranian Conference on Electrical Engineering (ICEE)*, May 2013.

[7] D. Manstretta, M. Brandolini, and F. Svelto, "Second-order intermodulation mechanism in CMOS downconverters," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 394-406, Mar. 2003.

[8] A. Mirvakili and M. Yavari, "A noise-canceling CMOS LNA design for the upper band of UWB DS-CDMA receivers," *IEEE Int. Circuits Syst. Symp.*, pp. 217-220, May. 2009.

[9] M. S. Mehrjoo and M. Yavari, "A new input matching technique for ultra-wideband LNAs," *IEICE Electron. Express*, vol. 7, no. 18, pp. 1376-1381, Sept. 2010.

[10] G. Sapone and G. Palmisano, "A 3–10-GHz Low-Power CMOS Low-Noise Amplifier for Ultra-Wideband Communication," *IEEE Trans. Microw. Theory Tech.,* vol. 59, no. 3, pp. 678–686, Mar. 2011.

[11] J. Shim, T. Yang, and J. Jeong, "Design of low power CMOS ultra wide band low noise amplifier using noise canceling technique," *Microelectronics Journal*. vol. 44, no. 9, pp. 821-826, Sept. 2013.

[12] J. W. Park and B. Razavi, "A Harmonic-Rejecting CMOS LNA for Broadband Radios," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1072–1084, Apr. 2013.