A High Dynamic Range Differential Rectifier for RF Energy Harvesting

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***Abstract*— This paper proposes a differential rectifier for radio frequency energy harvesting systems with a high dynamic range. This architecture suggests a feedback circuit to reduce the reverse leakage current at high input power and proposes another auxiliary circuit to increase the forward current at low power. Another advantage of this architecture is sensitivity improvement. This proposed structure is Designed and simulated in 0.18 µm standard CMOS technology. The simulation results exhibit a peak Power Conversion Efficiency (PCE) of 86.78% and a dynamic range of 9.8 dBm for a PCE>80% with a sensitivity of -19.38 dBm at 1 V output across a 100KΩ resistive load.**

Keywords*— *RF energy harvesting, rectifier, dynamic range, CMOS, power conversion efficiency, RF–to-DC converter

I. INTRODUCTION

In the last two decades, energy harvesting (EH) systems have become more darling, and this is because of the fact that EH technology is an available way for powering different applications like medical implantation [1]-[3], passive radio frequency identification (RFID) [4], internet of things (IoT) sensors [5], [6] and so on. Electronics devices have been powered by batteries or wired connection to electricity, but, today, these techniques are being substituted with powering by energy harvesting systems for many reasons. The main reason is that batteries have a limited life and have to be replaced at regular times. Therefore, this replacement causes some dangerous and costly effects, especially in the medical part, so EH is a technique to enlarge battery lifetime or even substitute it entirely [6].

Researchers harvest energy from many different sources like vibration, light, heat, and radio frequency (RF) signals. RF energy is almost independent of special situations like geographical conditions, weather conditions, and time. Also, this is possible to use the same source for powering many systems. Actually, RFEH systems are formed by four parts, as shown in fig. 1. RF-to-DC Rectifiers are the heart of these systems that produce DC supply voltage by the antenna's incoming RF energy. Three essential parameters in RF-to-DC rectifiers are power conversion efficiency (PCE), sensitivity, and dynamic range (DR). The PCE is the output power ratio to the input power, and the sensitivity is the minimum amount of input RF power that needs to achieve a particular output DC voltage like 1volt; also, the DR is the range of input RF power where PCE is more than a certain percentage of its peak [7]. Another so important issue is that components such as regulators that are after this system should consume less power to deliver maximum power to the output load [8].

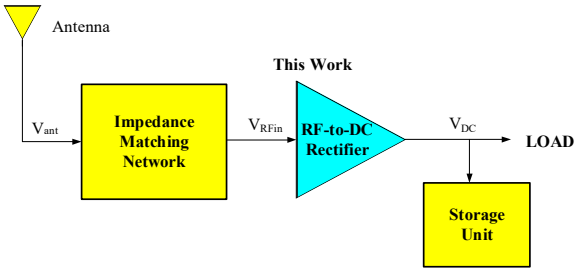

Fig. 1. Block diagram of radio frequency energy harvesting system

Nowadays, two categories of rectifiers are mostly used. Fig. 2. (a) shows the first rectifier type known as the Dickson multiplier [9], which is actually a diode-based rectifier. Diode-based rectifier realizes in CMOS technology by using a diode-connected transistor. Thus, because of the high dropout voltage in these rectifiers, they have a large dead-zone and suffer from low sensitivity and low PCE at low and medium input power. Researchers have some choices to improve Dickson rectifiers' sensitivity and PCE; one way is to replace diode-connected transistors with Schottky diodes. Schottky diodes have a low threshold voltage. With these diodes, RFEH systems could have high sensitivity and PCE at low and medium input power, but this requires some unusual costly additional fabrication steps in CMOS technology. The second way to achieve high sensitivity and PCE in these rectifiers is to add some auxiliary circuits or change some connections to compensate for transistors' threshold voltage [10].

Another type of rectifier is the cross-coupled differential-drive (CCDD) rectifier [4]. As shown in fig. 2. (b), transistors in the CCDD rectifier are designed as switches, instead of the diode-connected condition; in this case, differential RF power applies across transistors. Thanks to this situation, CCDD rectifiers have high sensitivity and PCE in low RF power. However, these rectifiers' defect is their high reverse current at high power. This deficiency causes low PCE at high incoming RF power and decreases the rectifier's DR. to compensate for this leakage, researchers add auxiliary feedback circuits to decrease reverse leakage and improve rectifier PCE at high power and enhance its DR [11]-[14].
The paper is organized as follows. Section II reviews the limitation of previous designs and compares their sensitivity, PCE, and DR. The proposed structure is introduced in Section III. Section IV presents the simulation results. At last, Section V provides the conclusion.

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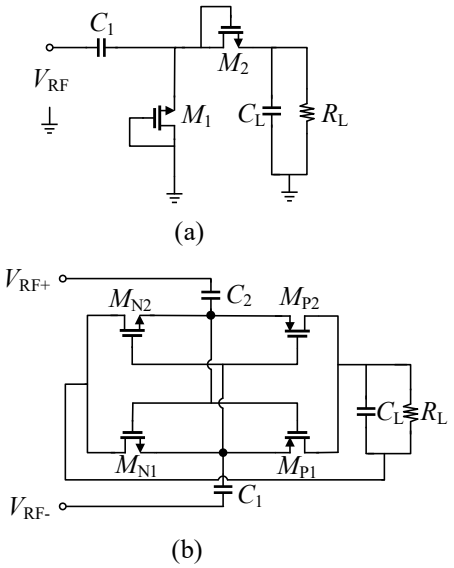

Fig. 2. (a) Dickson Rectifier [9] and (b) CCDD rectifier [4]

II. Limitation of Previous Work

A. Conventioanl CCDD Rectifier

Fig. 2. (b) shows the conventional CCDD rectifier [4]. In this structure, incoming RF power applies across the transistors differentially, helping the dead-zone area becomes small. When this circuit operates in the positive cycle, the gate of M_{N1} connects to a positive voltage, and its source connects to a negative voltage; so M_{N1} is ON in this case. Simultaneously, the gate of M_{P2} connects to a negative voltage, and its source connects to a positive voltage, so M_{P2} is ON too. In this situation, a loop appears in the circuit, and the input power is rectified and charges the output capacitor. Similarly, when the circuit operates in the negative cycle, M_{N2} and M_{P1} are ON and form the loop to charge the output capacitor. Unfortunately, at high incoming RF power, the output voltage becomes more than V_{RF+} and V_{RF-}, so the reverse leakage discharges the capacitor.

B. CCDD Rectifier Employing Feedback Circuit

As shown in fig. 3. (a), the author proposes a feedback circuit to avoid decreasing PCE at high RF power. this structure includes two transistors that sense the output voltage and divide it in a particular ratio, this ratio set with transistors sizes. As soon as this split voltage can turn on M_{N5} and M_{N6}, these transistors act as switches and connect VDD to gates of M_{P1}, M_{P2} and turn them off. With this technique, PMOS transistors are OFF at high RF power, and PCE decreasing is lesser than conventional [11]. Misfortunately, this feedback circuit has a negative effect on output power; also, this structure does not propose any way to improve forward current. fig. 3. (b) suggests a considerable resistance between the drain and gate of PMOS transistors instead of the enormous feedback circuit [12]. actually, in this research, DR is improved, but these resistances limit the forward current and cause PCE decreasing and low performance at low RF power.

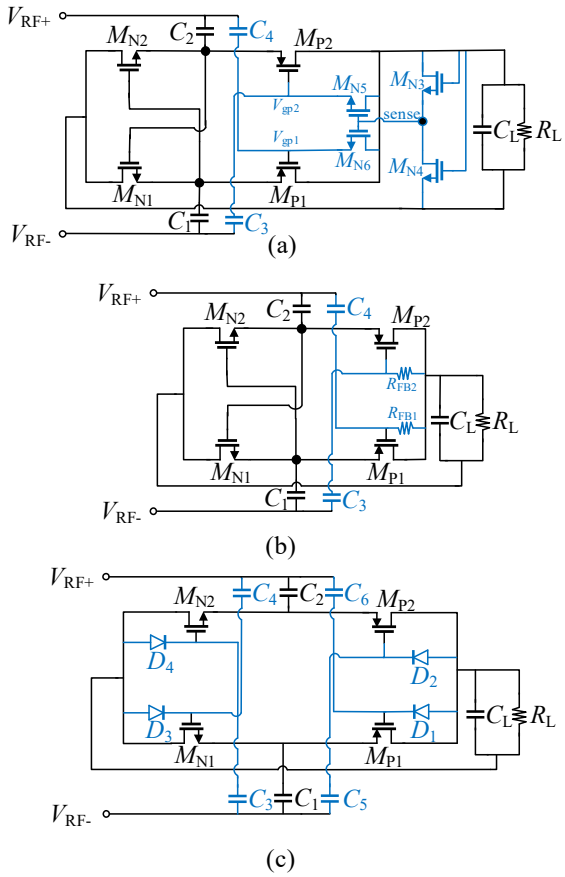

Fig. 3. Proposed CCDD rectifier in (a) [11] and (b) [12] and (c) [13]

C. CCDD Rectifier with Diode-based Feedback

An efficient solution to avoid PCE decreasing at high power without significant effect in forwarding current is to use the diode-connected transistors as a feedback network [13], [14]. Fig. 3. (c) shows diode-based feedback proposed in [13]. In this paper, high threshold diode-connected transistors are located between the PMOS transistors' gates and the output voltage. At low power, these diodes are OFF, and the rectifier operates as a conventional CCDD rectifier. On the other hand, at high incoming RF power, the output voltage becomes larger than V_{RF+} and V_{RF-} and turns on D_1 and D_2. these diodes increase the voltage of PMOS transistors' gates and turn off the PMOS transistors, so reverse current decreases [13]. This architecture is a great idea to decrease the reverse current in PMOS transistors. However, CCDD rectifiers have an almost symmetric structure, and NMOS transistors' reverse current is still a large amount. On the left side of this rectifier, D_4 and D_3 are proposed to increase forward current and improve the Rectifier's PCE, But high threshold diode-connected transistors need high input voltage to turn on and are usually OFF. Therefore, D_3 and D_4 have a negligible effect on PCE improvement.

III. Proposed CCDD Rectifier

The proposed system is shown in Fig. 4. (a). this structure is designed to enhance PCE at high RF incoming power and improve the rectifier's sensitivity by decreasing the reverse current and increasing the forward current, respectively. $D_{1\text{-}4}$ are located to be forward-biased for the output voltage and reverse-biased for the RF voltages and increase PCE at high power. In contrast, $D_{5\text{-}8}$ are located to be forward-biased for the RF voltages and reverse-biased for the output voltage, and these feedforward diodes enhance PCE and sensitivity. All of these auxiliary diodes make large DR for this architecture.

When the output voltage is larger than V_{RF+} and V_{RF-}, $D_{1\text{-}4}$ turn on. These diode-connected transistors connect DC voltage to PMOS transistors' gates and turn off these transistors to decrease their reverse current. We added these diodes to reduce PMOS transistors' reverse current, making sense that the diodes should not add extra reverse current to the circuit. According to [13], these diodes' current depends on the threshold voltage and their sizes. We have to design these diodes with a small size and a large threshold voltage to avoid reverse current increasing. In low RF power, the DC voltage is smaller than V_{RF+} and V_{RF-} so $D_{1\text{-}4}$ are OFF. $D_{5\text{-}8}$ help the rest of the circuit to improve its PCE

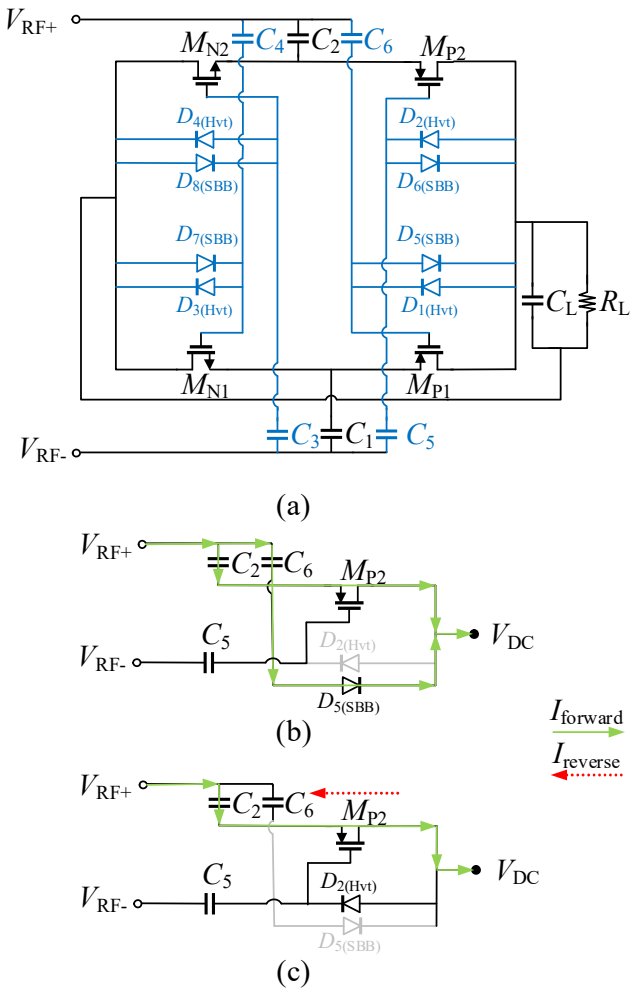

Fig. 4. (a) Proposed CCDD rectifier and steady-state operation of the rectifying devices at (b) low and (c) high input RF power.

and sensitivity at low and medium power. V_{RF+} and V_{RF-} have to be larger than $V_{DC} + V_{diode}$ to turn on $D_{5\text{-}8}$; the larger, the better; Hence, we want these diodes to have a small threshold voltage. Therefore, we can use the self-body biasing (SBB) technique and connect these transistors' bulks to their drains. We know that the threshold voltage has a relation with the source bulk's voltage.

$$V_{THP} = V_{THP0} - \gamma\left(\sqrt{2|\phi_F| + V_{BS}} - \sqrt{2|\phi_F|}\right) \quad (1)$$

Where γ denotes the body effect coefficient, and V_{bs} is the source-bulk potential difference. As shown in Figs. 5, when a PMOS diode-connected transistor works in forward biased, the drain's voltage is smaller than the source's voltage, so according to (1), the absolute value of threshold voltage decreases. In contrast, when a PMOS diode-connected transistor works in reverse biased, the drain's voltage is larger than the source's voltage. In this situation, the diode is OFF, and the new V_{SB} is zero. Therefore, the SBB technique reduces the diode's reverse current too.

Figs. 6 and 7 show the required steady-state currents and alternating charges to generate 1.5 V output DC voltage from the conventional and proposed rectifier. Both rectifiers need equal net charges to make an equal output voltage for the same load, as expected. However, The magnitude of alternating charges in the conventional rectifier is significantly larger in comparison with the Proposed rectifier.

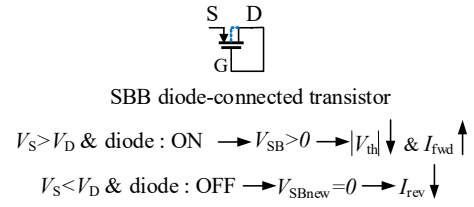

Fig. 5. SBB diode-connected transistor in ON and OFF situation

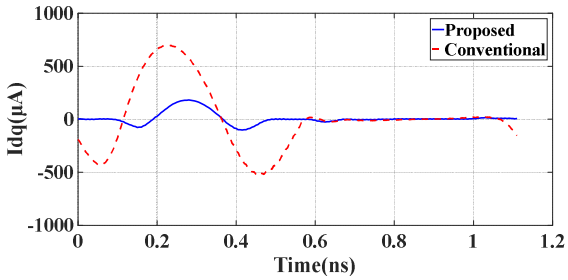

Fig. 6. Steady-state currents of MP2 in the conventional and proposed rectifier to produce 1.5v output DC voltage

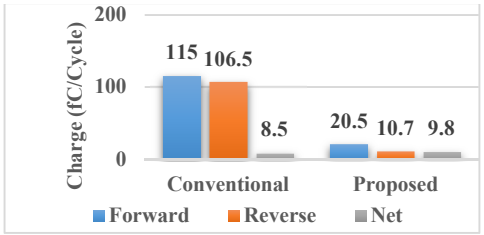

Fig. 7. Alternating Charges per cycle in the conventional and proposed rectifier to produce 1.5v output DC voltage.

IV. Simulation Result

The proposed structure is carried out with Spectre RF using 180 nm RF-CMOS technology to find the proposed rectifier's performance. The rectifier is simulated at the frequency of 900 MHz. The poly resistor and MIM capacitors are used for resistor and capacitors, respectively.

Fig. 8 shows the PCE of the conventional and proposed circuits. The simulation results exhibit a peak PCE of 86.78% and a DR of 9.8 dBm for a PCE>80% across a 100KΩ resistive load. Furthermore, fig. 9 illustrates the conventional and proposed circuits' output voltages, and we can realize that the proposed circuit sensitivity is -19.38 dBm at 1 V output across a 100 KΩ resistive load. Figs. 10 and 11 show the circuit's PCE and the output voltage in the worse process corner cases. Figs. 12 and 13 illustrate the output voltage and PCE for 30kΩ and 80kΩ loads; hence, the proposed rectifier operates efficiently for the extensive range of the load.

Table 1 summarizes the circuit's essential parameters in the corner cases. Also, Table 2 states a comparison between the proposed rectifier and some of the previous CCDD rectifiers. The proposed rectifier achieves higher PCE, larger DR, and better sensitivity than other work in this table. Reference [4] shows a high peak PCE at high input power, but it has poor sensitivity and DR. Reference [14] illustrates a good peak PCE and sensitivity; however, our proposed rectifier has better PCE and sensitivity and higher DR. Design parameters are collected in Table 3.

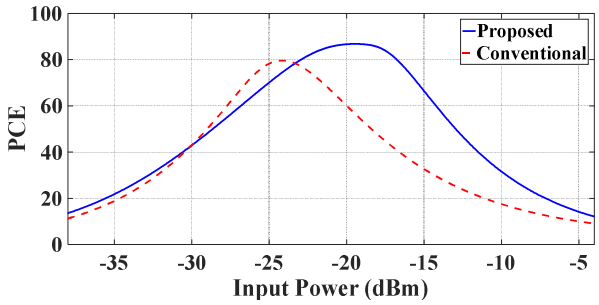

Fig. 8. Simulated PCE for the proposed and conventional rectifiers

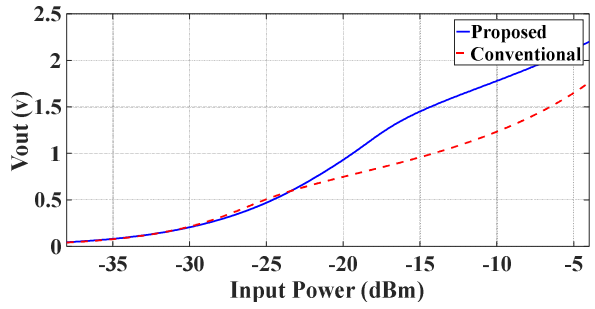

Fig. 9. Simulated output voltage for the proposed and conventional rectifiers

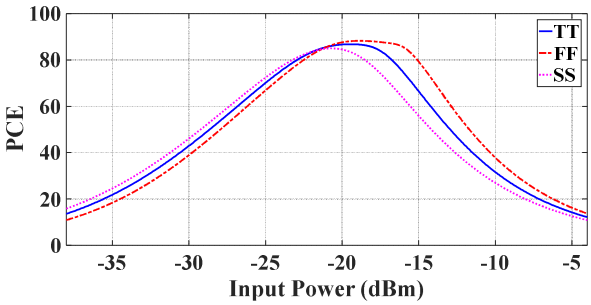

Fig. 10. Simulated output voltage for the proposed and conventional rectifiers

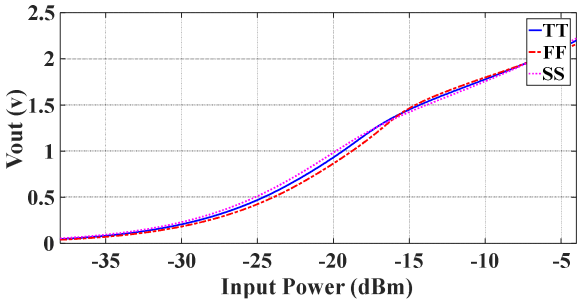

Fig. 11. Simulated output voltage in the worse process corner cases

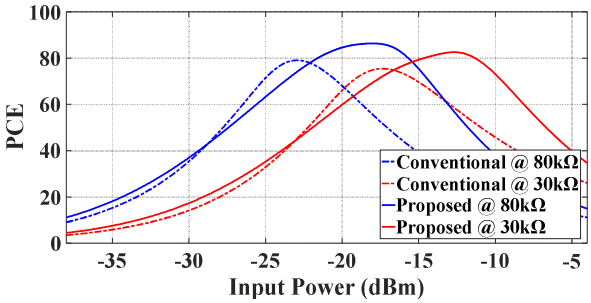

Fig. 12. simulated PCE of the proposed and conventional rectifiers in different loads

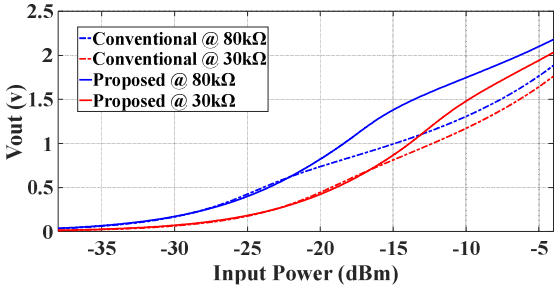

Fig. 13. simulated output voltage of the proposed and conventional rectifiers in different loads

Table 1. Corner case simulation results

Corner case	TT @ 27°C	SS @ 85°C	FF @ -40°C
Peak PCE	86.78%	85%	88.25%
Sensitivity (dBm) @ V_{DC} =1 volt	-19.38	-19.8	-18.8
DR (dB)	9.8	9.2	10.4

Table 2. Performance Comparison

Ref.	Architecture	CMOS process	Frequency (MHz)	Number of stages	Peak PCE	Sensitivity @ V_{DC}=1 volt	DR	R_{Load} (KΩ)
Proposed *	**Diode feedback and feedforward rectifier**	**180 nm**	**900**	**1**	**86.78%**	**-19.38 dBm**	**9.8 dB**	**100**
Conventional *	Standard CCDD rectifier	180 nm	900	1	81.63%	-14.1 dBm	6.3 dB	100
[4] JSSC '09	Standard CCDD rectifier	180 nm	953	1	86.2%**	-13 dBm**	6 dB**	100
[11] MWCL '16	Adaptive rectifier	180 nm	900	1	65%	-18 dBm	6.6 dB	100
[12] TCAS II '17	Self-biased	180 nm	433	1	51.5%	-17 dBm	7.9 dB	100
[13] MTT '18	Double-sided	180 nm	900	1	66%	-18.2 dBm	6.8 dB**	100
[14] TCAS II '19	Shared-capacitor coupling	130 nm	900	3	83.7%	-19.2 dBm	6.7 dB**	100
[15] * **IET '19**	Using thick-oxide transistors	180 nm	900	2	75.2%	-17 dBm	5.6 dB**	100
[16] * **WPTC '17**	DC-boosted biasing	65 nm	2450	2	59.6%	-17 dBm***	8.2 dB**	29

* Simulation results ** Estimated from the figure *** $R_{Load}= \infty$

Table 3. Designed values of the proposed rectifier

parameter	Size	parameter	size
$M_{P3,4}$	8.8µm/180nm	D_{5-8}	220nm/20µm
$M_{N1,2}$	1.76µm/180nm	C_L	0.5pF
D_{1-4}	220nm/500nm	R_L	100kΩ

V. CONCLUSION

This paper presents an architecture that reduces leakage current at high power and encreases forward current at low power. Auxiliary diodes act as feedback and feedforward and improve the circuit's PCE and DR. Also, the proposed rectifier operates efficiently for the extensive range of the load. Simulated in a 180 nm CMOS technology, the proposed rectifier achieves a peak PCE of 86.78% and a DR of 9.8 dBm for a PCE>80% with a sensitivity of -19.38 dBm at 1 V output across a 100 KΩ resistive load.

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