AN ANALYTICAL MODEL FOR THE SLEWING BEHAVIOR OF CMOS TWO-STAGE OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS

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ABSTRACT

This paper presents a complete time-domain model for the slewing behavior of CMOS two-stage operational transconductance amplifiers (OTAs). In this model, the effects of both first and second stage currents are included. An analytical expression is given in terms of the compensation capacitance, load capacitance and device sizes for each positive and negative slew rates. HSPICE simulation results are provided to show the validity of the proposed models using a 0.35-μm CMOS technology. These models show near perfect agreement with simulation results.

1. INTRODUCTION

Recently, design of high-speed and low-power OTAs is becoming more challenging due to new technology feature size scaling and reducing of the power supply voltage. Design of low-power and fast settling OTAs is needed to model some of their parameters such as the slew rate. These models must be simple with sufficient accuracy to help the circuit designers.

Switched-capacitor circuits have many benefits over the continuous-time circuit implementation techniques. In these circuits, the charge on a capacitor is transferred to another capacitor during a definite time period. The charge transfer between capacitors requires an OTA whose major role is to create a virtual ground at its inputs to transfer the charge completely. Changing of OTA's output voltage occurs in two different manners called the linear settling and non-linear settling or selwing. Linear settling depends on the OTA's unity gain bandwidth while slewing is defined by a parameter called the slew rate. Slewing occurs when one of the input signals are large than the other. During this period one of the input transistors are switched off. So, the total settling time is made up of two distinct regions: a slewing period (T_{SL}) and a settling period (T_{ST}) [1-3]. During the slewing period the OTA behaves as a non-linear device, forcing its output to follow the input.

Slewing of an OTA is a large signal characteristic; therefore a small-signal analysis in the s-domain cannot be used [1]. A two-stage OTA with NMOS input differential pair as shown in Fig. 1 is considered in this paper. The extension of the obtained models for PMOS input pair is straightforward. It is worth to mention that this architecture has been chosen for its simplicity and the results can be extended to the other two-stage structures without much effort [1].

For positive slew rate as shown in [1], the output voltage is given by:

$$V_o^+(t) = \frac{I_1}{C_c}t - \gamma \tanh\left(\frac{1}{2}\frac{\gamma k_5}{C_L}(t+t_0)\right) + V_o^+(0^+) \qquad (1)$$

where

$$\sigma = \sqrt{\frac{2I_2}{k_5}} + R_C I_1, \quad t_0 = \frac{C_L}{\gamma k_5}\ln\left(\frac{\gamma+\sigma}{\gamma-\sigma}\right)$$
$$\gamma = \sqrt{\frac{2I_0}{k_5}}, \quad I_0 = I_1 + I_2 + \frac{C_L}{C_C}I_1, \quad k_5 = \mu_P C_{OX}\left(\frac{W}{L}\right)_5. \qquad (2)$$

Similarly for negative slew rate it is as follows:

$$V_o^-(t) = -\frac{I_1}{C_C}t - \gamma' \tanh\left(\frac{1}{2}\frac{\gamma' k_5}{C_L}(t+t_0')\right) + V_o^-(0^+) \qquad (3)$$

where

$$\sigma' = \sqrt{\frac{2I_2}{k_5}} - R_C I_1 \quad t'_0 = \frac{C_L}{\gamma' k_5}\ln\left(\frac{\gamma'+\sigma'}{\gamma'-\sigma'}\right)$$
$$\gamma' = \sqrt{\frac{2I_0'}{k_5}} \qquad I_0' = I_2 - I_1\left(1+\frac{C_L}{C_C}\right). \qquad (4)$$

Using the approximation of $1 - \tanh(x) = 2\exp(-2x)$, when x is large, SR can be obtained as follows [1]:

$$SR_1^+ = \frac{I_1}{C_c} - \frac{2\gamma}{T_{SL}}\frac{\sigma-\gamma}{\sigma+\gamma} \tag{5}$$

$$SR_1^- = -\frac{I_1}{C_c} + \frac{2\gamma'}{T_{SL}}\frac{\sigma'-\gamma'}{\sigma'+\gamma'} \tag{6}$$

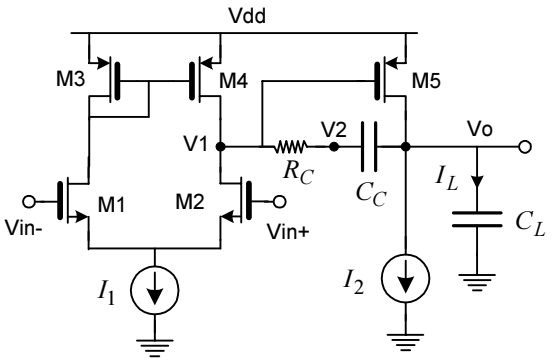

Figure 1: Single-ended CMOS two stage OTA.

Although this model shows good agreement with simulation results, it can be used only when

$$I_2 > (1+\frac{C_L}{C_C})I_1. \tag{7}$$

Because, it is needed to ensure that I_0' to be positive. So, a high current in the second stage is required due to existence of large load capacitances in many switched-capacitor circuits. The positive slew rate in two-stage OTAs with NMOS input diff pair can be obtained with relation (5). But, the negative slew rate cannot be shown with (6) as proposed in [1] for all values of the first and second stage currents. Therefore, a new model is presented to predict the negative slew rate when the above-mentioned condition could not be satisfied.

This paper presents an analytical approach on the slew rate of a CMOS two-stage OTA in the time domain. The paper is organized as follows. Section (2) presents a novel time domain model for the negative slew rate. In section (3) HSPICE simulation results are provided to show the validity of the proposed model. Section (4) concludes the paper.

2. MODIFIED SLEW RATE ANALYSIS

If I_2 is not high enough to support both I_1 and I_{D5} as V_{in} experiences a large negative step, the drain voltage of M4, V_1, increases so as to turn off the transistor M5. As drain voltage of M4 increases, the absolute value of drain-source voltage of M4 decreases. So, M4 will be forced to operate in the triode region. The key point to write the equations needed to obtain the second stage slew rate is as follows. When M4 enters the triode region, the current that flows through the compensation capacitance is no longer constant. So, it will be a function of V_1. The circuit can be simplified as shown in Fig. 2 to obtain the negative slew rate.

The node equations of the circuit in the time domain are as follows:

$$I_{12}(t) = k_4 V_{eff4}\left(V_{dd} - V_1(t)\right) \tag{8}$$

$$\frac{V_2(t)-V_1(t)}{R_c} + C_c\frac{d\left(V_2(t)-V_o(t)\right)}{dt} = 0 \tag{9}$$

$$C_c\frac{d\left(V_o(t)-V_2(t)\right)}{dt} + I_2 + C_l\frac{d\left(V_o(t)\right)}{dt} = 0 \tag{10}$$

$$V_1(t) - V_2(t) = R_c I_{12}(t) \tag{11}$$

where

$$V_{eff4} = \sqrt{\frac{2I_1}{k_4}}, \quad k_4 = \mu_P C_{OX}(\frac{W}{L})_4 \tag{12}$$

and I_{12} denotes the current that flows from node V1 to node V2 shown in Fig. 1. The initial conditions for these equations are as follows:

$$V_1(0^+) = V_{dd} + V_{THP} - V_{eff4} + R_C I_{12}(0^+). \tag{13}$$

Using Math simulation tools such as MAPLE to solve the equations (8-11) with initial condition of (13), the output voltage can be shown to be as follows:

$$V_o^-(t) = -\frac{I_2}{C_L+C_C}t - \frac{a.p}{h}\exp(-\frac{h}{p}t) + V_o^-(0^+) \tag{14}$$

where

$$h = V_{eff4}k_4(C_L+C_C) \tag{15}$$

$$p = |C_L C_C(R_C k_4 V_{eff4} - 1)|. \tag{16}$$

The value of a can be obtained using the following relation:

$$I_{12}(0^+) = k_4 V_{eff4}\left(V_{dd} - V_1(0^+)\right). \tag{17}$$

So, it will be:

$$a = -\frac{C_C I_2}{C_L(C_L+C_C)} + \frac{C_C(I_1 - k_4 V_{eff4}V_{THP})}{p}. \tag{18}$$

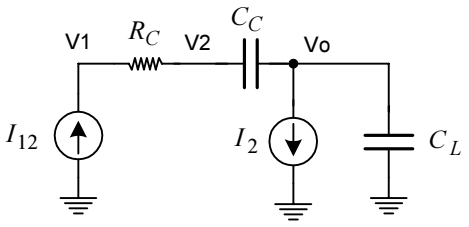

Figure 2: Equivalent circuit for negative slew rate calculation.

Similar analysis can be performed for two-stage OTAs with PMOS input differential pairs. It is worth to mention that the positive slew rate can be obtained similar to the negative slew rate approach. The output voltage will be as follows:

$$V_o^+(t) = \frac{I_2}{C_L + C_C} t - \frac{a'.p'}{h'} \exp(-\frac{h'}{p'} t) + V_o^+(0^+) \qquad (19)$$

where

$$a' = \frac{C_C I_2}{C_L (C_L + C_C)} + \frac{C_C (I_1 - k_4' V_{eff4} V_{THN})}{p'}. \qquad (20)$$

$$h' = V_{eff4}\, k_4' (C_L + C_C) \qquad (21)$$

$$p' = |\, C_L C_C (R_C k_4' V_{eff4} - 1)\,|\,. \qquad (22)$$

$$k_4' = \mu_n C_{ox} (\frac{W}{L})_4 \qquad (23)$$

The slew rate of an OTA is given by the derivative of its output voltages with respect to time *t*. The output voltage as shown in the relation (14) is itself a function of time. Therefore the effective slew rate is defined as $SR = \big(V_o(T_{SL}) - V_o(0)\big)/T_{SL}$ is a more useful quantity, where T_{SL} is the time it takes the output voltage to change from its original value to the value when the OTA enters the linear region [1]. So, the negative slew rate of NMOS input differential pair two-stage OTAs can be derived as follows:

$$SR_N^- = -\frac{I_2}{C_L + C_C} + \frac{C_C}{T_{SL} h} (q_N - \frac{I_2 p}{C_L (C_L + C_C)}) \qquad (24)$$

where the exponential terms in the resulted slew rates were neglected and

$$q_N = I_1 - k_4 V_{eff4} V_{THP}. \qquad (25)$$

Similarly, the positive slew rate of a two-stage OTA with PMOS input differential pair will be as follows:

$$SR_P^+ = \frac{I_2}{C_L + C_C} + \frac{C_C}{T_{SL} h'} (q_P + \frac{I_2 p'}{C_L (C_L + C_C)}) \qquad (26)$$

$$q_P = I_1 - k_4' V_{eff4} V_{THN}\,. \qquad (27)$$

These relations show that the effective negative slew rate in a two-stage OTA with NMOS input transistors is not only a function of I_2, C_L and C_C, but is also a function of I_1 and k_4. Additionally, the effective slew rate is less or more than the value is predicated by the simple equation $I_2 / (C_C + C_L)$, depending on the circuit parameters and bias conditions. Another important property that can be derived from (24) and (26) is that the effect of the load capacitance and compensation capacitances are not the same. In general, if the sum of compensation and load capacitances is constant, the larger compensation capacitance leads to a higher T_{SL}, which is not desired. Also it can be concluded that with proper values of k_4, slew rate can be simplified to the conventional model $I_2 / (C_C + C_L)$ which used in many papers and text books [4, 5].

3. SIMULATION RESULTS

In order to show the validity of the proposed model for slew rate in a CMOS two-stage OTA circuit level simulation with HSPICE are provided using a BSIM3v3 level 49 0.35-µm CMOS technology. The OTA shown in Fig. 1 was simulated with design parameters as shown in Table 1 for a simple switched-capacitor circuit. The results are shown in Figs. 3, 4, and 5 for several values of compensation and load capacitances, the first stage current I_1 and the second stage current I_2. It is worth to mention that in the calculation of slew rate proposed by analytical model in this paper in relations (24) and (26), T_{SL} was replaced by those were obtained from circuit level simulation results. It should be noted that these equations can be also useful to find the exact values of the first and second stage currents with a defined slew rate and T_{SL}. The simulation results show the usefulness and validity of the proposed model. It has an excellent agreement with simulation results. Also these results show that the slew-rate can be more or less than the conventional model used in most books and literatures. The proposed model has a perfect agreement for wide range of the circuit parameters.

Table 1: Circuit parameters

Parameter	Value
$(W/L)_{1,2}$	100/0.35
$(W/L)_{3,4}$	100/0.35
$(W/L)_5$	200/1
R_C	1 kΩ
V_{dd}	3-V

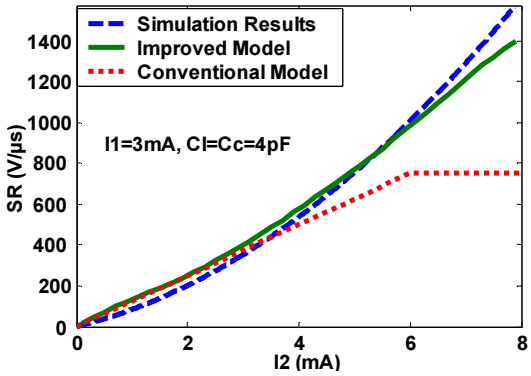

Figure 3: Slew Rate vs. I_2 with I_1=3mA

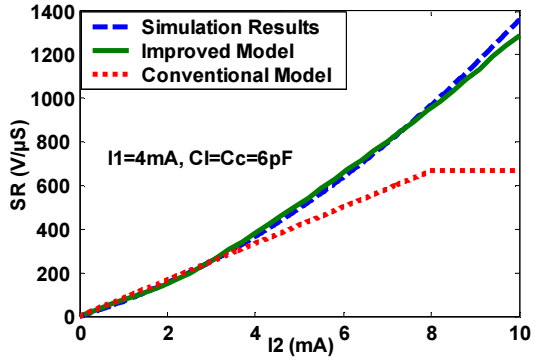

Figure 4: Slew Rate vs. I_2 with I_1=4mA

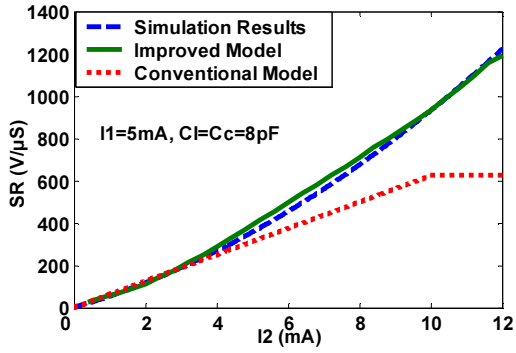

Figure 5: Slew Rate vs. I_2 with I_1=5mA

4. CONCLUSION

A novel time-domain analysis of slew-rate in CMOS two-stage OTAs was presented in this paper. The previous analytical model suffers from several conditions imposed on bias currents and device sizes. The models proposed in this paper work on a wide range of the circuit parameters such as the first and second stage currents, load and compensation capacitances, and the device sizes. They are applicable for most design parameters and can be simplified to the conventional model with proper selection of device sizes. The models are in good agreement with simulation results shown in circuit level simulators.

5. REFERENCES

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