Multirate Double-Sampling Hybrid CT/DT Sigma-Delta Modulators for Wideband Applications

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***Abstract*— As the sampling frequency in modulators is upper limited by the amplifier bandwidth and power consumption, sigma-delta modulators should operate with low oversampling ratios (OSRs) in broadband applications. But, the modulator accuracy is reduced by lowering the OSR. Multirate signal processing and double-sampling have been proven appropriate techniques for preventing this effect and also lowering the power consumption in discrete-time modulators. In this paper, both of these techniques are simultaneously used to achieve power efficient hybrid CT/DT sigma-delta modulators.**

I. INTRODUCTION

Continuous-time (CT) modulators have received increasing attention over the last years due to their higher sampling rate capability over the discrete-time (DT) counterparts. In DT implementations, a unity gain bandwidth (GBW) about one order of magnitude higher than the sampling frequency is required, but now, this could be relaxed to a factor of 1.25-3 by using the CT ones [1]. In practice there exist some non-idealities which make CTs hard to realize the theoretical systems in an integrated circuit, among them large variations of the integrator's time constants, high sensitivity to clock jitter and excess loop delay (ELD) [1]. Recent approaches have been drawn to the hybrid ΣΔ modulators featuring the integration of initial stage(s) in the loop filter as CT integrator(s) and the subsequent stages as DT integrators [1], [2]. These hybrid modulators are suitable for high speed applications.

For sigma-delta modulators there is a trade-off between the oversampling ratio (OSR) and the modulator's order. Increment in OSR leads to the SNDR improvement, but for a fixed nyquist rate, doubling the OSR generally translates into opamps that are roughly twice as fast. So, in order to employ ΣΔ modulators in broadband applications, low OSRs should be used. But, the modulator accuracy is reduced by lowering the OSR. Consequently, novel modulator structures are needed to alleviate the reduction of resolution in low OSR applications.

A useful approach for handling DT modulators in broadband applications is to employ the double-sampling technique [3]. In this method, the integrator circuit operates during both phases of the clock. Hence, the effective sampling frequency of the system is twice that of the clock frequency. This results in doubling the OSR or the available time for settling of the integrators if the OSR and input signal bandwidth are fixed. Another technique is to use multirate signal processing. In high-speed modulators, opamps are operated near their maximum bandwidth, so as addressed in [4] power consumption dramatically increases with sampling frequency. An example can be seen in [4], where two modulators with similar performances were built in the same technology. The implementation which used OSR=16, achieving more than a 70% of power saving than the one used OSR=24. It was shown by [5] that using different OSRs along the structure of a modulator can alleviate some of the major problems faced in high-speed designs.

In this paper, by using the merits of both multirating and double-sampling, a new class of hybrid modulators called multirate double-sampling cascaded ΣΔ modulators (MDC-SD) is proposed for broadband applications. In section II we describe the derivations of the proposed modulator structure. Section III provides the behavioral simulation results and addresses the effect of the circuit non-idealities. All simulations have been carried out in the time domain using MATLAB-Simulink. The conclusions are given in Section IV.

II. MULTIRATE DOUBLE-SAMPLING ΣΔ MODULATORS

The noise of each succeeding stage of a cascaded modulator, when referred to the modulator input, is shaped by the preceding stages. Therefore, the requirements on the second stage noise cancellation are much relaxed than those from the first stage. So, usually only the first stage in a cascaded modulator requires special design considerations and it determines the power consumption of the full converter. In order to reduce the power consumption of a cascaded ΣΔ modulator both the multirate signal processing and double-sampling can be used. In a MDC-SD modulator the first stage operates at a low sampling rate, f_{s1}, while the rest of stages operates at a high sampling frequency, $f_{s2} = N \times f_{s1}$, where N is the *OSR* increment in the last stages of the modulator.

Figure 1 shows the proposed hybrid CT/DT cascade 2-2 modulator with 4 bit internal quantizers. In the analog part, the only difference between the conventional cascade 2-2 modulator and the proposed modulator in Fig. 1 is in the interpolator located between the modulator stages. The simplest implementation of an interpolator has been selected, as it merely maintains the input signal for N clock cycles, not requiring any additional hardware.

It will be shown later that a system working in multirate mode has an equivalent single-rate system works at the *OSR* of between OSR_1 and OSR_2 while consuming less power. This can be interpreted from (1). The inband quantization noise power of an Lth-order ΣΔ modulator with M stages is given by [5]:

$$IBN \propto \frac{\pi^{2L}}{(2L+1)} \frac{\Delta^2}{OSR_1^{2L_1} OSR_2^{2L_2} \ldots OSR_M^{2L_M+1}} \qquad (1)$$

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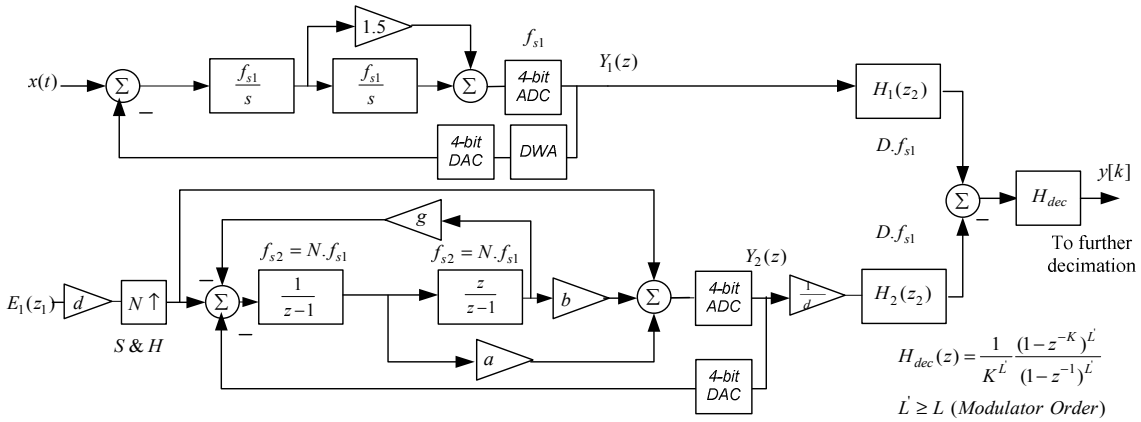

Figure 1. Proposed multirate double-sampling hybrid CT/DT cascade 2-2 ΣΔ modulator

where Δ is the quantization step, and L_i and OSR_i are the modulator's order and the oversampling ratio of the i^{th} stage, respectively. Note that concerning the power consumption, only the analog portion of the modulator is considered since as technologies are scaling down, the contribution of the digital part on the total power consumption decreases significantly.

Note that in our design, when we just use double-sampling, both stages work in the same sampling rate. In this case, the S/H interpolation block placed between the stages is removed and also parameter N is set to 1 in the second stage. However, the effective sampling frequency of the second stage is twice that of the whole system clock frequency. This results in doubling the effective OSR of the second stage (D = 2). So, digital filters in the cancellation logic must operate in higher sampling rate, i.e. $f_s = D \times f_{s1}$.

The proposed cascade 2-2 modulator shown in Fig. 1 is designed as follows. The first step in the design procedure is to find initial stable NTFs. For the first stage we choose a simple FIR NTF in order to realize digital filter of second stage easily. In the second stage, the situation is different and a unity STF is adopted. The noise transfer function of the second stage is given by:

$$NTF_2 = \frac{z^2 - (2-g)z + 1}{z^2 - (2-g-a-b)z + 1 - a} \tag{2}$$

To match (2) with FIR NTF, the parameter values a =1, b=1-g and g = 2- 2(cos(α)) must be chosen. This results in:

$$NTF_2 = 1 - 2(\cos\alpha)z^{-1} + z^{-2} \tag{3}$$

Now, we design the first stage (continuous-time integrators) of the modulator. There are two main techniques for designing CT NTF. One is based on the design of a DT modulator first, from which an equivalent CT ΣΔ modulator is computed afterwards. The other one is based on a full design in CT domain. We choose the first methodology because good techniques and tools exist in DT domain [6]. As mostly used in recent designs because of some advantages such as less sensitivity to clock jitter, we adopt CIFF (Cascade of Integrators Feedforward) architecture for the first stage. We choose the DT NTF_1 as follows:

$$NTF_1 = (1 - z^{-1})^2 \tag{4}$$

In [6] the method of equivalent loop filters has been applied to convert DT modulators into their CT counterpart. The main idea was to convert every existing loop filter from the DT to the CT domain. Therewith exactly the same modulator output spectrum could be obtained. We follow the same procedure for converting (4) to its CT counterpart. Result is the second order, first stage of Fig.1. The next step is to compensate the excess loop delay without influencing the NTF. A way to compensate this effect is to insert an intentional delay in the feedback path of the modulator [7]. Compensating ELD has been considered in our design as proposed by [8] (see Fig. 2).

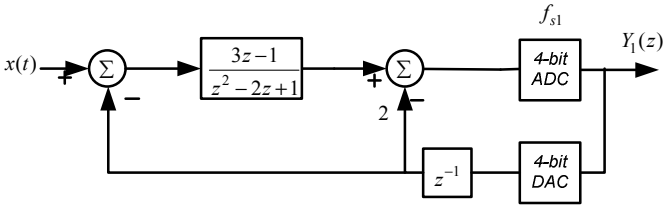

Figure 2. The DT equivalent of first stage with an intentional delay

In the proposed design, the DAC feedback pulse shape is chosen considering clock jitter sensitivity, required BW, and slew rate of the op-amps. The use of a decaying waveform minimizes the jitter influence, while the op-amp power is increased due to increased slew rate [6]. Therefore, the NRZ DAC shape can be used for low power consideration and reasonable jitter tolerance. For further reduction of clock jitter sensitivity, multibit internal quantizer is used. Equation (5) shows that in-band noise can be reduced with more internal DAC levels. In (5), $A_{NRZ,MB}$ approximately equals to 1 [6].

$$IBN_{\sigma_t} = \frac{{V_{FS}}^2}{(2^{B_{\text{int}}} - 1)^2} \left(\frac{\sigma_t}{T_s}\right)^2 \frac{A_{NRZ,MB}}{OSR} \tag{5}$$

The synthesis of DT multirate modulators and the corresponding digital filters has been shown in [5] and can be done similarly. The result for the digital filters of Fig. 1 is:

$$\begin{aligned} H_1(z_2) &= STF_2(z_2) = 1 \\ H_2(z_2) &= NTF_1(z_2) = (1 - {z_2}^{-D})^2 \end{aligned} \tag{6}$$

where z_1 and z_2 correspond to the low and the high sampling rates, respectively, and $z_1^{-1} = z_2^{-D}$.

With regard to selected NTFs, the contribution of the second quantization error to the overall output of MASH in the case of single-rate modulators is then:

$$\begin{aligned} Y|e_2 &= -\frac{NTF_2 H_2(z_2)}{d} \\ &= -\frac{(1-z^{-1})^2 (1-(2-g)z^{-1} + z^{-2})}{d} \end{aligned} \tag{7}$$

Now a pair of complex conjugate zeros is introduced in the overall NTF whose location depends on the coefficient g. Optimal value of g for maximizing the SNDR is obtained as follows [9]:

$$g_{opt} = \frac{2\sin\frac{3\pi}{OSR} - 18\sin\frac{2\pi}{OSR} + 90\sin\frac{\pi}{OSR} - \frac{60\pi}{OSR}}{24\sin\frac{\pi}{OSR} - 3\sin\frac{2\pi}{OSR} - \frac{18\pi}{OSR}} \tag{8}$$

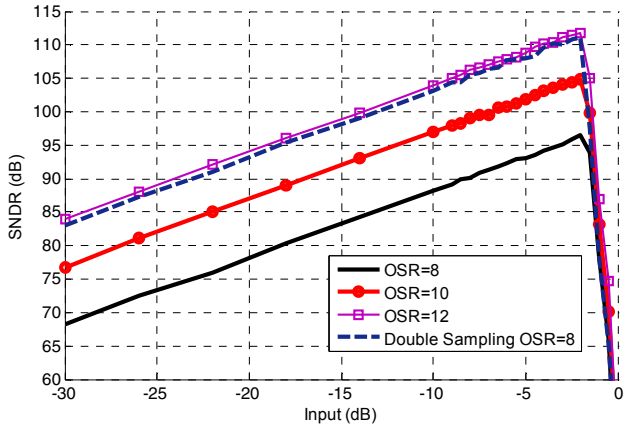

Figure 3. SNDR vs. input signal amplitude for cascade 2-2 ΣΔ modulators.

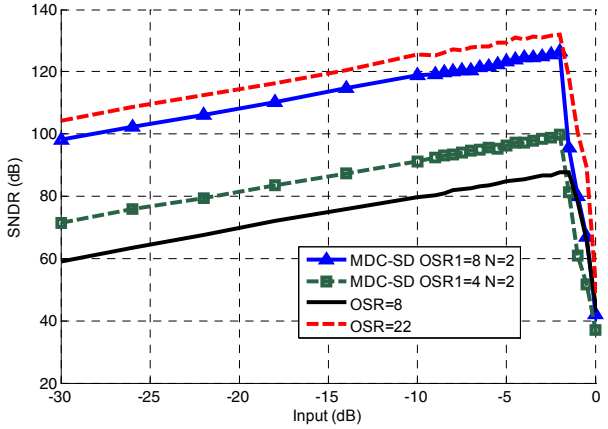

Figure 4. SNDR of cascade 2-2 and proposed MDC-SD ΣΔ modulators.

Like in single-rate architectures, optimal value of g can be found in the case of multirate systems. When the second stage of the modulator uses double-sampling technique, optimization gives rise to:

$$g_{opt} = (8\sin\frac{\pi}{OSR_2} + 16\sin\frac{2\pi}{OSR_2} - 2\sin\frac{4\pi}{OSR_2} - 4\sin\frac{3\pi}{OSR_2} + 0.8\sin\frac{5\pi}{OSR_2} - \frac{24\pi}{OSR_2}) / (8\sin\frac{2\pi}{OSR_2} - \sin\frac{4\pi}{OSR_2} - \frac{12\pi}{OSR_2}) \quad (9)$$

Similarly optimal value of g in the case of MDC-SD modulator when $D = 4$ is then:

$$g_{opt} = (24\sin\frac{\pi}{OSR_2} + 8\sin\frac{4\pi}{OSR_2} - \sin\frac{8\pi}{OSR_2} - \frac{16}{3}\sin\frac{3\pi}{OSR_2} - \frac{16}{5}\sin\frac{5\pi}{OSR_2} + \frac{4}{7}\sin\frac{7\pi}{OSR_2} + \frac{4}{9}\sin\frac{9\pi}{OSR_2} - \frac{24\pi}{OSR_2}) / (4\sin\frac{4\pi}{OSR_2} - 0.5\sin\frac{8\pi}{OSR_2} - \frac{12\pi}{OSR_2}) \quad (10)$$

Note that in the case of multirating, the optimal value of g depends on OSR_2.

III. Simulation Results and Discussions

Now we begin to simulate our proposed systems: double-sampling hybrid ΣΔ modulator and MDC-SD structure. Due to the motivation to build wideband ΣΔ modulators, the *OSR* in the first stage is limited to 8. To be able to see the advantages of MDC-SD modulators in broadband applications adequately, the single-rate structures with different *OSR*s and signal bandwidth of 10MHz will be compared to them. In the simulations, ideal DAC unit elements have been assumed. However, in the real implementations, dynamic element matching techniques such as the data weighted averaging (DWA) algorithm can be used to correct the DAC errors [10].

The SNDR versus the input signal level of the double-sampling hybrid architecture is shown in Fig. 3. Four systems were simulated and compared to each other. Three single-rate modulators with *OSR* = 8, 10, 12 and double-sampling hybrid modulator with *OSR* = 8. One can investigate and find from (1) that the performance of the proposed double-sampling hybrid ΣΔ modulator operating at fs = 2×8×10 = 160MHz is approximately equals to the performance of the conventional modulator operating at fs = 2×12×10 = 240MHz. This fact is also clear from Fig. 3. This result shows that using double-sampling in the second stage of hybrid ΣΔ modulator can be lead to significantly power saving.

Similarly, Fig. 4 shows the SNDR for different cascade 2-2 modulators. Note that the SNDR for a MDC-SD modulator with $OSR_1 = 8$ and $N = 2$ ($D = 4$) is approximately equal to the SNDR of

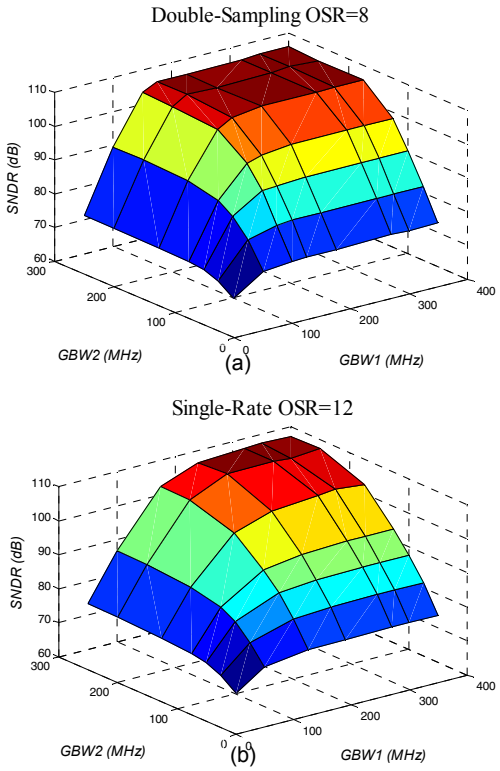

Figure 5. SNDR vs. GBW of different integrators, (a) Double-Sampling modulator. (b) Single-Rate modulator.

the conventional modulator operating at the *OSR*=22. This can be also proved by (1). As mentioned before, because of using double-sampling in our structure, the parameter N set to 2 but digital filters work in sampling rate of fs = 4×2×10×8 = 640MHz. This result shows that a reduction in the *OSR* of the first stage modulator can be compensated for increase in the *OSR* of the last stages, whose effects on power consumption are not so critical. Fig. 4 also shows that SNDR of a MDC-SD modulator with $OSR_1 = 4$ and $N = 2$ is similar to the SNDR of the single-rate modulator with *OSR* = 8.

Required GBWs for the first stage integrators in two cases (double-sampling modulator and single-rate architecture) are shown in Fig. 5. Input signal level is -7.7dB. Results are also summarized in table I. As it is clear, although double-sampling hybrid modulator with *OSR*=8 and single-rate one with *OSR*=12 have the same performance,

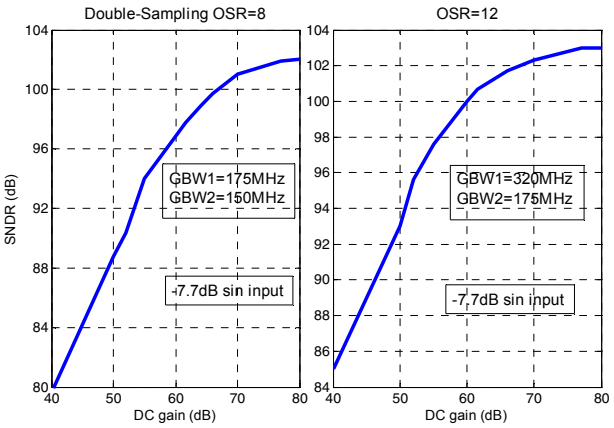

Figure 6. SNDR vs. opamp dc gain of the first integrator.

TABLE I. COMPARSION OF DOUBLE-SAMPLING AND SINGLE-RATE MODULATORS

	OSR	f_{s1} (MHz)	GBW_1 (MHz)	GBW_2 (MHz)	A_1 (dB)	SNR (dB)
Double-Sampling	8	160	175	150	66	99.74
Single rate	12	240	320	175	60	100

but because of lower required GBW, the proposed double-sampling hybrid modulator consumes less power.

Like the conventional ΣΔ modulators, the finite opamp dc gain limits the accuracy of the proposed MDC-SD modulators. Figure 6 shows the simulated SNDR of the proposed double-sampling hybrid modulator with OSR_1 = 8, N = 1 and D = 2 and its single-rate equivalent with OSR = 12 versus different values of the first integrator dc gain. According to Fig. 6, the proposed modulator requires the first integrator with 66 dB dc gain and the conventional single-rate one needs about 60 dB dc gain.

Sensitivity to clock jitter is one of the main concerns in CT designs. The performance degradation due to the clock jitter in rectangular feedback DACs is proportional to clock jitter variance relative to the sampling time. Since in the MDC-SD structure, the sampling time in the first stage is extended, the relative clock jitter will be smaller as long as the absolute clock jitter is kept constant. Therefore the use of MDC-SD modulators is slightly advantageous with regard to the clock jitter. In Fig. 7 simulations are shown equivalently to single-rate (OSR=22) and MDC-SD (OSR_1=8, N=2) under clock jitter influence and the facts just stated can be seen.

Because of using double-sampling, simulation on the quantization noise folding due to the sampling paths mismatch must be performed. Fig. 8 shows the SNDR degradation vs. the mismatch of the sampling paths. It can be seen that the SNDR degradation of the proposed MDC-SD modulator is negligible even with a 0.3% mismatch between the sampling paths of the integrators. This is because the double-sampling technique is used in the second stage.

IV. CONCLUSION

A new class of hybrid ΣΔ modulators called Multirate Double-Sampling Cascaded hybrid modulator was introduced. It was found that despite of higher OSR in higher stages the lower OSR in the first stage will lead to decreased power consumption. This new architecture is also less sensitive to the clock jitter than the single-rate modulators and sampling paths mismatch has negligible effect on its performance.

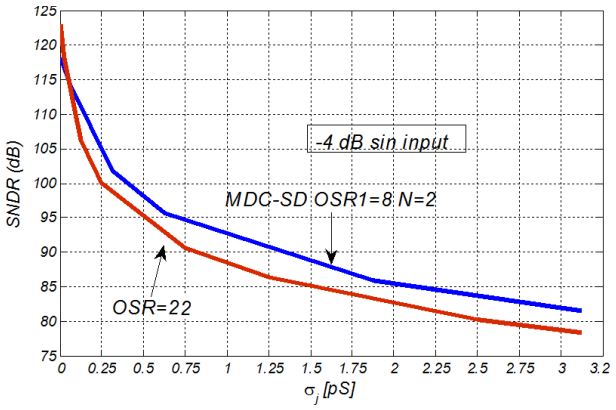

Figure 7. Performance degradation due to the clock jitter.

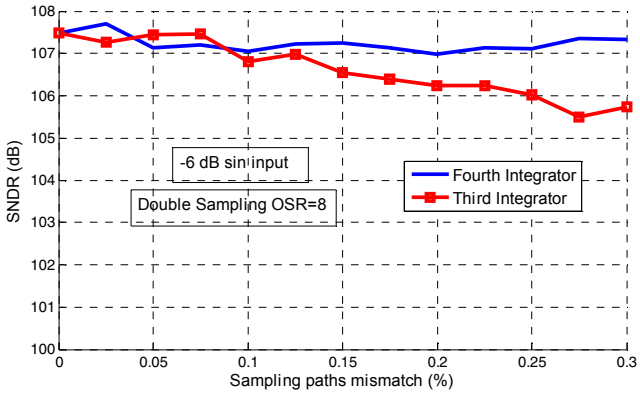

Figure 8. SNDR degradation versus the sampling paths mismatch.

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