

A Double-Sampled Hybrid CT/DT SMASH $\Sigma\Delta$ Modulator for Wideband Applications

Mohammad Hossein Maghami and Mohammad Yavari

Integrated Circuits Design Laboratory, Department of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran

E-mails: mhmaghami@ieee.org, myavari@aut.ac.ir

Abstract— This paper presents a novel hybrid continuous-time (CT) and discrete-time (DT) sturdy multi-stage noise shaping (SMASH) $\Sigma\Delta$ modulator architecture. The double-sampling technique is employed in the DT second stage modulator to reduce the power consumption of the overall modulator. A flat and unity STF's are used in the first and second stage modulators, respectively, to reduce the output swing of the analog building blocks without influencing the inherent anti-aliasing behavior of the first stage CT modulator. As a design example, the proposed SMASH 2-2 modulator is designed in a 90nm CMOS technology with 1V power supply. HSPICE simulation results show a signal-to-noise plus distortion ratio (SNDR) of 80.4dB in 12.5MHz bandwidth with 17mW power consumption while operating at 200MHz sampling frequency.

I. INTRODUCTION

Nowadays there is an increasing demand for both higher sampling rates and higher resolution while not expanding the power consumption too much. Therefore, CT modulators have received increasing attention over the last years due to their some meaningful advantages over DT implementations [1, 2]. Recent approaches have been drawn to the hybrid $\Sigma\Delta$ modulators featuring the integration of initial stage(s) as CT integrator(s) and subsequent DT integrators in the loop filter. These hybrid modulators are suitable for high speed applications. An example of this generation of modulators has been reported in [1].

A useful approach for handling DT modulators in wideband applications is to employ the double-sampling technique [3, 4]. In this method, since the integrator circuit operates during both phases of the clock, the effective sampling rate of the system is twice that of the clock frequency. This results in doubling the available time for settling of the integrators if the OSR and input signal bandwidth are fixed.

In CT $\Sigma\Delta$ architectures the analog coefficients are realized by some inaccurate RC time constants, with accuracy about $\pm 50\%$. By using an RC time constant tuning approach, the accuracy is improved to 1%–10% [5]. However, this is not enough for cascaded modulators. Therefore, the cascaded modulators are not a suitable candidate for CT $\Sigma\Delta$ modulators. An alternative $\Sigma\Delta$ architecture that reduces the sensitivity to noise leakages of traditional MASH structures has been recently presented for DT modulators and called sturdy MASH (SMASH) [6]. This topology replaces the error cancellation logic required in traditional MASH modulators by inherent analog filtering of the modulator stages. This is achieved by simply feeding back the second stage output to the most insensitive node of the first stage modulator which is the output of the first stage quantizer.

In this paper, a new hybrid CT/DT SMASH $\Sigma\Delta$ modulator is introduced for broadband applications. As an example, the proposed SMASH 2-2 modulator is designed in a 90nm CMOS process which achieves 80.4dB SNDR over 12.5MHz signal bandwidth. The proposed SMASH $\Sigma\Delta$ topology employs the double-sampling technique in the DT second stage modulator to reduce the power consumption.

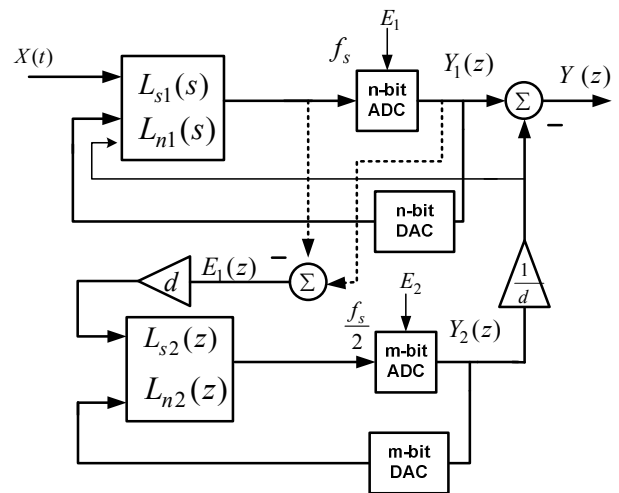


Figure 1. Proposed hybrid CT/DT SMASH modulator.

This paper is organized as follows. In Sect. II, the structure of the proposed modulator is briefly introduced. Section III gives details of the behavioral simulations. Circuit design and simulation results are presented in Sect. IV and the conclusions are given in Sect. V.

II. PROPOSED $\Sigma\Delta$ MODULATOR

Figure 1 shows the proposed double-sampling hybrid CT/DT SMASH $\Sigma\Delta$ modulator. The first stage is a CT modulator with an n -bit internal quantizer and the second stage is a DT one with an m -bit quantization. L_{si} , L_{ni} and E_i denote the signal loop filter, noise loop filter and quantization error of the i^{th} stage, respectively. In high-speed modulators, the opamps are operated near their maximum bandwidth, so the power consumption dramatically increases with the sampling frequency. To reduce the power consumption of the proposed $\Sigma\Delta$ modulator, the double-sampling technique is used in the second stage modulator. The operating frequency of the second stage is chosen half of the first stage modulator. So, the effective sampling rate of both stages is the same and since the operating frequency of the second stage is halved with respect to the overall modulator sampling rate, the power consumption of the second stage modulator is reduced.

For the CT integrators, a simple finite impulse response NTF is selected. The cascade of integrators feedforward (CIFF) architecture in the first stage is adopted, because it has the advantage of requiring only one multibit DAC, compared to the multiple feedback counterparts that need as many DACs as the modulator's order. As stated in [2], CT DACs are sensitive to the clock jitter, so by reducing the number of DACs, more insensitivity against clock jitter is achieved.

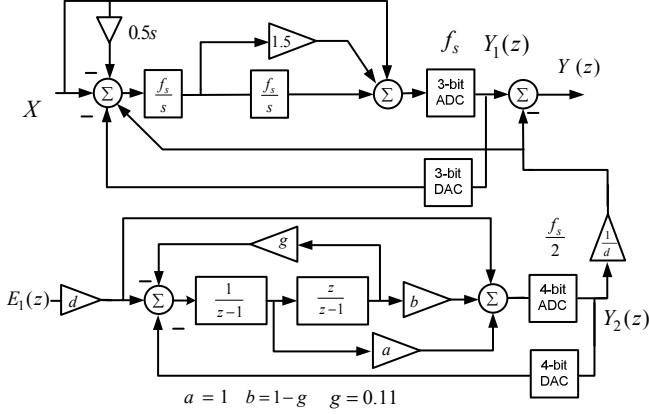


Figure 2. Proposed hybrid CT/DT SMASH 2-2 modulator.

A flat STF is used in the first stage CT modulator to reduce the effects of the analog circuits' imperfections such as the amplifier's nonlinear DC gain and limited output swing. Designing a flat STF in the first stage is followed by the methodology presented in [7] in order to not affect the inherent anti-aliasing behavior of first stage CT modulator. As most of the modulators presented in the literature show a peak in their STF, the out of band signals compromise the correct operation of the modulators [7]. In the simple DT unity STF, a direct path from the input of the modulator to the input of the quantizer leads to a STF which is identical to 1, but this is not true for CT modulators as analyzed in [7] and will be also shown later.

As a result of not processing the input signal by the second stage modulator, there is an option between choosing a unity STF and a flat one in the second stage modulator. But, since the second stage STF does not affect the anti-aliasing performance and the unity STF is a stricter condition than the flat STF, the unity STF is chosen in order to achieve low signal swing at the output of second stage integrators.

As a design example, the proposed SMASH 2-2 shown in Fig. 2 is considered. In this design the DT $NTF_1(z)$ is chosen as follows:

$$NTF_1(z) = (1 - z^{-1})^2 \quad (1)$$

The method of equivalent loop filters [2] has been applied to convert the DT NTF into its CT counterpart. The non-return-to-zero (NRZ) DAC shape is used in the proposed design for low power consideration and reasonable jitter tolerance. For further reduction of clock jitter sensitivity, a multibit internal quantizer is employed [2]. Considering the second stage of Fig. 2, $NTF_2(z)$ is given by:

$$NTF_2(z) = 1 - (2 - g)z^{-1} + z^{-2} \quad (2)$$

Using a linear model for the quantizers in Fig. 2, it can be shown that the z -domain transform of the modulator's output ideally is given by:

$$\begin{aligned} Y(z) &= X(z) - E_2(z) \left(\frac{NTF_2(z)NTF_1(z)}{d} \right) \\ &= X(z) - E_2(z) \frac{(1 - z^{-1})^2(1 - (2 - g)z^{-1} + z^{-2})}{d} \end{aligned} \quad (3)$$

where $X(z)$ stands for the input signal and $E_2(z)$ is the second stage quantization noise. The parameter d is chosen to be 4 in the presented work. The optimal value of parameter g which is a function of the oversampling ratio (OSR) is obtained by minimizing the second stage quantization noise in the overall modulator output and hence maximizing the SQNR. As is clear in Fig. 2, 3-bit and 4-bit quantizers are used in the first and second stages, respectively, in order to achieve more dynamic range and sufficient stability.

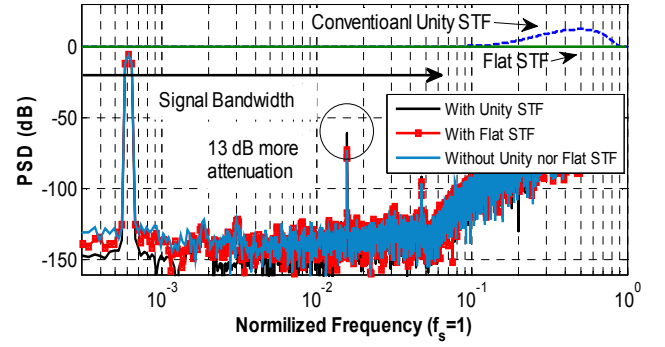


Figure 3. Anti-aliasing behavior of the proposed modulator.

III. SIMULATION RESULTS OF PROPOSED MODULATOR

In this section, time domain simulation results using MATLAB/Simulink are provided. The assumed OSR was 8. Using the opamp DC gain model proposed in [2], the presented SMASH structure requires 25dB DC gain for the first integrator whereas the equivalent MASH structure needs about 60dB DC gain. The behavioral simulations are performed to specify the required amplifier bandwidth (BW) in CT first stage. Using the model of [2] in system level simulations, the first and second opamps need a bandwidth higher than $2f_s$ and $1f_s$, respectively. It is worth mentioning that as stated in [2], CT MASH structures need more bandwidth than the above reported values even after the error compensation of this non-ideality.

The SNDR degradation of the proposed modulator is negligible (less than 1 dB) even with a 0.5% mismatch between the sampling paths of the second stage integrators since the effect of the sampling paths mismatch is attenuated by noise shaping property of the first stage modulator. Hence, the double sampling approach is efficiently employed in the proposed modulator without requiring any additional technique to alleviate the SNDR degradation due to the sampling paths mismatch. Figure 3 shows the anti-aliasing behavior of the proposed modulator. In these simulations, a -6dBFS input signal tone added with a -20dBFS noise tone at $f_s - (BW)/4$ were applied to the input of the modulator. As is clear, the proposed cascaded modulator which uses a flat STF in the first stage has the same anti-aliasing behavior where a flat STF is not employed. In other words, the anti-aliasing behavior of the first stage CT modulator is completely preserved while using a flat STF in the first stage. Note that, if a conventional unity STF is employed in the first stage, the anti-aliasing behavior of the modulator is degraded. As shown in Fig. 3, unlike the flat STF, the CT STF achieves an out-of-band peak when designing the DT STF as unity and then converting it to a CT one.

In order to minimize the excess loop delay (ELD) problem, one of the viable solutions is to reduce the delay of the loop comprising of the quantizer and the DAC. This is accomplished by using a high-speed comparator embedded in the quantizer in order to reduce the delay. Based on the behavioural simulations, with a delay of $0.3T_s$ which is 1.5ns in this design, the modulator doesn't show any degradation in its noise shaping property. Therefore, by using high-speed comparators, it is not necessary to compensate for ELD problem by available approaches.

IV. CIRCUIT DESIGN AND SIMULATION RESULTS

The modulator is designed in a 90nm CMOS technology. It operates at a clock frequency of 200MHz with a 1.0V supply voltage. The full scale differential input signal range is $0.8V_{pp}$.

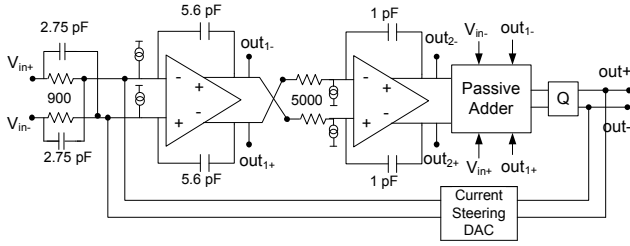


Figure 4. First stage circuit implementation.

Figure 4 shows the realization of the first stage CT modulator. The value of integrating resistors and full-scale current DAC is selected by considering their circuits' noise impact on the modulator's overall performance. All of the current source transistors are cascoded to increase their output impedance. To reduce the clock feedthrough and charge injection resulting from the switching transistors, high-crossing low-swing switch drivers are used to drive the current switches.

The linearity requirement of multibit current DACs is as high as the modulator's overall accuracy. Usually, two techniques are employed to enhance the linearity of multibit DACs: self-calibrated current-steering technique (SCCS) [8] and data weighted averaging (DWA) algorithm [9]. The DWA circuit increases the ELD in CT modulators. When the sampling rate is high, this phenomenon is very apparent. So, the SCCS technique is very suitable in low OSR wideband applications and used in this design.

A. Operational Amplifiers

Behavioral simulation results show that 25dB DC gain in amplifiers is sufficient to achieve 90dB SNDR. To consider a safety margin for process and temperature variations, the amplifiers with 35dB open loop DC gain are designed. Shown in Fig. 5 is a simple folded cascode amplifier which is used to realize the integrators. In conventional MASH structures high DC gain amplifiers are needed and hence two-stage or gain boosted topologies should be used resulting in more power dissipation compared to the proposed SMASH topology. A continuous-time common-mode feedback was used to define the output common mode voltage of the amplifiers.

B. Quantizers

In order to speed up the comparator circuit, a latch with two regenerative branches was used. Each comparator is composed of a regenerative latch, a preamplifier, and SR flip-flops. A switched-capacitor adder as shown in Fig. 6 is used in front of each preamplifier to add the input signal and output of CT integrators. It is critical to reset the comparator in order to minimize the memory effects [10]. To eliminate this effect, the preamplifiers and regenerative latches are reset in every clock period.

C. Second Stage Implementation

The realization of third and fourth integrators are shown in Figs. 7 and 8, respectively. The third integrator in Fig. 7 uses the double sampling technique. This discrete-time integrator works with a sampling frequency of 100MHz, but as the result of double sampling, the effect sampling rate is 200MHz. Since no active adder was used in front of the first stage quantizer, the error extraction is done at the input of the second loop using the output of the first stage quantizer, the input signal and the output of the first stage integrators. In Fig. 7 X+ is the indicator of signals that must be used for extraction of the first stage quantization error. The output signals of the third integrator are fed into the inputs of the fourth integrator. The fourth integrator also uses the double sampling technique with 100MHz sampling clocks.

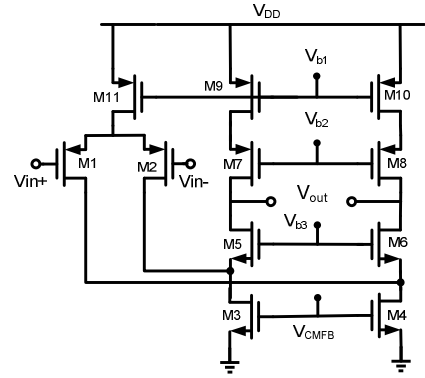


Figure 5. Amplifier used in the integrators.

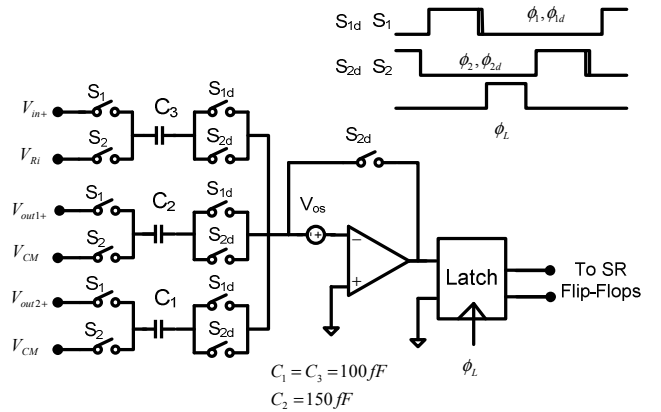


Figure 6. Passive adder used in the first stage modulator.

As the result of handling a unity STF in the second stage, an active adder is required in order to realize the adder of the second stage of Fig. 2. A simple implementation for this adder is adopted. The output of this adder is fed to the second stage quantizer. The same latches as the first stage modulator are used in the second stage.

A. HSPICE Simulation Results

In order to verify the validity of the proposed design, HSPICE simulations are performed. In order to take the FFT and calculate the SNDR, 32768-points FFT with a Hanning window is utilized. The simulated output spectrum for a -8dBFS 244kHz sinusoidal input signal is shown in Fig. 9. The overall performance of the modulator is summarized in Table I. It achieves 80.4dB SNDR over 12.5MHz signal bandwidth with an oversampling ratio of 8. It dissipates 17mW from a single 1V supply. To compare the performance of the simulated modulator with of some of state-of-the-art wideband (7.5MHz+) modulators, the following figure of merit (FOM) is employed:

$$FOM = \frac{Power}{2 \times BW \times 2^{ENOB}} \quad (4)$$

where BW and $ENOB$ are the modulator's input signal bandwidth and effective number of bits, respectively. A lower FOM indicates a higher performance. Table II lists the performance of some recently published wideband $\Sigma\Delta$ modulators. As is seen, this work is among the best published papers to date, but it should be noted that only the simulation results have been reported in this work.

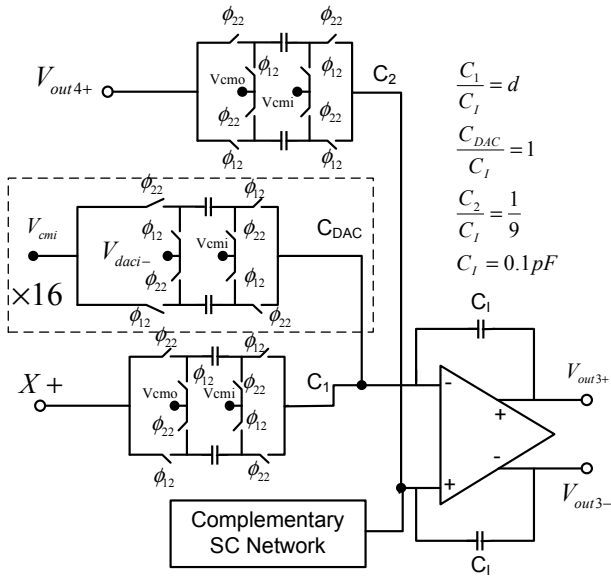


Figure 7. Third integrator.

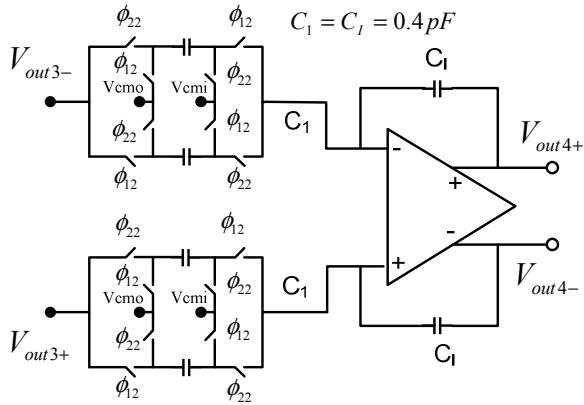


Figure 8. Fourth integrator.

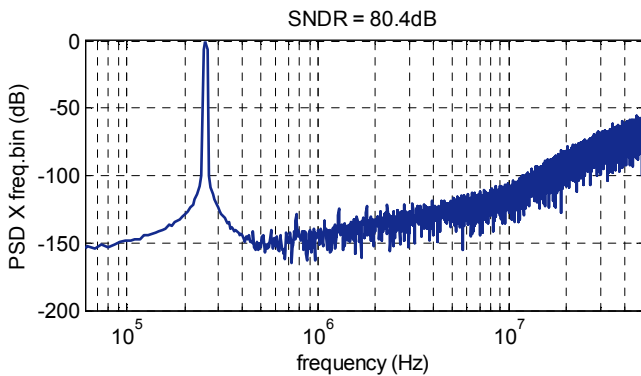


Figure 9. Simulated output spectrum.

TABLE I. SIMULATED PERFORMANCE SUMMARY.

Input Bandwidth (MHz)	OSR	Supply Voltage	Power Consumption (mW)	SNDR (dB)	Technology
12.5	8	1V	17	80.4	90 nm CMOS

TABLE II. COMPARISON WITH SOME REPUTED ADCs.

Reference	CMOS process/supply	Modulator Resolution (bit)	BW (MHz)	Power (mW)	FOM (pj/Conversion)
[1]	0.18μm/1.2V	11.5	7.5	63.6	1.46
[11]	0.18μm/1.8V	11.7	10	7.5	0.11
[12]	0.13μm/1.5V	10.8	15	70	1.31
[13]	0.13μm/1.2V	12	20	20	0.061
[14]	0.09μm/1V	12.2	25	16.4	0.069
This work	0.09μm/1V	12.5	12.5	17	0.12

V. CONCLUSIONS

A new hybrid CT/DT SMASH $\Sigma\Delta$ modulator was proposed. The double-sampling technique was employed in the second stage which is a discrete-time modulator. Since the double-sampling is utilized in the second stage, the proposed modulator has much less sensitivity to the sampling paths mismatch of double-sampled switched-capacitor circuits. The output swing requirement of the integrators was relaxed by employing a flat STF in the first stage and a unity STF in the second stage modulators without any sacrificing the inherent anti-aliasing behavior of the first stage CT modulator. As a design example, a wideband modulator was designed in a 90nm CMOS technology. It achieves 12.5bit resolution with a bandwidth of 12.5MHz while operating at 200MHz sampling rate with 17mW power consumption.

REFERENCES

- [1] S. D. Kulchychki et al., "A 77-dB dynamic range, 7.5-MHz hybrid continuous-time/discrete-time cascaded $\Sigma\Delta$ modulator," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 796-804, Apr. 2008.
- [2] M. Ortmanns and F. Gerfers, *Continuous-time sigma-delta A/D conversion*, Springer-Verlag, 2005.
- [3] P. J. Hurst and W. J. McIntyre, "Double-sampling in switched-capacitor delta-sigma A/D converters," *IEEE Int. Symp. on Circuits and Systems*, pp. 902-905, May 1990.
- [4] M. Yavari, O. Shoaie, and A. Rodriguez-Vazquez, "Double-sampling single-loop $\Sigma\Delta$ modulator topologies for broadband applications," *IEEE Trans. on Circuits and Syst., II*, vol. 53, no. 4, pp. 314-318, Apr. 2006.
- [5] B. Xia et al., "An RC time constant auto-tuning structure for high linearity continuous-time $\Sigma\Delta$ modulators and active filters," *Trans. on Circuits and Syst., I*, vol. 51, no. 11, pp. 2179-2188, Nov. 2004.
- [6] N. Maghari et al., "Sturdy MASH $\Sigma\Delta$ modulator," *Electronics Letters*, vol. 42, no. 22, Oct. 2006.
- [7] J. Maeyer et al., "Controlled behavior of STF in CT $\Sigma\Delta$ modulators," *Electronics Letters*, vol. 41, no. 16, Aug. 2005.
- [8] D. W. J. Groeneveld et al., "A self-calibration technique for monolithic high resolution D/A converters," *IEEE J. Solid-State Circuits*, vol. 24, no. 12, pp. 1517-1522, Dec. 1989.
- [9] R. Baird, and T. Fiez, "Linearity enhancement of multibit $\Sigma\Delta$ A/D and D/A converters using data weighted averaging," *IEEE Transactions on Circuits and Systems-II*, vol.42, no.12, pp. 735-763, Dec. 1995.
- [10] C. Sandner, M. Clara, A. Santner, T. Hartig, and F. Kuttner, "A 6-bit 1.2-GS/s low-power flash ADC in 0.13-μm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1499-1505, Jul. 2005.
- [11] R. Schoofs et al., "A design-optimized continuous-time delta-sigma ADC for WLAN applications," *IEEE Transactions on Circuits and Systems-I*, Vol. 54, No. 1, pp. 209-217, Jan. 2007.
- [12] S. Paton et al., "A 70-mW 300-MHz CMOS continuous-time $\Sigma\Delta$ ADC with 15-MHz bandwidth and 11bits of resolution," *IEEE J. Solid-State Circuits*, vol.39, no. 7, pp. 1056-1063, Jul. 2004.
- [13] G. Mitteregger et al., "A 20-mW 640-MHz CMOS continuous-time $\Sigma\Delta$ ADC with 20-MHz signal bandwidth, 80dB CMOS dynamic range and 12-bit ENOB," *IEEE J. Solid-state Circuits*, vol. 41, no. 12, pp. 2641-2649, Dec. 2006.
- [14] F. Chen et al., "Design of wideband low-power continuous-time $\Sigma\Delta$ modulator in 90nm CMOS technology," *Analog Integrated Circuits and signal Processing*, vol. 54, No. 3, pp. 187-199, Mar. 2008.