

# Hybrid CT/DT Resonance-Based Cascade $\Sigma\Delta$ Modulators for Broadband Low-voltage Applications

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**Abstract**—In this paper, two new hybrid CT/DT cascade  $\Sigma\Delta$  modulators are proposed for use in low-voltage broadband applications. Unlike the MASH architecture, these modulators are less sensitive to amplifier DC gain of continuous-time (CT) stage and avoid the need of compensation for finite gain-bandwidth induced error in CT loop filter. The modulators also feature global resonance scheme, noise transfer function enhancement, double-sampling technique and flat and unity STF. These techniques are combined together in novel topologies that allow increasing the resolution in nanometer CMOS high-speed applications. Behavioral simulations confirm the effectiveness of the proposed schemes.

**Index Terms**—Analog-to-digital converter,  $\Sigma\Delta$  modulation, Continuous-time circuits, Switched-capacitor circuits.

## I. INTRODUCTION

Many digital communication systems demand analog-to-digital converters with megahertz signal bandwidth and high-resolution in next generation nanometer CMOS technologies at low power consumption. Most of the earlier  $\Sigma\Delta$  modulators are based on switched-capacitor (SC) circuits, whereas  $\Sigma\Delta$  modulators with CT loop filters can potentially achieve higher clock frequency with lower power consumptions with the advantage of inherent anti-alias filtering [1]. Therefore they have received increasing attention over DT implementations. Recent approaches like the modulator presented in [2] have been moved toward handling hybrid  $\Sigma\Delta$  modulators in which the front-end SC circuits are replaced with CT circuits, providing faster operation and embedded anti-aliasing behaviour. These hybrid modulators are suitable for high-speed applications.

Employing  $\Sigma\Delta$  modulators in wideband applications demands using low oversampling ratios (OSRs). This will result in reduction of modulator accuracy. MASH topologies with multi-bit quantization are often used to achieve the required dynamic range. But they are sensitive to the quantization noise leakage caused by mismatches between the analog and digital signal processing parts. Moreover, CT MASH structures need for compensation for finite gain-bandwidth induced error in CT loop filter [3]. Therefore cascade architectures are not suitable for CT  $\Sigma\Delta$  modulators. An alternative  $\Sigma\Delta$  architecture that reduces the sensitivity to noise leakages of traditional MASH structure has been presented for DT modulators called Sturdy MASH (SMASH) modulator by omitting the digital filters [4]. This topology replaces the error cancellation logic required in traditional MASH modulators by inherent analog filtering of the modulator stages. This is achieved by simply feeding back the second stage output to the most insensitive node of the first stage which is the output of the first stage quantizer.

In the presented work, using the feature of SMASH structure in a case of CT integrators, two modulators are proposed based on four strategies. First, the global resonance is used to optimally distribute the zeroes of the noise transfer function (NTF) within the required signal bandwidth. Second, the NTF enhancement technique [5] is applied to shape-out the second stage quantization noise further without considerable degradation the stability of it. Third, flat [6] and unity signal transfer functions (STF) [7] are employed in integrators of modulator to reduce the amplifier output signal swings. Fourth, the

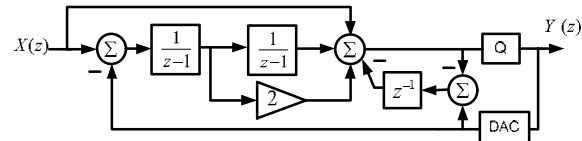


Figure 1. A DT  $\Sigma\Delta$  modulator with NTF enhancement.

double-sampling technique [8] is effectively applied to the second stage of modulators to reduce the overall power consumption.

The paper is organized as follows. In section II the derivations of the proposed modulator structures are described. Section III provides the system level simulation results by considering the circuit non-idealities. The conclusions are given in Section IV.

## II. PROPOSED $\Sigma\Delta$ MODULATORS

The SMASH structure obviates the matching requirement between analog and digital parts of traditional cascaded modulators, which allows using low-gain amplifiers with no significant degradation of the modulator performance. To further enhance the noise shaping property of SMASH structures, resonance inside the modulator loop filter can be applied to it. This is an efficient way to increase the resolution without penalizing the number of integrators. Local resonance technique has been used in  $\Sigma\Delta$  modulators, allows shifting the zeroes of the NTF from DC and distributing them in an optimum way to maximize the SNDR. Recently, a new kind of resonance strategy, named global resonance, has been applied to cascade  $\Sigma\Delta$  modulators [9] and modified in some cases by [10]. This new approach is obtained by feeding back the quantization error from the last stage to the previous one.

NTF enhancement is another technique for increasing the noise shaping performance of a  $\Sigma\Delta$  modulator, without affecting its STF and adding integrators to its loop filter. This technique raises the effective order of the modulator by one or more, depending on the applied coupling filter, without aggravating the original stability (before NTF enhancement). Shown in Fig. 1, a delayed replica of the quantization error is fed back into the modulator to be shaped by the NTF. Since this increments the NTF by an extra  $(1-z^{-1})$  factor, the order of the modulator is increased by one [5].

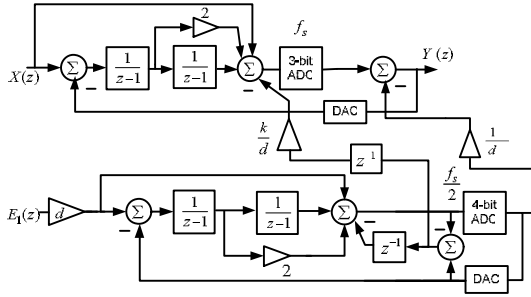
### A. First Proposed $\Sigma\Delta$ Modulator

The first proposed modulator is depicted in Fig. 2. Both stages are DT and as will shown later, the first stage will convert to CT modulator. Finding stable NTFs is the first step in the design procedure. For both stages simple FIR NTF are chosen as follow:

$$NTF = (1 - z^{-1})^2 \quad (1)$$

Unity STF is adopted for both stages to reduce the integrator output swings and mitigate the effects of circuit imperfections such as the

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 Figure 2. First proposed SMASH  $\Sigma\Delta$  modulator.

amplifier's nonlinear DC gain. NTF enhancement with global resonance is applied to the second stage modulator.

In high-speed modulators, opamps are operated near their maximum bandwidth, so power consumption dramatically increases with sampling rate. A useful approach for handling DT modulators in wideband applications with lower power consumption is to employ the double-sampling technique. In this way, the integrators operate during both phases of the clock by two distinct sampling capacitors, resulting in doubling the available time for settling of the integrators if the OSR and input signal bandwidth are fixed. In this work, the effective sampling rate of both stages are the same and since the operating frequency of the second stage is halved with respect to the first stage sampling rate, the power consumption of the second stage modulator is expected to be reduced. As a result of using only forward Euler (FE) integrators for realizing the chosen NTF, because of simpler implementation, an addition of the analog delayed last stage quantization error is required at the input of the first stage quantizer, demanding an additional inter-stage DAC [10].

Considering linear model for internal quantizers of modulator in Fig. 2 analysis gives rise to:

$$Y = X - E_2 \left( \frac{NTF_2 NTF_1 - z^{-1} NTF_2 NTF_1 + z^{-1} NTF_1 k}{d} \right) \quad (2)$$

Regards to selected NTFs, the contribution of the second quantization error to the overall output of SMASH is then:

$$Y|_{e_2} = - \frac{(1-z^{-1})^5 + (1-z^{-1})^2 k z^{-1}}{d} = - \frac{(1-z^{-1})^2 (1-(3-k)z^{-1} + 3z^{-2} - z^{-3})}{d} \quad (3)$$

Now a pair of complex conjugate zeros is introduced in the overall NTF whose location depends on coefficient  $k$ . Optimal value of  $k$  for maximising the SNDR is obtained as follows:

$$k_{opt} = \arg \min_k \int_0^{fs/(2OSR)} \left| (1-z^{-1})^2 (1-(3-k)z^{-1} + 3z^{-2} - z^{-3}) \right|^2 df \quad (4)$$

Assuming  $z = e^{j\theta}$  and  $\theta = 2\pi f / f_s$ , the optimal value can be found by nulling the first derivative, which gives rise to (5).

$$k_{opt} = \frac{0.5 \sin \frac{4\pi}{OSR} + 28 \sin \frac{2\pi}{OSR} - \frac{16}{3} \sin \frac{3\pi}{OSR} - 112 \sin \frac{\pi}{OSR} + \frac{70\pi}{OSR}}{-16 \sin \frac{\pi}{OSR} + 2 \sin \frac{2\pi}{OSR} + \frac{12\pi}{OSR}} \quad (5)$$

Table I shows the SNDR for different OSRs when the global resonance and NTF enhancement techniques are applied to the SMASH structure. Interstage gain of 4 ( $d = 4$ ) is used in all the simulations to utilize the full dynamic range of the last loop. As is clear, in most of the cases the SNDR improvement is in the order of 10dB. The input signal level is -4dBFS.

### B. Second Proposed $\Sigma\Delta$ Modulator

Recently, another kind of global resonance strategy has been app-

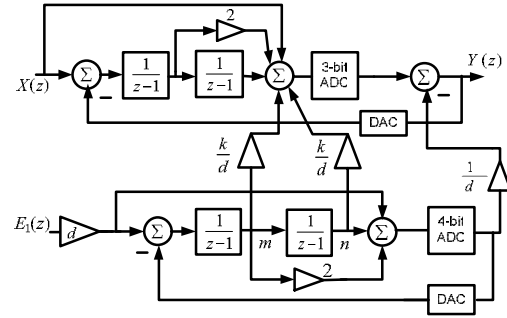

 Figure 3. SMASH  $\Sigma\Delta$  modulator with modified global resonance.

TABLE I. SNDR FOR DIFFERENT OSRS (FIRST PROPOSED MODULATOR).

OSR	$K_{opt}$	SNDR ( $k = 0$ ) without NTF Enhancement	SNDR ( $k = k_{opt}$ ) with NTF Enhancement
16	0.0004	112.2 dB	125.4 dB
12	0.0013	99.7 dB	112 dB
8	0.0065	82.5 dB	91.7 dB
4	0.0961	57.3 dB	59.4 dB

lied to cascade  $\Sigma\Delta$  modulators [10]. This new approach is a modified version of previous global resonance technique. In this method resonance is achieved through the inter-stage paths that feed back a scaled version of the last stage integrator outputs at the input of the first stage quantizer. This technique is employed in a case of SMASH structure as shown in Fig. 3. The implementation of global resonance in this modulator also uses only FE integrators, thus simplifying the circuit level implementation. Considering the second stage of Fig. 3, it can be shown that the input,  $m$ , and the output,  $n$ , of the second integrator are given by:

$$m(z) = -z^{-1}(1-z^{-1})E_2(z), n(z) = -z^{-2}E_2(z) \quad (6)$$

Thus:

$$m(z) + n(z) = -z^{-1}E_2(z) \quad (7)$$

Now, a delayed version of second stage quantization noise is obtained directly by adding the  $m$  and  $n$  signals.

Combining this global resonance with NTF enhancement and double-sampling techniques, modulator depicted in Fig. 4 is obtained. Since in double-sampling, output of integrators are valid during both phases, inter-stage gains can be directly fed back to the first stage. It can be shown that the  $m$  and  $n$  signals in Fig. 4 are given by:

$$m(z) = -z^{-1}(1-z^{-1})^2 E_2(z), n(z) = -z^{-2}(1-z^{-1})E_2(z) \quad (8)$$

In this case, the addition of  $m$  and  $n$  in the second stage results in:

$$m(z) + n(z) = -z^{-1}(1-z^{-1})E_2(z) \quad (9)$$

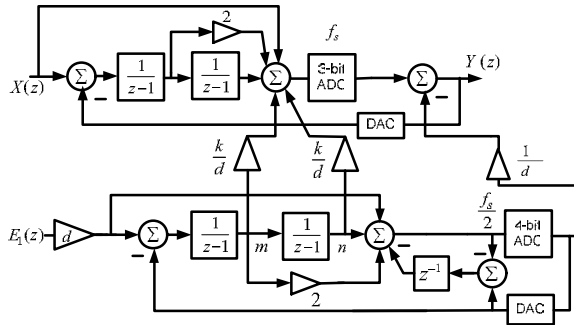
Considering the above relation and linear model for internal quantizers of modulator in Fig. 4 analysis gives rise to:

$$Y = X - E_2 \left( \frac{NTF_2 NTF_1 - z^{-1} NTF_2 NTF_1 + z^{-1} (1-z^{-1}) NTF_1 k}{d} \right) \quad (10)$$

Regards to selected simple FIR NTFs, the contribution of the second quantization error to the overall output of SMASH is then:

$$Y|_{e_2} = - \frac{(1-z^{-1})^5 + (1-z^{-1})^3 k z^{-1}}{d} = - \frac{(1-z^{-1})^3 (1-(2-k)z^{-1} + z^{-2})}{d} \quad (11)$$

Similar to previous sub-section, a pair of complex conjugate zeros is introduced in the overall NTF. The optimal values of in-band zeros are depend on  $k$ , where its value is obtained like the first proposed modulator and is:


 Figure 4. Second proposed SMASH  $\Sigma\Delta$  modulator.

$$k_{opt} = \frac{-3 \sin \frac{4\pi}{OSR} - 168 \sin \frac{2\pi}{OSR} + 32 \sin \frac{3\pi}{OSR} + 672 \sin \frac{\pi}{OSR} - 420\pi}{4 \sin \frac{3\pi}{OSR} + 180 \sin \frac{\pi}{OSR} - 36 \sin \frac{2\pi}{OSR} - \frac{120\pi}{OSR}} \quad (12)$$

Table II shows the SNDR of the proposed modulator for different OSRs when the input signal level is  $-4\text{dBFS}$ . In most of the cases the improvement is in the order of 20 dB. As is clear, when  $OSR = 4$  SNDR of 73.1dB (11.85 bits) is achieved which is very remarkable in high-speed applications.

### C. DT-to-CT Conversion of First Stage

Now, first stage of the proposed modulators is converted to CT integrators in order to benefit the features of CT design. The method of equivalent loop filters [1] has been applied to convert DT modulators into their CT counterparts. The main idea is to convert every existing loop filter from the DT to the CT domain. Therefore, exactly the same modulator output spectrum could be obtained.

CT  $\Sigma\Delta$  modulators are considered to be very interesting because of their implicit anti-aliasing filter. However, while an anti-aliasing filter is not necessary in front of the modulator, still a 'no-overload' filter should precede the modulator to prevent instability. This filter is required as in the CT  $\Sigma\Delta$  modulator, the STF peaks. This causes out-of-band signals to be amplified, which can corrupt the correct operation of the modulator and cause instability. As analyzed in [6] if a DT modulator is designed with a unity STF and then converted to a CT one, the resulting STF would see a peak in out-of-band frequencies where the out-of-band input signals to the modulator are highly amplified rather than attenuated resulting in degraded anti-aliasing behavior. The STF of the first stage modulator is designed based on the technique proposed in [6] in order to achieve a flat STF. Also by employing this technique, the output swing of the integrators is reduced. Proposed hybrid  $\Sigma\Delta$  modulators are shown in Fig. 5.

In the proposed designs, the DAC feedback pulse shape is chosen considering clock jitter sensitivity, required gain-bandwidth and slew rate of the opamps. Therefore, the non-return-to-zero DAC shape is used for low power consideration and reasonable jitter tolerance [1]. For further reduction of clock jitter sensitivity, a multi-bit internal quantizer is used. CT  $\Sigma\Delta$  modulators suffer from a problem not seen in DT designs, that is nonzero delay between the quantizer clock edge and the time when a change in output bit is seen at the feedback point in the modulator known as excess loop delay (ELD). ELD may cause the modulator to be unstable. In order to minimize the ELD problem, one of the viable solutions is to reduce the delay of the loop comprising of the quantizer and the DAC. This is accomplished with the help of high-speed comparators in order to reduce the quantizer delay. The ELD problem is analyzed using behavioral simulations. With the delay of  $0.3T_s$  in these designs, the modulators don't show any degradation in their noise shaping property. Consequently by using high speed comparators, it is not necessary to compensate this

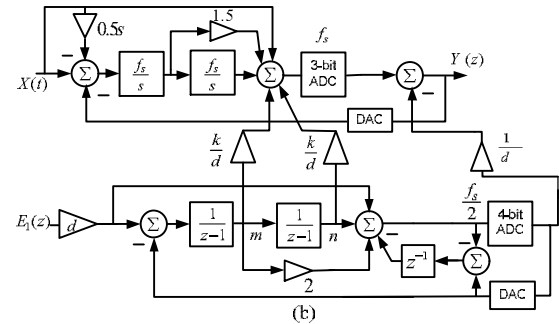
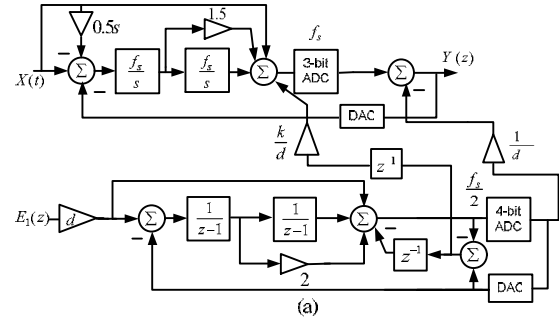

 Figure 5. Proposed hybrid CT/DT SMASH  $\Sigma\Delta$  modulators.

TABLE II. SNDR FOR DIFFERENT OSRS (SECOND PROPOSED MODULATOR).

OSR	$K_{opt}$	SNDR ( $k = 0$ ) without NTF Enhancement	SNDR ( $k = k_{opt}$ ) with NTF Enhancement
16	0.03	112.2 dB	138.5 dB
12	0.053	99.7 dB	125 dB
8	0.1185	82.5 dB	105.9 dB
4	0.4571	57.3 dB	73.1 dB

problem. Note that as the linearity of first stage DAC must exceed the whole modulator resolution, self-calibrated current-steering technique [11] can be applied to it without increasing the ELD in CT modulator with easy circuit implementation.

### III. SIMULATION RESULTS

In order to show the effectiveness of the proposed modulators, some behavioral simulations using MATLAB-Simulink are performed. In this section only the second proposed modulator is considered for saving space. In Fig. 6 SNDR is shown versus the input signal amplitude. The peak SNDR is obtained at  $-4\text{dBFS}$  input for  $OSR = 16$ , at  $-3.5\text{dBFS}$  input for  $OSR = 12$  and  $OSR = 8$ , and at  $-2.5\text{dBFS}$  input for  $OSR = 4$ . The integrators used in these simulations were assumed to be ideal. Note that the combined usage of flat and unity STF with multi-bit quantization leads to these low overload factors.

The proposed SMASH shown in Fig. 5 (b) was simulated and compared with equivalent MASH structure. For this simulation,  $OSR$  of 8 was used and input signal level is  $-6\text{dBFS}$ . One of the most important concerns in MASH modulators is the noise leakage due to opamp non-idealities of integrators. Figure 7 plots the SNDR versus first integrator DC gain of SMASH and equivalent MASH structure while all the other integrators are ideal. As is clear, the proposed structure is less sensitive to opamp gain. A low DC gain requirement allows using simple one-stage opamps rather than two-stage ones, leading to power savings. Behavioral simulations also reveal that, the

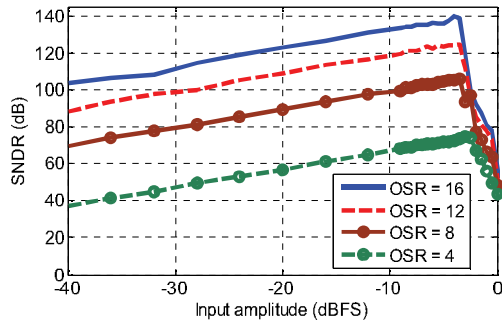


Figure 6. SNDR versus input signal of proposed (II)  $\Sigma\Delta$  modulator.

first and second opamps that are more important than the second stage opamps need a gain-bandwidth higher than  $1.3f_c$  and  $1f_c$  respectively. Note that as mentioned in [3], CT MASH structures need more gain-bandwidth than above reported values even after error compensation of this non-ideality. So the use of SMASH structure results in both reduced gain-bandwidth requirements and omitting the need for compensation for finite gain-bandwidth induced error in CT loop filter.

It is worth mentioning that any mismatch between the sampling capacitors in double-sampling technique produces unwanted out-of-band noise folding to the inband frequencies. Therefore, the SNDR is degraded. Since the effect of the sampling paths mismatch in the proposed modulators is attenuated by noise shaping property of the first stage modulator, this technique is efficiently employed without requiring any additional technique to alleviate the mismatch problem. Behavioral simulations show that the SNDR degradation of the proposed modulators is negligible even with a 0.7% mismatch between the sampling paths of the second stage integrators (Fig. 8).

Another advantage of the proposed architectures comes from the use of flat and unity STF, yielding to the reduction of the amplifiers' output swing. As illustrated in Fig. 9, the integrators output swings in the second proposed modulator are much less than the reference voltage level. This is translated into a better linearity of the proposed architectures and makes them more feasible in low-voltage nanometer CMOS technologies. Moreover, by employing flat STF in first stage of proposed modulators, anti-aliasing behavior of them is not affected. Simulations show that in this design if a DT modulator with unity STF is converted to CT one, the resulting STF would see a 12dB peak in out-of-band frequencies where this will result in degraded anti-aliasing behavior.

#### IV. CONCLUSIONS

Two novel hybrid CT/DT SMASH  $\Sigma\Delta$  modulators were proposed. They combine global resonance and NTF enhancement techniques with flat and unity STF to achieve reduced output swings. Because of featuring SMASH structure, the proposed modulators are very robust with respect to non-linearities as compared to traditional MASH modulators. The double-sampling technique is employed in the second stage of modulators in order to reduce the overall power consumption of them. Since the double-sampling is utilized in the second stage, the proposed modulators have much less sensitivity to the sampling paths mismatch of double-sampled switched-capacitor circuits. These characteristics make the proposed modulators very appropriate for low-voltage wideband nanometer CMOS A/D conversion.

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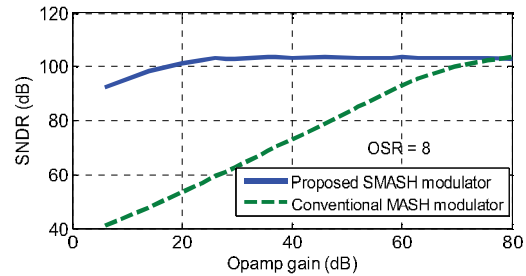


Figure 7. SNDR versus amplifier DC gain of first integrator.

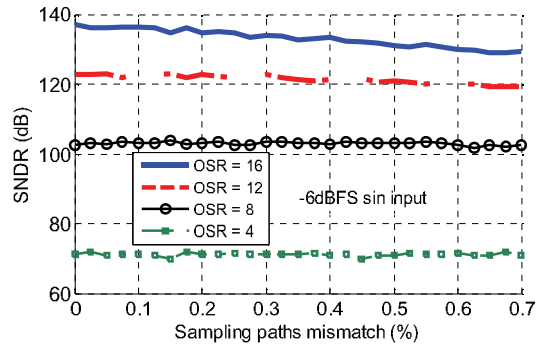


Figure 8. SNDR versus sampling paths mismatch.

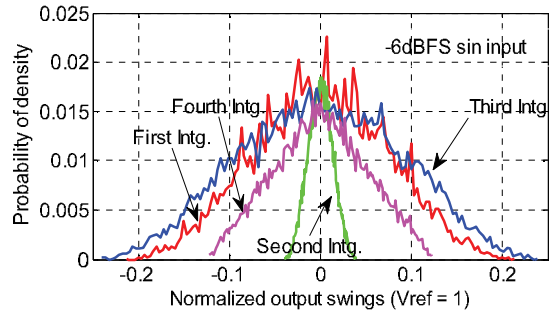


Figure 9. Integrator output swings.

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