Low Voltage Low Power Techniques in Design of Zero IF CMOS Receivers

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Abstract- **In this paper a new technique is proposed for designing the front-end of the narrow band CMOS receivers. The signal current of the input transconductance directly drives the low flicker noise PMOS switches of the mixer. Two inductors connected to VDD provide the DC current path for the input transconductance and the switches. The inductors absorb the parasitic capacitances of the switches at the operating frequency reducing the noise, and nonlinearity components at the output. Due to fewer transistors in stack the approach provides large signal swing at the output which makes it desirable for low voltage and low power applications. A low voltage technique is used for designing the CMFB circuit for stabilizing the common mode of the output. The output of the downconverter is a second order low pass passive filter comprising of series filtering and the usual parallel filtering. The series filtering not only relaxes the linearity of other subsequent stages but also; provides lead-lag compensation making the CMFB loop more stable. The techniques have been applied to a front-end of a prototype UMTS receiver in 0.18µm CMOS technology using 1.2V supply voltage. The simulation results show 26.5 dB voltage conversion gain, -5.5dBm IIP3, 51.5dBm IIP2, -20.5dBm 1dB-CP, 3.1dB double side band thermal noise figure, and 6 kHz flicker noise corner frequency. The circuit only draws 4.5mA current from the 1.2V supply voltage.**

Index Terms— **Downconverter, Flicker noise, Front-end, LNA, Mixer, Second order intermodulation, Zero IF.**

I. INTRODUCTION

Demand for using zero IF CMOS receivers in commercial telecommunication standards is undoubtedly increasing due to its higher capability of integration and lower cost [1], [2]. But there are some obstacles in the path mainly related to the down conversion part: DC offset, second order nonlinearity, and the flicker noise. The first two problems are due to zero IF property while the last is due to employing CMOS technology in active mixers. Active mixers are attractive due to their conversion gain and reduction of the effects of the succeeding blocks on the total NF of the receiver. Therefore more attentions have been paid to modeling of the noise behavior of the mixer as well as its second order nonlinearity behavior. In [3] the noise in active mixers has been completely analyzed. The amount of the flicker noise at the output is proportional to the DC current passing through the switches. In [4] current reuse technique has been used in the input transconductance for flicker noise reduction. Another technique has been used for decreasing the current of the switches at the transition instants, to reduce the flicker noise at the output [5].

Second order nonlinearity analysis in active mixers has been done in [6],[7], and some techniques have been proposed for improving the IIP2 of the active mixers.

In [8] a technique has been used for improving both the flicker noise and second order nonlinearity behavior of the active mixers. The technique is developed and optimized for low voltage and low power receivers and has been applied on the front-end of the prototype UMTS receiver.

The organization of the paper is as follows: the structures for the RF front-end and circuit implementation are mentioned in the next section. Section III is allocated for the simulation results and conclusions are summarized in IV.

II. CMOS RF FRONT-END AND CIRCUIT IMPLEMENTATION

Two main structures that have been commonly used for the LNA in the most recent CMOS receivers are inductively source degenerated (ISD) and common gate (CG) structures. At the same power consumption ISD presents lower NF, and higher equivalent input transconductance compared to CG.

Output current of the input devices could be converted to voltage at the load of the LNA using tank circuit for deriving the input transconductance devices of the mixer. This approach reduces the contribution of the mixer in NF but imposes high linearity requirement to the mixer which demands higher power consumption. Therefore in some recent receivers the merged LNA and mixer has been used for wideband applications [2]. So proper designing of the downconversion is more important because it significantly affects the linearity and low frequency specifications of the receiver.

Based on the above short discussion for presenting low NF at lower power consumption a merged LNA and mixer with the ISD technique for the input matching is used in this design.

Figure 1 illustrates the core schematic of the front-end designed in a 0.18µm CMOS technology using 1.2V supply voltage for a prototype UMTS receiver. The input trasconductance is based on ISD differential LNA due to its low NF and high equivalent transconductance at the low power consumption. The $M_{1\text{-}2}$ are input devices and are selected large (450/0.18µm) to make the required capacitance for the input matching. The $L_{s1\text{-}2}$ are 0.85nH and are used for 50Ω impedance matching, and the $L_{g1\text{-}2}$ are 6.5nH which could be realized as a combination of on-chip spiral inductor (4nH), and bond-wire/pin parasitic inductors (2.5nH). Input devices, $M_{1\text{-}2}$ draw 2.8mA and are biased through constant g_m biasing circuit to have less sensitivity to the corner cases and process variations. $M_{3\text{-}4}$, Cascode devices, have the same size as $M_{1\text{-}2}$ and used for more isolation between the input and other ports of the receiver.

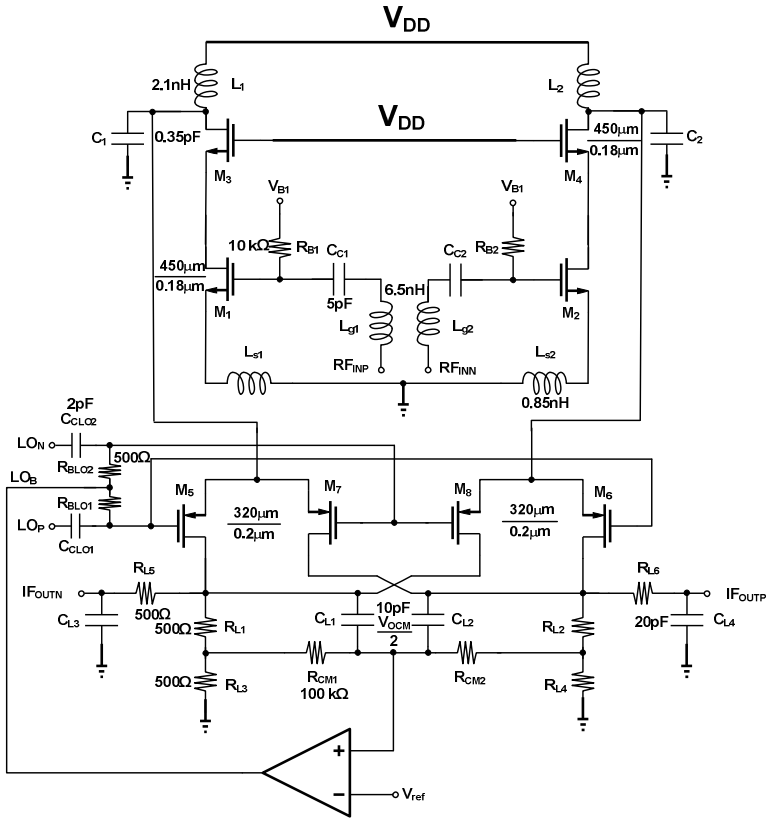


Figure 1. The core schematic of the RF front-end.

The inductors $L_{1\text{-}2}$ are tied to VDD to provide DC current path for the input devices and the switches. Moreover they absorb undesired parasitic capacitances at the source of the switches providing a clean path for the signal current to be directed to the output. In addition, they limit the parasitic effects due to switches on noise figure and nonlinearity [8]. The inductors are 2.1nH resonating with the parasitic capacitances and 0.35pF MIM capacitors in the 2.14GHz. In this design they are considered to be implemented through bond-wire/pin parasitic inductances.

The PMOS switches, $M_{5\text{-}8}$, are selected large (320/0.2μm) to have less flicker noise and sensitivity to the process variations and the mismatch. The gate of the switches is biased through the CMFB circuit. In this design the part of the load resistors which carry the DC current are 1kΩ and the common mode output voltage is 0.6V which forces each switch to draw 0.3mA DC current.

The load of the downconverter is a second order passive filter instead of typical first order filter. The first stage is a parallel one just like the filter used in the conventional mixers. The second stage is a series one which provides more blocker and unwanted signal rejection, and improves the phase margin of the CMFB loop. The series branch relaxes the linearity, amount of rejection, and power consumption constraints of the subsequent stages. For controlling the noise of the series resistor of the second stage of the filter, lower resistor should be chosen. In this design 1kΩ (two 500Ω resistors) and 10pF are used for the first stage (parallel filtering) and 500Ω and 20pF are chosen for the second stage of the filter (series filtering).

In the CMFB loop of the circuit the output voltage is set at 0.6V for the maximum swing. This makes the design of the error amplifier difficult to work properly with the wide range of input common mode variation. Therefore the parallel 1kΩ resistors are split into two equal series resistors ($R_{L1\text{-}4}$) so that the output common mode is sensed at a lower voltage level of 0.3V. The reduced loop gain is compensated using the gain of a simple one-stage PMOS input OTA.

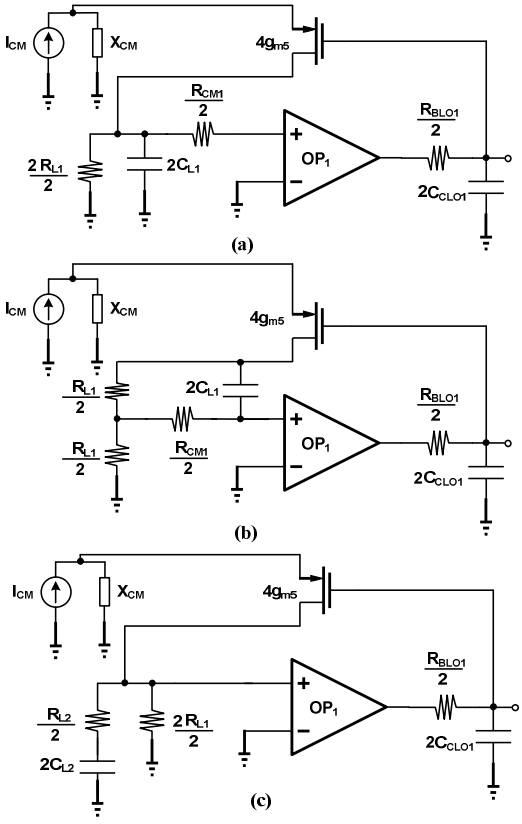


Figure 2. The simplified equivalent circuit of the CMFB loop in case of, (a) no modification is done on the circuit (typical), (b) connecting the capacitors of the parallel filtering to the output common mode node, (c) adding the series filtering branch to the circuit.

Figure 2(a) illustrates the simplified equivalent circuit for the CMFB loop in the typical mixer (C_{L1} and $2R_{L1}$ are used as the parallel load of the mixer, C_{L1} is connected to ground, and no resistor splitting and series filtering are used). R_{CM1} is a large resistor for sensing the common mode signal, OP_1 is the error amplifier, R_{BLO1} and C_{CLO1} are the LO biasing resistor and coupling capacitor. Moreover, $4g_{m5}$ represents the transconductance of the LO switches in the transition instants of the LO signal when all the switches are conducting (g_m of the switches changes due the large LO signal on their gates). I_{CM} and X_{CM} model the common mode signal current and impedance at the source of the switches. X_{CM} is near to zero at the very low and high frequency and reaches to its maximum at the operating frequency. The loop should be stable at its higher loop gain which is at the low frequency. As it is seen in Figure 2(a), the simplified loop gain at low frequency is:

$$A_{CL1} = \frac{-4g_{m5}R_{L1}}{1+2R_{L1}C_{L1}s} \times \frac{g_{mOP}R_{LOP}}{1+2(R_{LOP}+R_{BLO}/2)C_{CLO}s} \quad (1)$$

Where g_{mOP} is the input transconductance of the OP_1, and R_{LOP} is the output impedance of the OP_1 determining the DC gain of the OPAMP. In this analysis, the parasitic capacitances of the OP1 are neglected. The A_{CL1} has two poles that are close to each other. In case of DC loop gain more than 40dB, the phase margin of the loop is not positive and the loop will oscillate.

For solving the problem, as it is shown in Figure 2(b) the parallel load capacitors are connected to common mode output node instead of ground node. The loop gain in this case is:

$$A_{CLnew1} = -4g_{m5}\frac{R_{L1}}{2}\frac{1+(R_{L1}+2R_{CM1})C_{L1}s}{1+(R_{L1}+R_{CM1})C_{L1}s} \times \frac{g_{mOP}R_{LOP}}{1+2(R_{LOP}+R_{BLO}/2)C_{CLO}s} \quad (2)$$

The second fraction of the A_{CLnew1} is the same as in (1) while; the DC gain of the first fraction is half of its counterpart in (1) and it has a low frequency zero and a pole that is nearly twice of the zero (R_{L1} is negligible respect to R_{CM1}). This however removes the pole of the first fraction and replaces a low frequency zero and pole (of twice the zero) instead; it will raise the loop gain by 6dB at high frequencies causes the unity gain bandwidth of the loop to be twice, consequently raising the effect of parasitics on the stability of the loop.

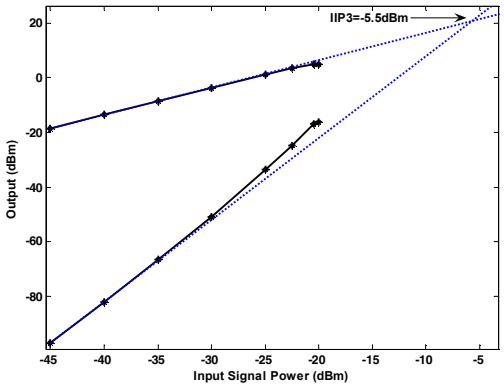
For further compensating, the series filter composed of R_{L2} and C_{L2}, is added at the output. Figure 2(c) shows the equivalent circuit for the CMFB loop of the front-end at the high frequencies. The $2C_{L1}$ is shorted so, the low frequency zero and pole are neglected for simplicity. Moreover R_{CM1} is ignored respect to R_{L1}. The loop gain in this case is:

$$A_{CLnew2} = \frac{-4g_{m5}R_{L1}(1+R_{L2}C_{L2}s)}{1+2(R_{L1}+R_{L2}/2)C_{L2}s} \times \frac{g_{mOP}R_{LOP}}{1+2(R_{LOP}+R_{BLO}/2)C_{CLO}s} \quad (3)$$

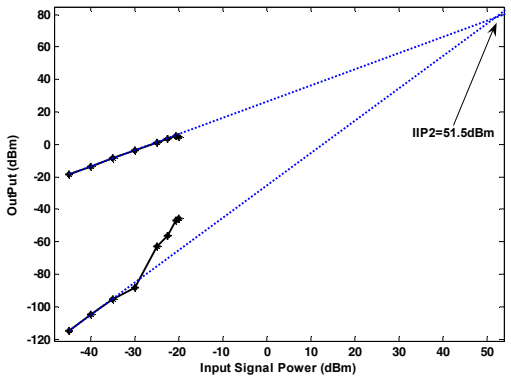
Like the previous equation, the second fraction does not change. Regarding the first fraction, the series branch imposes a high frequency pole and a zero (three times of the pole if R_{L1} is twice of R_{L2}) to the CMFB loop gain. Adding a pole before a zero to the loop gain will reduce the unity gain bandwidth accordingly; the higher phase margin will be obtained (lead-lag compensation). The series branch not only compensates the effect of the low frequency zero and pole on the unity gain bandwidth of the loop but also it is used as the second stage of the low pass filter at the output of the mixer.

III. SIMULATION RESULTS AND COMPARISON

A proposed technique is applied to the front-end of a zero IF UMTS prototype receiver. The circuit is designed using a 0.18µm CMOS technology with 1.2V supply voltage. Figure 3(a) shows the IIP3 two tone test results. The tones are in 2.143GHz and 2.144GHz while the 0dBm LO is in 2.14GHz. Simulation results show 26.5dB voltage conversion gain, 1dB compression point of -20.5dBm, and -5.5dBm IIP3. Figure 3(b) illustrates the second order nonlinear component at the output versus the power of input signal, while the 1.5% and 0.5% intentional mismatch have been respectively applied to the size of the active and passive elements in the circuit. The circuit however, shows +51.5dBm IIP2. In case of having no mismatch in the circuit, the IIP2 will increase by about 20dB. As mentioned before, the low frequency second order nonlinear components of the input devices are directed to the low impedance supply voltage through the $L_{1\text{-}2}$. Any residue of these components is upconverted to high frequency and could only leak to the output through the mismatch of the switches. Thus the mismatch of the switches and the load is the dominant source of IIP2.



(a)



(b)

Figure 3. The downconverted fundamental and (a) third order, and (b) second order intermodulated components at the output versus the power of the input signal.

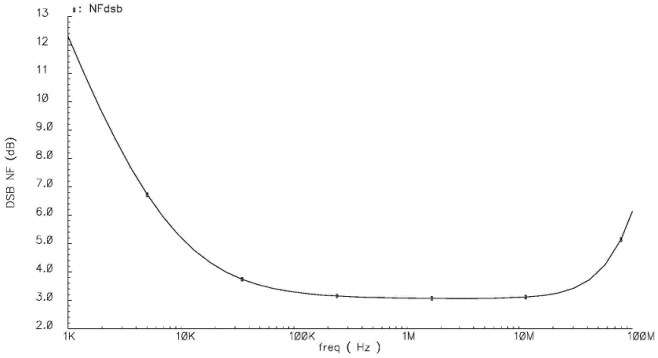


Figure 4. The Double side band NF of the RF front-end.

Double side band NF of the downconverter is depicted in Figure 4. The thermal NF of the front-end is 3.1dB and its flicker noise corner frequency is 6 kHz indicating the potential of the technique for applying to the low channel bandwidth applications.

The DC loop gain of the CMFB is about 40 dB and its ¬3dB bandwidth is about 5.5MHz. Simulation results show adding the series filtering branch to the circuit causes the unity gain bandwidth of the loop to be reduced from 660MHz to 220MHz and its phase margin to increase from 65 degree to 80 degree. Moreover the series branch causes more than extra 10dB blocker rejection at 140MHz away from the center of the channel. The circuit draws 4.5mA current from the 1.2V supply voltage (2.8mA by input transconductance, 1.2mA by the switches and 0.5mA by the OPAMP and biasing circuit).

Table I summarizes the performance of this circuit and the results of other published works. It is seen that, the NF, the flicker noise corner frequency and the power consumption of the proposed front-end is the least, and it provides comparable gain and nonlinearity performance, while it uses 1.2V supply voltage in a 0.18µm CMOS technology. The IIP2 of the circuit with assumed mismatch is the best, however if proper attention is paid during the layout to lower the mismatch further, the IIP2 of the front-end could be even better. The flicker noise of the circuit is considerably low due to the technique used in the design which shows the effectiveness of the approach in alleviating the problems of CMOS technology in zero IF receiver in low voltage applications.

IV. CONCLUSION

A new technique is proposed for designing the narrow band CMOS front-end. The current of the input transconductance directly drives the low flicker noise PMOS switches of the mixer. Two inductors connected to VDD provide the DC current path for the input transconductance and switches. They also absorb the parasitic capacitances of the switches at the operating frequency reducing the non-ideality components due to switches at the output. Due to fewer transistors in the stack the approach is more desirable for low voltage applications. Techniques have been used for the design of a low voltage and stable CMFB circuit. The output of the downconverter is a second order low pass passive filter comprising of series filtering and the usual parallel filtering. The series filtering branch not only relaxes the linearity of other subsequent stages but also; provides lead-lag compensation making the CMFB loop more stable.

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TABLE I. SUMMARY OF COMPARISON WITH OTHER PUBLISHED WORKS.

	Freqency (GHz)	Voltage Gain (dB)	IIP3 (dBm)	IIP2 (dBm)	1-dB CP (dBm)	NF (dB)	1/f corner (kHz)	Current cons. /Supply	Technology
[9]	5.15	29	-21	13	-	5.3	45	17.5mA/1.8V	0.18µm CMOS
[10]	5-6	26	-2	18	-	3.5	200	10m/1.2, 5m/2.5	0.13µm CMOS
[7]	1.8	31.5	-10.5	51	-	3.5	15	15mA/0.75V	90nm CMOS
[11]	2-8	23	-8	18	-	4.5	-	25.8mA/1.2V	65nm CMOS
[2]	0.5-7	18	-3	20	-	5.5	-	13.3mA/1.2V	65nm CMOS
[12]	0.6-10	14	0	20	-	7	-	25mA/1.2V	45nm CMOS
[This Work]	**2.14**	**26.5**	**-5.5**	**51.5**	**-20.5**	**3.1**	**6**	**4.5mA/1.2V**	**0.18µm CMOS**