A SAR ADC with an Efficient Threshold Voltage Generation

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***Abstract*—A new architecture is proposed in which with respect to the conventional successive approximation register (SAR) analog-to-digital converter (ADC), the switching power and capacitor area are significantly reduced without an appreciable increase in digital complexity. In the proposed scheme, the threshold voltage for each comparison is divided into two parts where producing these two parts consumes appreciably less switching energy and requires less total capacitance than the conventional one. With respect to the conventional scheme, the switching power and total capacitance of the proposed SAR ADC for 10 bit resolution is reduced by more than 87% and 40%, respectively.**

I. INTRODUCTION

One of the most important part of mixed analog-digital systems are the ADCs acting as the link between the analog and digital worlds. Each ADC configuration is suitable for some specific applications. Since SAR converters have a moderate speed, moderate resolution and low power consumption, they are one of the most suitable architectures for applications such as biomedical sensor interfaces and nodes of wireless sensor networks (WSNs). One of the most important parts of a SAR converter is the capacitive digital-to-analog converter (DAC) where a significant proportion of the power consumption and area of the converter is consumed. Many efforts have been done to reduce the amount of total capacitance of capacitive network and optimize the switching in DAC.

With respect to the conventional switching technique, the split-capacitor scheme [1] and the energy-saving technique [2], without any reduction in total capacitance, achieves 37% and 56% reduction in switching energy, respectively. However, these switching schemes improve the switching power consumption at the cost of increased digital switching complexity and power. The monotonic switching scheme [3] achieves 81% reduction in switching power and 50% reduction in total capacitance. The proposed scheme achieves 40% reduction in the total capacitance and about 87% reduction in switching power without a significant increase in the digital switching complexity.

The rest of this paper is organized as follows. Section II briefly explains the conventional SAR ADC operation. Section III explains the function of the proposed scheme. In Sect. IV the switching power of the proposed scheme is explained and finally in Sect. V, the circuit level simulation results of the proposed scheme for 10 bit resolution is presented.

II. CONVENTIONAL SAR ADC

The function of a conventional SAR ADC is explained in [4]. In this section the function of a conventional SAR ADC is briefly discussed. In Fig. 1 the circuit of a conventional SAR ADC is depicted. The conventional switching method uses the trial-and-error search procedure. At the sampling time, the input signal (V_{in}) is sampled. At this time the bottom plate of all capacitors is switched to V_{in} and the top plates of them is switched to the ground. After sampling time, at the holding phase, switch S_{R1} is open and the bottom plate of all capacitors is switched to the ground. So the voltage of the top plate of all capacitors (V_+) becomes $-V_{in}$. For the first comparison, the bottom plate of the largest capacitor (C_N) is switched to V_{REF}. So the voltage of the top plate goes to ($-V_{in}+V_{REF}/2$). Therefore in the first comparison, the input signal is compared with $V_{REF}/2$. If $V_{in}>V_{REF}/2$, the most significant bit (MSB) B1 is 1 and in addition to C_N, the bottom plate of C_{N-1} is also switched to V_{REF}. So, V_+ goes to ($-V_{in}+3V_{REF}/4$). But if $V_{in}<V_{REF}/2$, B1 is 0 and the bottom plate of C_N is returned to the ground and the bottom plate of C_{N-1} is switched to V_{REF}. So V_+ goes to ($-V_{in}+V_{REF}/4$). Therefore, depending on the first bit, in the second comparison, V_{in} is compared with $3V_{REF}/4$ or $V_{REF}/4$. The ADC repeats this procedure until the least significant bit (LSB) B_N is decided.

After sampling and holding phases, in N cycles, the input signal is estimated by comparing it with N threshold voltages where N is the resolution of the converter. In each comparison, with respect to the previous cycle, the threshold voltage is changed by adding or subtracting a binary weighted fraction of reference voltage to or from the previous threshold voltage. When a binary weighted fraction of V_{REF} is added to or subtracted from the threshold voltage, an Up or a Down transition occurs, respectively. Since in a conventional SAR ADC for any transition in the threshold voltage some charges are consumed from the reference voltage, all transitions in the

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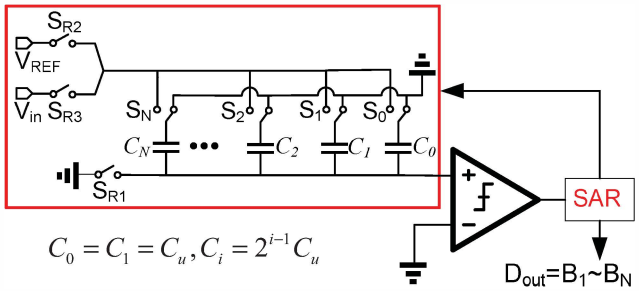

Fig. 1. A simplified circuit of a conventional SAR ADC

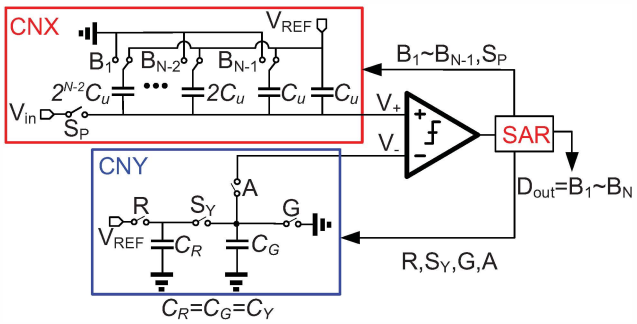

Fig. 2. The proposed SAR ADC.

threshold voltage in a conventional SAR ADC is power consuming. On the other hand, the energy consumption of an Up transition and a Down transition are not equal and the later consumes much more than the former [1]. For some cases, a Down transition consumes five times more energy than an Up transition [1]. In addition to two these points, since the DAC energy consumption is related to charging and discharging of the DAC capacitors, it is obvious that the switching power consumption is proportional to the total capacitance of DAC. Due to these simple facts, the proposed scheme appreciably decreases the switching energy of a SAR ADC. In the proposed scheme, firstly, the number of power consuming transitions is roughly reduced by 50%. Secondly, all Down transitions are omitted. Finally, the total capacitance is roughly 40% reduced. So, the total switching power consumption of the proposed scheme is significantly reduced.

III. Proposed SAR ADC Scheme

In a conventional SAR ADC, the required threshold voltage for generating the i^{th} bit (B_i) is $V_t[i]=\left(\alpha/2^i\right)V_{REF}$ where $1\le\alpha\le 2^i-1$. If we write the threshold voltage as the sum of two parts V_X and V_Y, it will lead to:

$$V_t[i]=V_X[i]+V_Y[i] \tag{1}$$

Considering $V_X[i]$ and $V_Y[i]$ as the following equations, makes a good efficiency in generation of the threshold voltages:

$$V_X[i]=\begin{cases}0 & i=1\\ V_X[i-1] & 2\le i\le N \;\&\; B_{i-1}=0\\ V_t[i-1] & 2\le i\le N \;\&\; B_{i-1}=1\end{cases} \tag{2}$$

$$V_Y[i]=\left(1/2^i\right)V_{REF} \tag{3}$$

As it is explained later, the generation of V_X and V_Y, could be more efficient than V_t which is used in a conventional SAR ADC. The circuit of the proposed SAR ADC is depicted in Fig. 2. As is seen, the circuit consists of two capacitive networks CNX and CNY that are corresponding to the V_X and V_Y threshold voltages, respectively.

In the proposed scheme, each cycle is composed of three phases. These phases are Reset (Res), Regeneration (Reg) and Comparison (Comp), respectively. At the sampling phase (first reset phase), the input signal is sampled on CNX. So at this time, switch S_P is close and the top plate of all capacitors in CNX is charged to V_{in}. The bottom plate of them is connected to V_{REF}. At the same time, in CNY, the capacitor C_R is reset to V_{REF} and C_G and the parasitic capacitor of the negative node of the comparator (C_P) are reset to the ground. After this phase, CNY is completely disconnected from the reference voltage so this capacitive network doesn't consume any more power. At the Reg phase, the charge on capacitors C_R and C_G are shared. So, the voltage of each of these two capacitors becomes $V_{REF}/2$. At the Comp phase, capacitor C_G is connected to the negative node of the comparator. So, at this phase, V_{in} is compared with $V_{REF}/2$. If $V_{in}>V_{REF}/2$, the first bit (B_1) is set to 1 and If $V_{in}<V_{REF}/2$, B_1 is set to 0. This is the end of the first cycle bit. At the beginning of the second bit cycle, if $B_1=1$ the bottom plate of the largest capacitor in CNX is switched to the ground and if $B_1=0$ there is no change in CNX.

After any comparison, the corresponding bit is produced. At the beginning of each cycle, according to the produced bit, the corresponding capacitor in CNX is switched to the ground or remains connected to V_{REF}. On the other hand, in CNY, after each bit generation, at the Res phase, the capacitor C_G and the parasitic capacitor of the negative node of comparator (C_P) is completely discharged. At Reg phase, two capacitors C_R and C_G are charge shared and therefore the voltage of C_R is halve. At the Comp phase, the capacitor C_G is connected to the comparator input and therefore the corresponding comparison is done. It is worth mentioning that since at the Reg phase, capacitors C_R and C_G are disconnected from the comparator, so, C_P doesn't affect the charge sharing between C_G and C_R, and hence, the voltage of C_R with a good accuracy is halved. But, at the Comp phase, C_P is charge shared with C_G. So, for a good accuracy it is necessary to make C_P minimal and use an appreciably larger capacitor for C_G with respect to C_P. The flow chart of the proposed successive approximation procedure is shown in Fig. 3. As is seen, because of some differences between the first reset phase and the other reset phases, the function of CNY in the first reset phase is remarked by Res 1 and in the other cycles is remarked by Res 2. The function of CNY at the regeneration and the comparison phases for all cycles is remarked by Reg and Comp, respectively. In Table 1, the switching procedure of CNY at each phase is illustrated. In Fig. 4 the timing

diagram for the proposed scheme for 10 bit resolution is illustrated. In this figure, the reset, regeneration and comparison phases are remarked by Φ_{Res}, Φ_{Reg}, and Φ_C, respectively. As it is clear, only four signals (R, G, A and S_Y) are required to control the switching of CNY. So, the digital section is not much more complex and power consuming than the conventional SAR ADC.

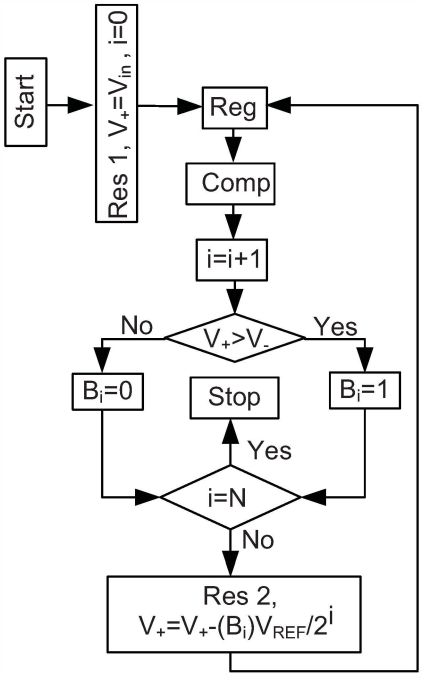

Fig. 3. Flow chart of the proposed SAR ADC.

Table 1: Switching procedure of CNY network.

Function name	Closed Switches of CNY
Res1	All switches except S_Y
Res 2	A, G
Reg	S_Y
Comp	A

IV. SWITCHING ENERGY OF THE PROPOSED SCHEME

As it is depicted in Fig. 2, CNX is similar to the conventional DAC, but, the total capacitance is 50% reduced and all 'Down' transitions are omitted. So, roughly 50% of transitions in a conventional switching procedure are eliminated. Also for generating MSB, there are no transitions in CNX. So, with respect to the conventional DAC, the power consumption of CNX is significantly reduced. In CNY, only at the first Reset phase, the capacitor C_R is charged up to V_{REF} and after this phase, the CNY network is disconnected from V_{REF}. Therefore, the total power consumption of CNY is $C_Y V_{REF}^2$ where C_Y is the capacitance of C_R and C_G.

The switching energy of CNX could be calculated as follows. After the i^{th} cycle, depending on the generated bit, the voltage of the positive node of the comparator could be changed or not. This voltage at the end of $(i\text{-}1)^{th}$ cycle and at the beginning of the i^{th} cycle is remarked by $V_+(t_i^-)$ and $V_+(t_i^+)$, respectively. It is obvious that $V_+(t_i^+) \le V_+(t_i^-)$. As explained in [1], the power consumption of CNX in each bit cycle could be calculated as follows:

$$i = 1 \Rightarrow E(i) = 0 \tag{4}$$

$$\begin{aligned} 2 \le i \le N \Rightarrow E(i) &= V_{REF}\left(Q_i(t_i^+) - Q_i(t_i^-)\right) \\ &= C_{Ti} V_{REF}\left(V_+(t_i^-) - V_+(t_i^+)\right) \\ &= C_{Ti} V_{REF}\left(V_X(i) - V_X(i-1)\right) \end{aligned} \tag{5}$$

where $E(i)$ is the energy consumption of CNX in the i^{th} bit cycle. C_{Ti} is the total capacitance of the capacitors in CNX which are connected to V_{REF} at the beginning of the i^{th} cycle. $Q_i(t_i^-)$ and $Q_i(t_i^+)$ are the charge stored on C_{Ti} at the end of the $(i\text{-}1)^{th}$ cycle and at the beginning of i^{th} cycle, respectively. $V_X(i)$ and $V_X(i-1)$ are defined by equations (1) and (2). According to equations (2) and (5), if $B_{i-1}=0$ the voltages $V_X(i-1)$ and $V_X(i)$ are equal and therefore there is no power consumption in CNX. A behavioral simulation of the switching power of the proposed scheme for 10 bit resolution and $C_Y=50C_u$ is done by MATLAB where C_u is the unit capacitance. The plot of the corresponding switching power consumption is depicted in Fig. 5. The average switching power of the proposed scheme is $177.75C_u V_{REF}^2$ which in comparison with a conventional switching scheme which consumes $1365.3C_u V_{REF}^2$, is about 87% more efficient.

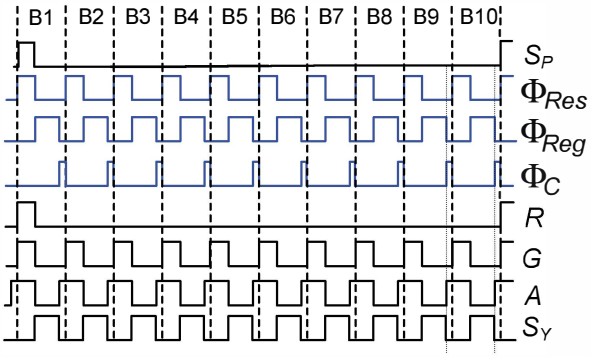

Fig. 4. Timing diagram of the proposed scheme for 10 bit resolution.

V. SIMULATION RESULTS

To verify the feasibility of the proposed scheme, a primary simulation of the proposed circuit is performed by HSPICE. In this simulation, a simple dynamic comparator shown in Fig. 6 is used. All switches in CNY except R are implemented by nMOS transistors and switch R is implemented by a pMOS transistor. In CNX, the sampling switch (S_P) is

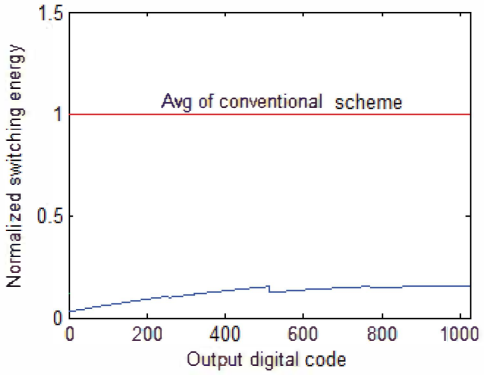

Fig. 5. Power consumption of the proposed scheme against output digital code for 10-bit SAR ADC in comparison with the conventional one.

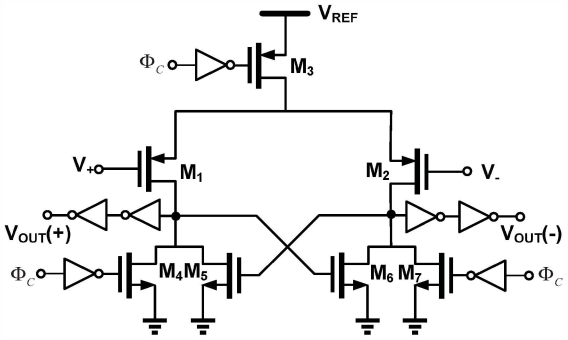

Fig. 6. Comparator circuit.

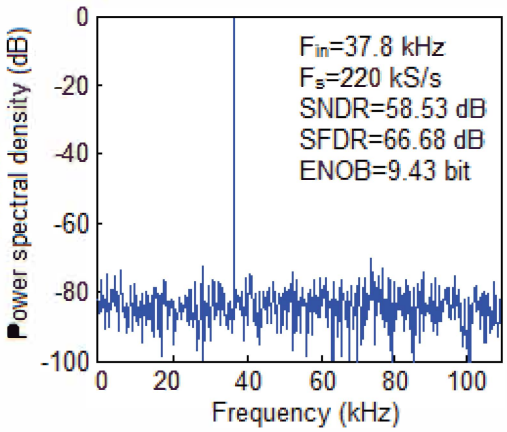

Fig. 7. FFT plot of ADC

implemented by a bootstrapping switch and the other switches are implemented similar to [3]. The ADC with 10 bit resolution, a sampling frequency of 220 kS/s and an input frequency of 37.8 kHz was simulated with HSPICE using a 0.13 µm CMOS process. The value of reference voltage is 1.2 V. The FFT plot for $C_Y = 50C_u$ and $C_u = 20$fF is illustrated in Fig. 7. In Table 2 the proposed scheme for 10 bit resolution is compared with some known schemes. It is worth mentioning that in this comparison, all schemes are considered as a single ended design. As is seen, for 10 bit resolution, the total switching power and capacitance of the proposed ADC is appreciably lower than the conventional, split capacitor and energy saving schemes. It also could be seen that although the total capacitance of the proposed ADC is a little more than the monotonic switching scheme, but, the total switching power consumption of the proposed technique is lower than the monotonic one.

VI. Conclusion

In this paper, a new SAR ADC scheme by dividing the threshold voltage into two parts was reported. Using this technique, for 10 bit resolution, the number of power consuming transitions and the total capacitance of DAC are significantly reduced. Also all Down transitions are omitted. These improvements could be achieved without a significant increase in digital switching complexity and power. All these points lead to a more power saving SAR ADC.

Table 2: Comparison the proposed scheme with some known schemes for 10 bit resolution.

Switching scheme	Number of switches	Total capacitor	Switching energy consumption
Conventional	25	$1024C_u$	$1365.3C_uV_{REF}^2$
Split capacitor [1]	43	$1024C_u$	$852.3C_uV_{REF}^2$
Energy saving [2]	41	$1024C_u$	$563.8C_uV_{REF}^2$
Set and down [3]	20	$512C_u$	$255.5C_uV_{REF}^2$
This work	23	$612C_u$	$177.75C_uV_{REF}^2$

References

[1] Ginsburg, B.P., and Chandrakasan, A.P.: "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC," *IEEE Int. Symp. on Circuits and Systems*, May 2005, pp. 184–187

[2] Chang, Y.,and Wang, C.: "A 8-bit 500-KS/s low power SAR ADC for bio-medical applications," IEEE Asian Solid-State Circuits Conf., 2007, Jeju, Korea, November 2007, pp. 228–231

[3] 1 Liu ,C.C. and Chang, S.J.: ' A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure' IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. 4, APRIL 2010,pp 731-740

[4] J. McCreary, and P.R. Gray, "All-MOS charge redistribution analog-todigital conversion techniques – Part-I", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-10, ,pp 371-379,December 1975

[5] Agnes ,A., Bonizzoni ,E., Malcovati ,P. and Maloberti ,F.: 'A 9.4-ENOB 1V 3.8µW 100kS/s SAR ADC with Time- Domain Comparator' in IEEE ISSCC Dig. Tech. Papers, Feb. 2008.

[6] Yu, W., Lin, J., and Temes, G.C.: 'Two-step split-junction SAR ADC', Electron. Lett., 2010, 46, pp. 211–212

[7] Hariprasath, V., and Guerber,J.: 'Merged capacitor switching based SAR ADC with highest switching energy-efficiency', Electron. Lett., 2010, 29th April 2010 Vol. 46

[8] Yu, W., Lin, J., and Temes, G.C.: 'Multi-step capacitor-splitting SAR ADC', Electron. Lett., 2010, 46, pp. 211–212

[9] Chen, Y., Tsukamoto, S., and Kuroda, T.: 'A 9b 100MS/s 1.46 mW SAR ADC in 65 nm CMOS'. IEEE Asian Solid-State Circuits Conf., Taipei, Taiwan, November 2009, pp.145-148

[10] Yoo, S., Park, J., Lee, S., and Moon, U.: 'A 2.5-V 10-b 120-MSample/s CMOS pipelined ADC based on merged-capacitor switching', IEEE Trans. Circuits Syst. II, 2004, vol. 51, pp. 269–275.