A Time-Based Analogue-to-Digital Converter for ECG Applications

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***Abstract*—This paper presents a low-power time-based analog-to-digital converter (ADC) for wearable electrocardiogram (ECG) sensor applications. In this work, by applying the difference between two consecutive samples to the input of the conventional voltage-to-time converter, the requirements on the high-frequency ramp signal will be relaxed and we can design for low power consuming implementation. The proposed approach reduces the converter complexity and generates a 1-bit data stream which leads to more power saving. The proposed circuit was designed and simulated in the 180 nm CMOS technology process, achieving a resolution of 10.4 bit and consumes 163 nW power with a supply voltage of 0.8 V.**

***Keywords*—Cardiovascular Disease, Analogue-to-Digital Converter, Electrocardiography, Voltage-to-Time Converter.**

I. Introduction

In recent years, cardiovascular disease (CVD), with a large percentage of death, is one of the biggest problems in the worldwide. The high importance of heart proper operation reveals the need for the constant and continuous care of the patient's heart. Electrocardiogram (ECG) sensors are one of the best choices for continuous monitoring of the heart condition, which from the last times many researches have been done about them [1-3]. Fig. 1 shows the simplified block diagram of a typical wearable ECG sensor used to amplify and digitize weak (1-100 μV) and low frequency (0.5-150 Hz) biomedical ECG signals [4]. Acquired ECG signals from the sensing electrodes are differentially amplified to common-mode noise suppression. Then being filtered by the band-pass filter to reject noise at frequencies out of the signal bandwidth and the notch filter at the frequency of (50/60 Hz) to attenuate the line power interference. The last block in the sensor system is an analog-to-digital converter (ADC), which is used to digitize the filtered signals [5]. In such applications, because of the limited power budget, the sensing system requires ultra-low power consumption. Therefore, the ability to design ultra-low power ADC while meeting the required performance parameters becomes a key design challenge.

Low power consumption, sample rate reduction, and convert resolution are highly important parameters of the ADC in wearable ECG acquisition circuits. One basic method to reduce the power consumption is to reduce the supply voltage, which reduces the voltage swing, and thus, limiting the dynamic range of the circuit. So to separate the dynamic range from the supply voltage, in many areas, including ADC circuits, time-based processing is used [6]. Given that the input signal is in the voltage domain, in order to perform time-based processing, a voltage-to-time converter block is required. This block also will face dynamic range constraints similar to voltage-based circuits.

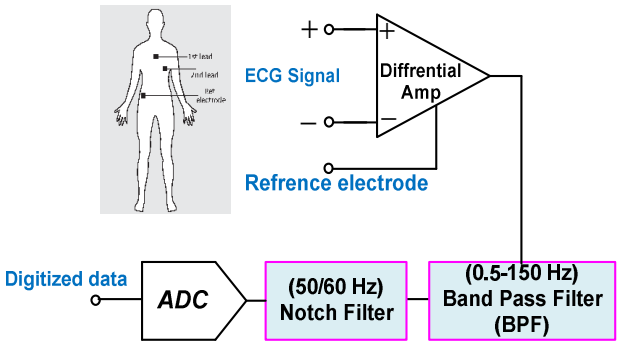

Fig. 1. Simplified block diagram of a typical wearable ECG sensor.

There are various types of time-based ADC circuits that operate based on time or frequency [6, 7]. The main disadvantage of them is requiring a high-frequency clock for proper operation. Other structures operate based on voltage-controlled delay cells with a large dynamic range. In such structures, the input signal is converted to time delay [8], but designing a voltage-controlled delay cell with high linearity and large dynamic range becomes a challenging task. Therefore, one of the main challenges is the design of optimal voltage-to-time converter for wearable ECG systems. In this paper, we present a new time-based ADC for wearable ECG sensors that achieves 10.4 bit resolution with 4 kHz sampling frequency and consumes 163 nW power from a 0.8-V supply voltage.

This paper is organized as follows. Section II will describe the background, structure, and small-signal analysis of the proposed time-based ADC. The architecture and circuit-level details of the proposed ADC will be discussed in Section III. Section IV presents the simulation results and Section V will conclude the paper.

II. Proposed Analogue-to-Digital Converter

A. Proposed Work

In a conventional voltage-to-time converter [6], as shown in Fig. 2, the input signal is compared with a linear slope waveform such as the ramp signal and generates a pulse width modulated (PWM) signal. Then the PWM waveform, by passing through a simple digital low-pass filter is converted into a digital value. This converter to proper operation requires a high-frequency ramp, much higher than the input frequency and the comparator must have a poor delay. These requirements lead to the implementation of a power-consuming structure.

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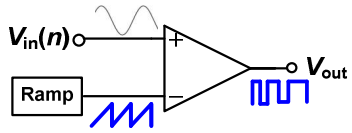

Fig. 2. Conventional voltage-to-time converter.

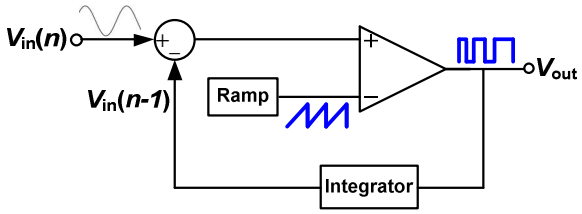

Fig. 3. Proposed voltage-to-time converter.

In this work to overcome the problems of the conventional voltage-to-time converter, the difference between two consecutive samples is applied to the input of the conventional voltage-to-time converter. Given that the difference between two consecutive samples is small, the requirements on the high-frequency ramp and comparator delay will be relaxed and we can design it for low power consuming implementation. The block diagram of the proposed voltage-to-time converter is shown in Fig. 3. In this structure, an integrator is used in the feedback path to convert the output PWM waveform into $V_{in}(n\text{-}1)$ voltage, which acts as a time-to-voltage converter. This voltage ($V_{in}(n\text{-}1)$) is subtracted from the input signal ($V_{in}(n)$) to generate the difference between two consecutive samples. Then the subtracted signal is compared with a ramp signal and generates the output PWM waveform.

B. Converter Transfer Function

In order to develop the small-signal model of the proposed converter, we need to define the transfer function of the ramp comparator. If we assume the ramp function as follows:

$$V_r(t) = V_{r,\max} \times \frac{t}{T_S} \tag{1}$$

where $V_{r,\max}$ and T_s are the maximum amplitude and time period of the ramp signal, respectively. According to Fig. 2, when the input signal, which is time sampled, is equal to the ramp signal, the output PWM waveform pulse width is equal to T[n]. So we have:

$$V_r(T[n]) = V_{r,\max} \times \frac{T[n]}{T_S} \tag{2}$$

$$V_{in}(n) = V_r(T[n]) \tag{3}$$

Therefore, the transfer function of the ramp comparator is defined as follows:

$$\frac{T[n]}{V_{in}(n)} = \frac{T_S}{V_{r,\max}} = \frac{1}{f_S \times V_{r,\max}} \tag{4}$$

where $f_s = 1/T_s$ denotes the ramp repeating frequency.

The complete small-signal model of the proposed time-based ADC is shown in Fig. 4. In this model, the PWM output of the converter is converted into the digital value by passing it through a digital integrator with a transfer function similar to the integrator in the feedback path. Although the linear s-domain model of the integrator is well known, at the circuit level an integrator will have a pole at ω_{int}.

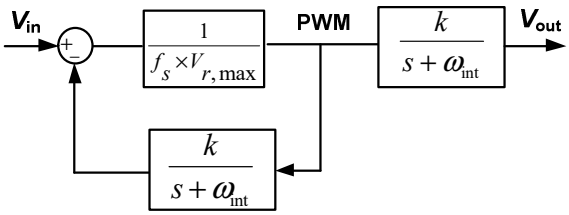

Fig. 4. Small-signal model of the proposed time-based ADC.

The transfer function of the proposed model is as follows:

$$G_{pwl} = \frac{PWM}{V_{in}} = \frac{\frac{1}{f_S \times V_{r,\max}}}{1 + \frac{1}{f_S \times V_{r,\max}} \times \frac{k}{s + \omega_{int}}} \tag{5}$$

Assuming that $s << \omega_{int}$, the total gain of the time-based ADC after the reconstruction can be written as follows:

$$G_{total} \approx \frac{\frac{1}{f_S \times V_{r,\max}}}{1 + \frac{1}{f_S \times V_{r,\max}} \times \frac{k}{s + \omega_{int}}} \times \frac{k}{s + \omega_{int}} \tag{6}$$

$$s << \omega_{int} \quad \Rightarrow \quad G_{total} \approx 1$$

III. Time-Based ADC Circuit Design

A. Overall Structure

The block diagram of the proposed ADC is shown in Fig. 5. This time-based ADC consists of a ramp generator, a subtractor, a comparator, which compares the subtractor output with the ramp signal and generates the PWM waveform, and a charge-pump circuit as the time-to-voltage converter in the feedback path. The ramp generator is synchronized with the reference clock of the circuit and determines the overall circuit sampling frequency. These blocks are explained in details in the following sections.

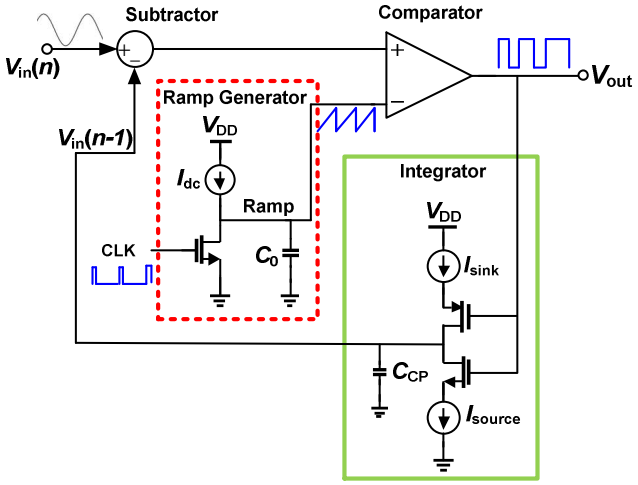

Fig. 5. Block diagram of the proposed ADC.

B. Ramp Generator Circuit

The ramp generator circuit which is shown in Fig. 6, consists of a cascode current source that charging capacitance C_0 by supplying it with a constant current. The discharging is controlled by the transistor M_0 which is

triggered by the CLK signal. So the output ramp signal is generated by charging and discharging of the C_0 capacitance which is controlled by the CLK signal. The noise performance of the circuit and the linearity of the generated ramp are the most important parameters in the design of the ramp generator circuit. Therefore, in order to circuit proper operation in low-frequency applications, the transistors M_1 and M_2 are designed with larger channel lengths to allow for reducing the flicker noise and biased at small g_m to reduce the thermal noise [9].

C. Comparator Circuit

The schematic of a high-performance comparator that uses the positive feedback to introduce hysteresis is shown in Fig. 7. It includes an input stage that provides hysteresis, a second stage to increase the output swing, and an output buffer to increase the drivability. Transistors M_1 and M_2 in the first stage are the input transistors that provide some gain for the input signal. Transistors M_3 and M_4 are the diode-connected loads. The cross-coupled transistors M_5 and M_6 form the positive feedback that introduces hysteresis.

D. Integrator Circuit

There are two possible ways to implement the integration function in the feedback path. One is by performing integration using an op-amp integrator and other one is by utilizing a charge-pump. Since the charge-pump implementation has fewer components, therefore leads to lower power consumption and an easier design for linearity [10]. Hence a charge-pump implementation is chosen in this design.

The feedback integrator circuit is shown in Fig. 8. It shows a simple charge-pump circuit, with a capacitor C_{CP}, and equal charging and discharging currents, I_{sink} and I_{source}, respectively. Since the main component of any charge-pump circuit is the current mirror. So we have used a self-biased high-swing cascode current mirror because of its high output impedance and efficient work in very low bias current.

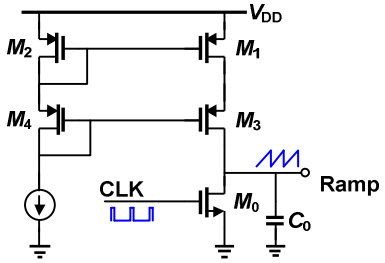

Fig. 6. Ramp Generator circuit.

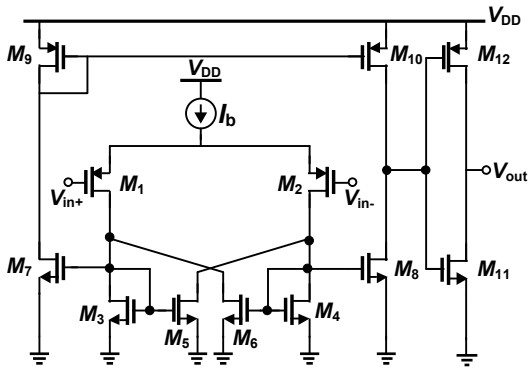

Fig. 7. Comparator circuit.

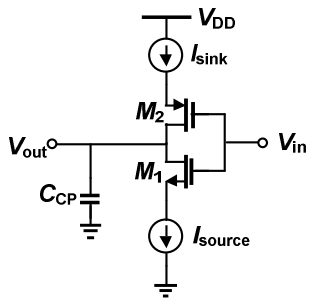

Fig. 8. Integrator circuit.

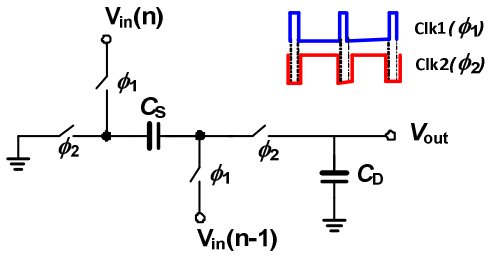

Fig. 9. Subtractor circuit.

E. Subtractor Circuit

Since the conventional analog subtractor with an operational amplifier consumes static power [11], the low power subtractor of Fig. 9 is used. The control signals of the subtractor are Clk1 and Clk2 derived from the system clock (CLK), where Clk2 is a nonoverlapping inverted replica of Clk1. First during phase ϕ_1, sampling capacitor C_S is connected between $V_{in}(n)$ and $V_{in}(n\text{-}1)$, so this capacitor has the charge of $V_{in}(n) - V_{in}(n\text{-}1)$. Then during phase ϕ_2, C_S is switched to ground and C_D holds the difference voltage on the output node. This circuit has lower parts and low supply current than differential amplifiers and is suitable for low power applications.

F. Control Signals

The timing diagram of the control signals for the proposed ADC is shown in Fig. 10. The involved control signals are Clk1 and Clk2 which are derived from the system CLK signal using a conventional non-overlapping clock generator circuit. When the CLK signal is low, the ramp generator circuit generates a ramp signal, and when the Clk2 signal becomes high, the subtractor circuit updates its output value. The subtractor output signal and the generated ramp signal are then compared to each other in order to produce the output PWM waveform.

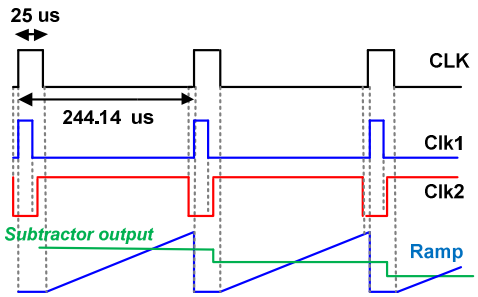

Fig. 10. Timing diagram of the control signals

IV. Simulation Results

The proposed time-based ADC was designed in TSMC 180 nm CMOS process and simulated in Cadance to obtain its performance parameters. In order to reduce power consumption, the circuit operates with a low supply voltage of 0.8 V and consumes 163 nW power. The sampling frequency of the ADC is determined by the ramp repetition frequency (CLK frequency) which is 4 kHz for this design.

Simulation results of the system's different nodes, including sinusoidal input signal, subtractor output, ramp generator output signal, and PWM output of the converter are shown in Fig. 11. The input voltage changes from –150 mV to150 mV and the ramp generator generates the ramp signal which its slope is proportional to the difference voltage between two consecutive samples. Then the difference signal is compared with the ramp signal and generates the output PWM waveform.

The proposed ADC is first tested using a 300 mV full-swing 11 Hz sinusoidal input signal [12]. The FFT simulation result after reconstructing the input signal from the PWM output is shown in Fig. 12. The simulated signal-to-noise and distortion ratio (SNDR) is 64.5 dB and the proposed ADC achieves 10.4 bit resolution. To demonstrate the proper working of the proposed converter, its performance is evaluated based on the sample realistic heartbeat record obtained from the MIT-BIH arrhythmia database [13]. The reconstructed ECG signal of the modulator output is shown in Fig. 13.

In order to verify the performance of this circuit, simulation results in different process corner cases, temperature and power supply variations are summarized in Table I. According to the simulation results, the proposed ADC achieves 64.5 dB ± 11.5 dB SNDR and 163 nW ± 14 nw power consumption over process (SS, TT, FF), voltage (0.72V, 0.8V, 0.88V), and temperature (-40°C, 27°C, 85°C) variations with a 4 kHz sampling frequency.

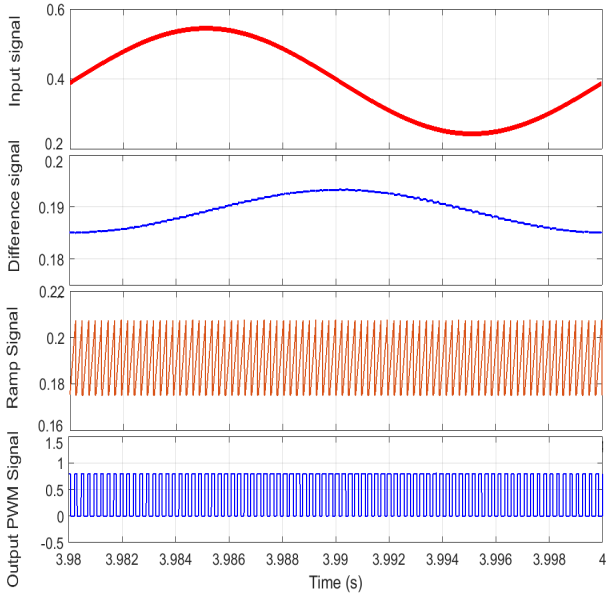

Fig. 11. Simulation result of the system different nodes.

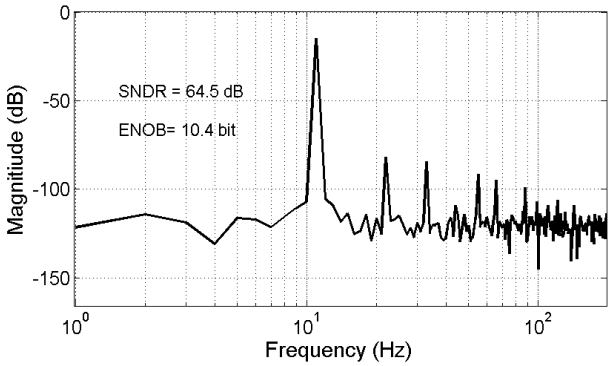

Fig. 12. 4096-point FFT result with a 11 Hz sinusoidal input signal.

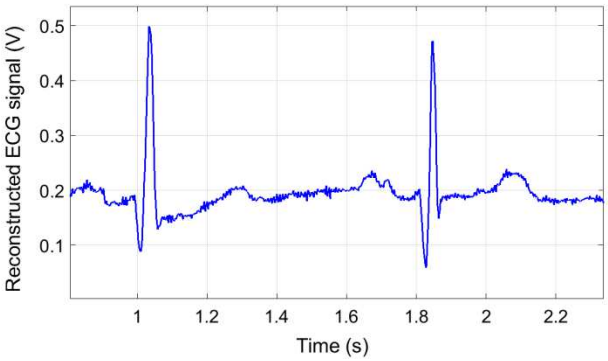

Fig. 13. Reconstructed ECG signal.

Table I. Performance summary of the simulated time-based ADC.

Parameter	TT @ 27°C, 0.8 V	FF @ -40°C, 0.88 V	SS @ 85°C, 0.72 V
SNDR (dB)	64.5	70	53.1
ENOB (bit)	10.4	11.3	8.5
Power dissipation (nW)	163	175	149
Sampling rate	4 kHz		
Technology	180 nm CMOS		

The comparison result of the proposed ADC with some previously reported converters in similar applications is shown in Table II. As can be seen in this table, by using the proposed structure, the power consumption of the converter is significantly reduced. Also, the sampling rate of 4 kS/s is lower than the corresponding value in SAR and time-based ADCs, which results in power saving in the transmission of data from ADC to processor (data rate). The proposed converter can achieve the required resolution of 10.4 bit for ECG systems.

V. Conclusion

In this work, we have presented a new time-based ADC for wearable ECG applications. The circuit is composed of the ramp generator, comparator, charge-pump integrator, and subtractor leading to less design complexity and lower power consumption. The proposed circuit generates a 1-bit data stream which leads to data rate reduction and more power saving in the transmitter.

Table II. Performance comparison with other related works.

Parameter	TBCAS'14 [12]	AICSP'19 [14]	JMS'19 [15]	TBCAS'19 [16]	JSSC'18 [7]	MEJO'20 [17]	This Work
Application	ECG	ECG, EEG	ECG	EEG	EAP	ECG	ECG
Technique	Event-Driven ADC	SAR ADC	Level-Crossing ADC	SAR ADC	Time-Based ADC	SAR ADC	Time-Based ADC
Technology (nm)	130	180	180	180	65	65	180
Resolution (bit)	4.4	9.3	9	10	8.3	9.4	10.4
Sampling rate (S/s)	---	5 k	10 k	20 k	----	10 k	4 k
Supply voltage (V)	0.3	1	0.8	1	0.5	1.2	0.8
SNDR (dB)	28.3	57.59[b]	57.5	57.6	51.78	58.4	64.5
Power (µW)	0.22[a]	0.420	0.367	0.5	1.2	0.060	0.163
Sim./Meas.	Meas.	Sim.	Sim.	Meas.	Meas.	Meas.	Sim.

[a] ADC and QRS detection: measured in 50 Hz input. [b] SQNR is reported

REFERENCES

[1] X. Zou, X. Xu, L. Yao, and Y. Lian, "A 1-V 450-nW fully integrated programmable biomedical sensor interface chip," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1067-1077, April. 2009.

[2] R. F. Yazicioglu, S. Kim, T. Torfs, H. Kim, and C. Van Hoof, "A 30µW Analog Signal Processor ASIC for Portable Biopotential Signal Monitoring," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 209-223, Jan. 2011.

[3] R. Mohan, S. Zaliasl, G. G. Gielen, C. Van Hoof, R. F. Yazicioglu, and N. Van Helleputte, "A 0.6-V, 0.015-mm2, Time-Based ECG Readout for Ambulatory Applications in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no.1, pp. 298-308, Jan. 2017.

[4] F. Cannillo, E. Prefasi, L. Hernández, E. Pun, F. Yazicioglu and C. Van Hoof, "1.4V 13µW 83dB DR CT-ΣΔ modulator with Dual-Slope quantizer and PWM DAC for biopotential signal acquisition," *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC'11)*, Sep. 2011, pp. 267-270.

[5] J. Xiang, Y. Dong, X. Xue, and H. Xiong, "Electronics of a Wearable ECG With Level Crossing Sampling and Human Body Communication," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 1, pp. 68-79, Feb. 2019.

[6] S. Naraghi, M. Courcy, and M. P. Flynn, "A 9-bit, 14µW and 0.06mm2 pulse position modulation ADC in 90 nm digital CMOS," *IEEE J. Solid-State Circuits,* vol. 45, no. 9, pp. 1870–1880, Sep. 2010.

[7] L. B. Leene, and T. G. Constandinou, "A 0.006 $mm^2$1.2µW Analog-to-Time Converter for Asynchronous Bio-Sensors," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2604-2613, Sept. 2018.

[8] H. Pekau, A. Yousif, and J. W. Haslett, "A CMOS integrated linear voltage-to-pulse-delay-time converter for time-based analog-to-digital converters," *in Proc. ISCAS,* 2006, pp. 2373–2376.

[9] F. A. Levinzon and L. K. J. Vandamme, "Comparison of 1/f noise in JFETs and MOSFETs with several figures of merit," *Fluctuation Noise Lett.*, vol. 10, no. 4, pp. 447-465, Dec. 2011.

[10] R. Mohan, S. Hiseni and W.A. Serdijn, "A Highly Linear, Sigma-Delta Based, Sub-Hz High-Pass Filtered ExG Readout System," *in Proc. IEEE ISCAS*, 2013, pp. 181-184.

[11] S.-J. Kim, L. Liu, L. Yao, W. L. Goh, Y. Gao, and M. Je, "A 0.5-V sub-µW/channel neural recording IC with delta-modulation-based spike detection," *in Proc. IEEE ASSCC,* Nov. 2014, pp. 189–192.

[12] X. Zhang and Y. Lian, "A 300-mV 220-nW event-driven ADC with real-time QRS detection for wearable ECG sensors," *IEEE Trans. Biomed. Circuits Syst*., vol. 8, no. 6, pp. 834-843, Dec. 2014.

[13] Physionet.(2013,Aug.).[Online].Available:http://www.physionet.orglcgi-bin/atrn! ATM.

[14] M. Nasserian, A. Peiravi, and F. Moradi, "An Adaptive-Resolution Signal-Specific ADC for Sensor-Interface Applications," *Analog Integrated Circuits, and Signal Processing*, vol.98, no.1, pp. 125-135, 2019.

[15] A. Antony, S. R. Paulson, and D. J. Moni, "Asynchronous Adaptive Threshold Level Crossing ADC for Wearable ECG Sensors," *Journal of Medical Systems*, vol. 43, no. 3, pp. 78, 2019.

[16] M. Tohidi, J. Kargaard Madsen and F. Moradi, "Low-power high-input-impedance EEG signal acquisition SoC with fully integrated IA and signal-specific ADC for wearable applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 6, pp. 1437-1450, Dec. 2019.

[17] L. Wang, C. Zhang, J. Wang, R. Ma, Z. Zhu, "A 10-bit SAR ADC using novel LSB-first successive approximation for reduced bitcycles," *Microelectron. J.*, vol. 103, Sep. 2020.

[18] S. Barati and M. Yavari, "An Adaptive Continuous-Time Incremental SΔ ADC for Neural Recording Implants," *International Journal of Circuit Theory and Applications*, vol. 47, no. 2, pp. 187-203, Feb. 2019.