A Novel Topology in RNMC Amplifiers with Single Miller Compensation Capacitor

Majid Jalalifar*, Mohammad Yavari**, and Farshid Raissi*

*Department of Electrical Engineering, K.N. Toosi University of Technology, Tehran, Iran
E-mails: mjalalifar@ee.kntu.ac.ir , raissi@kntu.ac.ir

**Department of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran
E-mail: myavari@aut.ac.ir

***Abstract*— This paper presents a reversed single active Miller compensation (RSAMC) technique for low-voltage and large capacitive load three-stage amplifiers. In this scheme, only one active compensation capacitor is employed. The main advantages of the proposed compensation method are the enhanced unity gain bandwidth and reduced silicon die area of the amplifier compared to those of the existing proposed techniques in reversed nested Miller compensation (RNMC) scheme. The simulation results with a 0.18µm standard CMOS process achieve 27MHz unity gain bandwidth and 60 degree phase margin for the proposed RSAMC amplifier, while driving 500 pF load from a single 1.5 V power supply.**

I. Introduction

Multistage amplifiers are widely used in the analog and mixed signal circuits to achieve high dc gain and large output signal swing simultaneously, because, although cascoding of transistors is a well-known technique to increase the dc gain in single-stage amplifiers, however, it is not possible in recent sub-micron CMOS technologies due to the reduced power supply voltage dictated by technology scaling. Nonetheless, multistage amplifiers have additional frequency poles and zeros resulting in inherently instability and reduced signal bandwidth if any frequency compensation technique is not employed.

There are generally two different compensation schemes in the three-stage amplifiers: nested Miller compensation (NMC) and reversed nested Miller compensation (RNMC) [1]-[5]. An RNMC amplifier usually has a higher bandwidth than the NMC one since in the RNMC amplifier the inner compensation capacitor does not load the amplifier's output. However, the RNMC scheme has the stability problem because of appearing a right half plane (RHP) zero in its frequency response. To alleviate this problem, many RNMC techniques have been reported which are basically canceling the RHP zero such as the RNMC amplifier with voltage buffer and nulling resistor [1], reversed active feedback frequency compensation (RAFFC) [2], RNMC with voltage buffer and resistor [3], RNMC techniques with current follower (CF) and voltage follower (VF) [4], [5].

In this paper, a novel frequency compensation technique called reversed single active Miller compensation (RSAMC) is proposed for three-stage amplifiers. This scheme of compensation uses only one active compensation capacitor and yields a higher amplifier bandwidth.

The paper is organized as follows. In Sect. II, the proposed RSAMC amplifier is described. The circuit implementation and the simulation results of the proposed amplifier are presented in Sect. III. Finally, Sect. IV concludes the paper.

II. The Proposed Technique

In this paper, a new technique in the frequency compensation of three-stage amplifiers called the *reversed single active Miller compensation* (RSAMC) is proposed. Figure 1 shows the basic block diagram of this technique where g_{mi}, C_i, and R_i represent the i^{th} stage transconductance, the equivalent parasitic capacitance, and the output resistance of the corresponding gain stages, respectively. R_b is the input resistance of current buffer stage. C_L and R_L are the loading capacitor and resistor, respectively. Besides, the proposed structure has an active feedback which consists of a current buffer stage, g_{mb}, to improve the bandwidth, and only one compensation capacitor, C_m. An additional transconductance stage, g_{mf}, is also used between the output of the first stage and the amplifier's output. This forms a push-pull stage at the output node that improves the transient response of the amplifier.

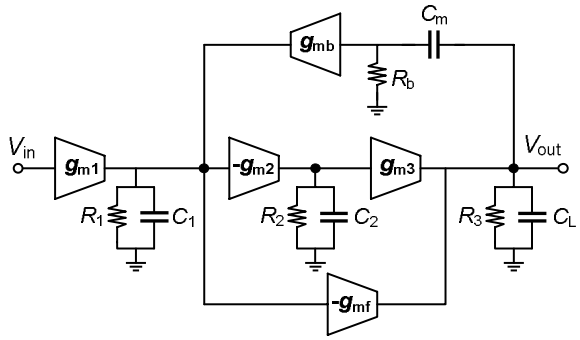

Fig. 1: Proposed reversed single active Miller capacitor topology.

Assuming that C_L and $C_m >> C_i$, and also $g_{mi}R_i$, $g_{mf}R_L$ and $g_{mb}R_1 >> 1$, and by considering $g_{mb} \approx 2/R_b$, the small-signal

transfer function of RSAMC amplifier can readily be obtained as follows:

$$A_v(s) = A_0 \frac{1 + s\left[\frac{2C_m}{3g_{mb}} + \left(\frac{g_{mf}}{g_{m2}g_{m3}}\right)C_2\right] + s^2 \frac{2g_{mf}}{3g_{m2}g_{m3}g_{mb}} C_m C_2}{\left(1 + \frac{s}{\omega_{P1}}\right)\left[1 + s\frac{g_{mf}}{g_{m2}g_{m3}}C_2 + s^2 \frac{C_2 C_L}{g_{m2}g_{m3}g_{mb}R_1}\right]} \quad (1)$$

where $A_0 = g_{m1}g_{m2}g_{m3}R_1R_2R_3$ is the dc gain, and $\omega_{P1} \cong 3/2C_m g_{m2}g_{m3}R_1R_2R_3$ the dominant real pole. Hence, the gain-bandwidth (GBW) of the amplifier is simply given by:

$$GBW = A_0.\omega_{P1} = \frac{3g_{m1}}{2C_m} \quad (2)$$

In order to achieve a class AB push-pull output stage and hence to improve the amplifier's slew rate (as will be shown in the circuit implementation of the proposed amplifier), the transconductance of the third stage, g_{m3}, can be set equal to that of the feedforward path, g_{mf}. This simplifies the amplifier's small signal transfer function as follows:

$$A_v(s) = A_0 \frac{1 + s\left[\frac{2C_m}{3g_{mb}} + \frac{C_2}{g_{m2}}\right] + s^2 \frac{2C_m C_2}{3g_{m2}g_{mb}}}{\left(1 + \frac{s}{\omega_{P1}}\right)\left[1 + s\frac{C_2}{g_{m2}} + s^2 \frac{C_2 C_L}{g_{m2}g_{m3}g_{mb}R_1}\right]} \quad (3)$$

The other zeros and non-dominant poles of the RSAMC amplifier can be obtained from relation (3) as follows:

$$\omega_{Z1} = -\frac{3g_{mb}}{2C_m} \quad (4)$$

$$\omega_{Z2} = -\frac{g_{m2}}{C_2} \quad (5)$$

$$\omega_{P_{2,3}} = -\frac{g_{m3}g_{mb}R_1}{2C_L}\left(1 \pm j\sqrt{1 - \frac{4g_{m2}C_L}{g_{m3}g_{mb}C_2R_1}}\right) \quad (6)$$

As is clear, there are two left half plane zeros which one of them occurs at a lower frequency than the other one. Besides, there are two complex non-dominant poles. The presence of two LHP zeros leads to an extra phase margin which improves the stability of the RSAMC amplifier.

By using a third-order Butterworth response in order to arrange the non-dominant poles of the RSAMC amplifier similar to that described in [6], the value of compensation capacitor, C_m, is given by

$$C_m = \frac{3g_{m1}}{g_{m2}} C_2 \quad (7)$$

Moreover, we get:

$$g_{mb} = \frac{2g_{m2}C_L}{g_{m3}C_2R_1} \quad (8)$$

According to (7), the compensation capacitor, C_m, is not related to the load capacitor, C_L. This helps us to decrease the compensation capacitor, C_m, significantly without any stability concern especially in large capacitive load applications. Moreover, a small g_{m1} and a large g_{m2} can be used to decrease the value of C_m further. However, this may increase the amplifier's power dissipation.

Since the order of the numerator of $A_v(s)$ in relation (3) is less than that of its denominator, the stability of the amplifier is basically determined by the denominator. Then, by applying the Routh–Hurwitz stability criterion as described in [2] on the characteristic equation (3), the following stability condition is obtained:

$$GBW < \frac{g_{m3}\, g_{mb}\, R_1}{C_L} \quad (9)$$

As is seen from (9), for a given load capacitance, C_L, the GBW can be increased by choosing a large g_{mb} or g_{m3}. However, since the large g_{m3} leads to high power dissipation, g_{mb} is used as an important design parameter in enhancing the GBW. It should be noted that g_{mb} can be made larger without considerable increasing in the power consumption because the current buffer stage does not need to drive the large load capacitance unlike the output stage.

III. Simulation Results

To prove the effectiveness of the proposed compensation technique, HSPICE simulation results are carried out using a 0.18-µm BSIM3v3 level 49 CMOS technology. The amplifier was designed to achieve a dc gain of about 100 dB and a phase margin of 60° with a capacitive load of 500 pF and a 1.5 V power supply.

The circuit realization of the proposed three-stage RSAMC amplifier is shown in Fig. 2. The first gain stage is realized by transistors M0–M8 with a pMOS input differential pair which is a folded cascode amplifier. The second inverting stage is implemented by a common source amplifier with an active load comprising of M9 and M10. The last non-inverting stage is realized by transistors M11-M14. Moreover, the g_{mb} compensation stage is simply realized by transistor M6 of the folded cascode input stage. Finally, the feedforward transconductance stage g_{mf} is realized through M14.

The designed circuit parameters of RSAMC amplifier is shown in Table I. The unity gain frequency is set at about 27.3 MHz. According to (7), the Miller capacitance C_m can be 0.7pF. To achieve the targeted gain-bandwidth product, we set g_{m1}=101 µA/V. From (8), g_{mb}=205 µA/V. Then, we set g_{m2}=g_{m3}=g_{mf}=345 µA/V.

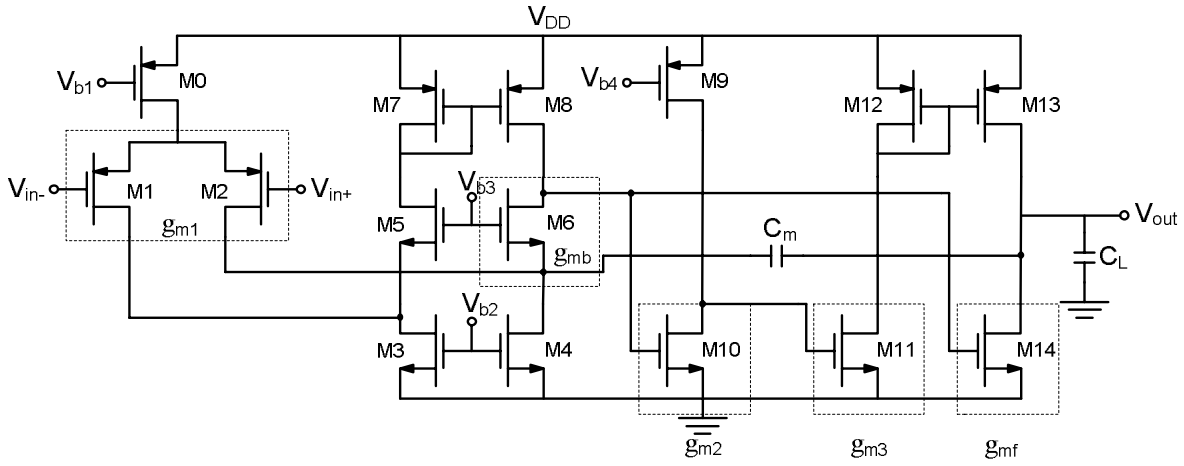

Fig.2: Circuit implementation of a three-stage RSAMC amplifier.

The simulated dc gain, gain-bandwidth product and phase margin are equal to 99.5 dB, 27.3MHz and 59.5°, respectively. The total current dissipation is 160 µA. Figure 3 shows the simulated open-loop frequency response whereas in Fig. 4 the large signal transient response of the amplifier in a unity-gain negative feedback configuration to a 400-mV input step is shown. Figure 5 shows the small signal characteristic of the amplifier in a unity-gain configuration to a 40-mV input step. Table II summarizes the simulation results of the proposed three stage amplifier.

Two figures of merit have been proposed to characterize and compare the small signal (GBW) and the large signal (slew rate) behaviors of different three-stage amplifiers [7], which are given by, respectively:

$$IFOM_S = \frac{GBW \times C_L}{I_{dd}} \tag{10}$$

$$IFOM_L = \frac{SR \times C_L}{I_{dd}} \tag{11}$$

By using these formulas, the higher figure of merit shows the better performance of the amplifier. Table III summarizes the performance results of few recently published three-stage amplifiers as well as the proposed one in this paper. As is seen, the proposed amplifier outperforms all of the amplifiers listed in Table III.

TABLE I
CIRCUIT PARAMETERS

Parameter	Value
M0	2×(6.55/0.36)
M1,M2	7/ 0.36
M3,M4	2×(3/0.36)
M5,M6	3/0.36
M7,M8	1.2/0.36
M9	3×(5.1/0.36)
M10	2/ 0.36
M11,M14	2/ 0.36
M12,M13	9/ 0.36

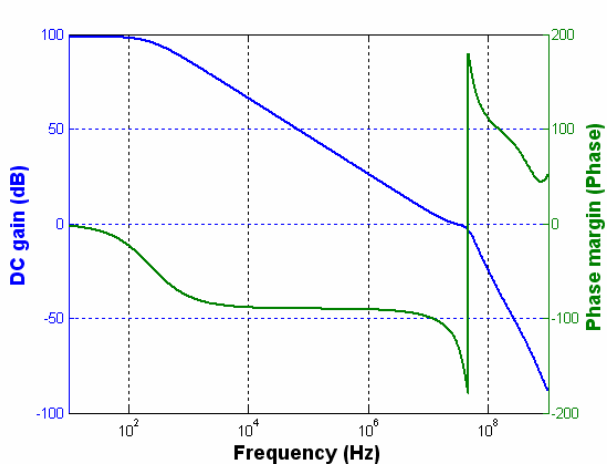

Fig. 3: Simulated open-loop frequency response of the amplifier.

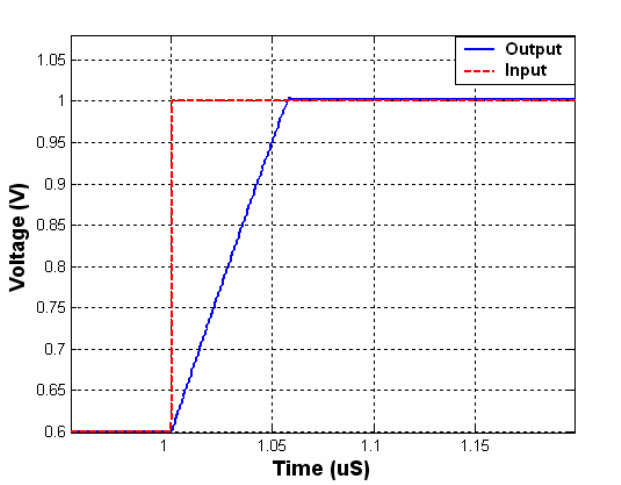

Fig. 4: Simulated large signal transient response of the amplifier.

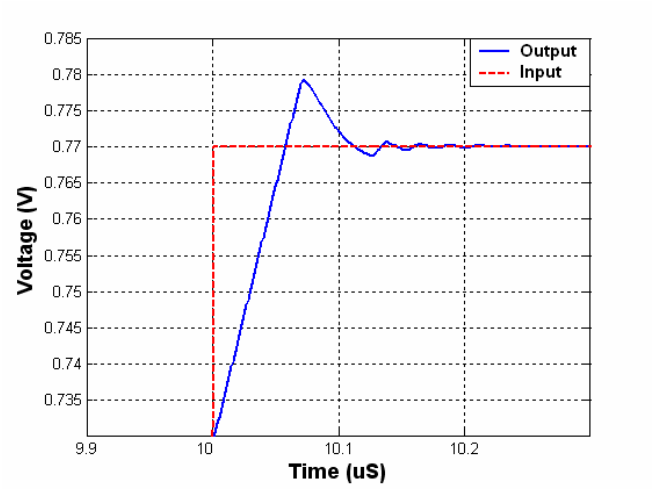

Fig. 5: Simulated small-signal transient response.

TABLE II
PERFORMANCE SUMMARY OF SIMULATED AMPLIFIER

Parameter	Value
Gain (dB)	99.5
GBW (MHz)	27.27
Phase Margin (degree)	59.4
Power (µW)	237
Total Current (mA)	0.16
T_S (µs) +/–	0.58/0.43
SR (V/µs) +/–	0.72/0.97
SR (V/µs) (average)	0.845
$IFOM_S$ (MHz×pF/mA)	85218
$IFOM_L$ (V/µs×pF)/mA	2640
C_m (pF)	0.7
V_{DD} (V)	1.5
C_L (pF)	500
Technology	BSIM3v3 Level 49 0.18-µm CMOS

IV. Conclusions

In this paper, a novel compensation scheme called RSAMC for three stage amplifiers was proposed. It was shown that a larger bandwidth compared to the other reported topologies can be obtained by using only one compensation capacitor as is used in the RSAMC amplifier. Furthermore, by using the active capacitance as the Miller compensation the die area of the amplifier is reduced significantly since its value can be selected very small. In general, the proposed technique achieves the largest $IFOM_S$ compared to the other reported compensation topologies.

References

[1] K. -P. Ho, C. -F. Chan, C. -S. Choy, and K. -P. Pun, "Reversed nested Miller compensation with voltage buffer and nulling resistor," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1735-1738, Oct. 2003.

[2] A. D. Grasso, G. Palumbo, and S. Pennisi, "Active Reversed Nested Miller Compensation for Three-Stage Amplifiers," *Proc. ISCAS'06*, vol. 1, pp. 911-914, May 2006.

[3] A. D. Grasso, D. Marano, G. Palumbo, and S. Pennisi, "Improved reversed nested Miller frequency compensation technique with voltage buffer and resistor," *IEEE Trans. Circuits and Systems-II*, vol. 54, no. 5, May 2007.

[4] R. Mita, G. Palumbo, and S. Pennisi, "Reversed nested Miller compensation with current follower," *Proc. ISCAS*, pp. 308-311, May 2001.

[5] G. Cataldo, R. Mita, G. Palumbo, and S. Pennisi, "Reversed nested Miller compensation with voltage follower," *Proc. ISCAS*, pp. 827-830, May 2002.

[6] H. Lee and P. K. T. Mok, "Active-feedback frequency compensation technique for low power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 511–520, Mar. 2003.

[7] X. Peng and W. M. Sansen, "AC boosting compensation scheme for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, Vol. 39, pp. 2074-2077, Nov. 2004.

[8] X. Fan, C. Mishra, E. Sanchez-Sinencio, "Single Miller Capacitor Frequency Compensation Technique for Low power Multistage Amplifiers," *IEEE J. Solid-State Circuits*, Vol. 38, pp. 1735-1738, Oct. 2003.

[9] J. Ramos, X. Peng, M. Steyaert, and W. Sansen, "Three stage amplifier frequency compensation," in *Proc. European. Solid-state Circuits Conf.* Lisbon, Portugal, Sept. 2003, pp. 365–368.

[10] H. Lee, K. N. Leung, and P. K. T. Mok, "A dual-path bandwidth extension amplifier topology with dual-loop parallel compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1739–1744, Oct. 2003.

TABLE III
COMPARISON OF DIFFERENT MULTISTAGE AMPLIFIERS

	C_L (pF)	V_{DD} (V)	I_{TOT} (mA)	Power (µW)	GBW (MHz)	SR (V/µs)	Capacitor (pF)	$IFOM_S$ (MHz×pF)/mA	$IFOM_L$ (V/µs×pF)/mA	Technology µm-CMOS
RNMCVBNR [1]	15	3	0.48	1.44	19.46	13.8	C_{m1}=3 C_{m2}=0.7	608	430	-
RAFFC [2]	500	2	0.12	0.24	1.75	1.52	C_{m1}=11.5 C_{m2}=0.5	7291	6333	0.6 µm
AFFC [6]	120	2	0.2	0.4	4.5	1.49	C_{m1}=5.4 C_{m2}=4	2700	894	0.8 µm
ACBCF [7]	500	2	0.162	0.324	1.9	1.0	C_{m1}=10 C_{m2}=3	5864	3086	0.35 µm
SMFFC [8]	120	2	0.21	0.42	9	3.4	C_m=4	5143	1943	0.5 µm
PFC [9]	130	1.5	0.19	0.275	2.7	1.0	C_{m1}=15 C_{m2}=3	1915	709	0.35 µm
DLPC [10]	120	1.5	0.22	0.33	7.0	3.3	C_{m1}=4.8 C_{m2}=2.5	3818	1800	0.6 µm
RSAMC	**500**	**1.5**	**0.16**	**0.237**	**27.27**	**0.845**	**C_m=0.7**	**85218**	**2640**	**0.18 µm**