A Novel Topology in Reversed Nested Miller Compensation Using Dual-Active Capacitance

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***Abstract*— A novel three-stage amplifier topology for low-voltage and large capacitive load applications is proposed. This scheme is called the dual-active capacitance in reversed nested Miller compensation (DACRNMC). The frequency bandwidth of the DACRNMC amplifier is improved due to the usage of active compensation capacitors. The amplifier's die area is reduced compared to the existing techniques in reversed nested Miller compensation (RNMC) scheme. Moreover, the presence of two left-half-plane zeros in the amplifier's frequency response enhances the stability and hence improves the settling behavior of the amplifier. The circuit level simulation results of the proposed amplifier with a 0.18µm standard CMOS process achieve 20MHz unity gain bandwidth and 59 degree phase margin, while driving 500 pF load from a single 1.5 V power supply.**

I. Introduction

Amplifiers are one of the most important components in the electronic systems. They increasingly demand low voltage power supply, high dc gain, wide frequency bandwidth, and wide output voltage swing capabilities. With supply voltage reduction dictated by the scaling down of device sizes in the modern CMOS technologies, the conventional single-stage cascode amplifiers are not capable to deliver both high dc gain and large output signal swing. On the other hand, multistage amplifiers can be used to achieve both high dc gain and output signal swing, but, at the expense of much more reduced signal bandwidth. Moreover, multi-stage amplifiers suffer from the closed-loop stability problem due to the presence of multiple frequency poles and zeros. Therefore, the frequency compensation is needed to design the stable three-stage amplifiers.

There are generally two different compensation schemes in the three-stage amplifiers: Nested Miller Compensation (NMC) and Reversed Nested Miller Compensation (RNMC) [1]-[5]. An RNMC amplifier usually has a higher bandwidth than the NMC one since in the RNMC amplifier the inner compensation capacitor does not load the amplifier's output. However, the RNMC scheme has the stability problem because of appearing a right half plane (RHP) zero in its frequency response. To alleviate this problem, many RNMC techniques have been reported which are basically canceling the RHP zero such as the RNMC amplifier with voltage buffer and nulling resistor [1], reversed active feedback frequency compensation (RAFFC) [2], RNMC with voltage buffer and resistor [3], RNMC techniques with current follower (CF) and voltage follower (VF) [4], [5].

In this paper, a novel frequency compensation technique called the dual-active capacitance in reversed nested Miller compensation (DACRNMC) is proposed for three-stage amplifiers. This scheme of compensation uses two active compensation capacitors and yields a higher amplifier bandwidth.

The paper is organized as follows. In Sect. II, the proposed DACRNMC amplifier is described. The circuit implementation of the proposed amplifier as well as its circuit level simulation results are presented in Sect. III. Finally, Sect. IV concludes the paper.

II. The Proposed Technique

In this paper, a new frequency compensation technique for three-stage amplifiers called the *dual-active capacitance in reversed nested Miller compensation* (DACRNMC) is proposed. Figure 1 shows the basic block diagram of this technique where g_{m1}, g_{m2}, and g_{m3} comprise the main three-stage amplifier. R_a is the output resistance of the ac path and R_b is the input resistance of the current buffer stage. C_{m2} is the ac coupling capacitor and C_{m1} is the Miller capacitor. g_{ma} acts as the AC boosting path of the second stage to increase the high frequency gain. Besides, the structure has a current buffer stage, g_{mb}, which creates a high speed feedback path and improves the amplifier's bandwidth.

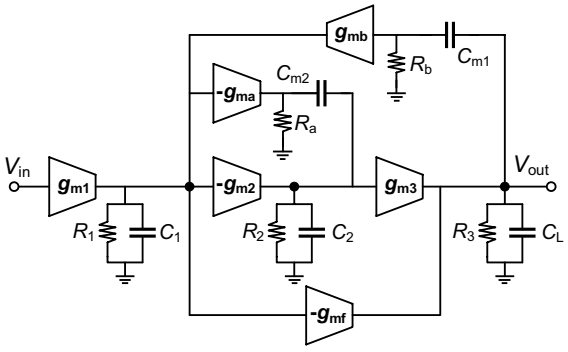

Fig. 1: Proposed dual-active capacitance compensation three-stage amplifier.

In the DACRNMC amplifier, there is not any passive compensation capacitor. Besides, in this technique an ac amplifier is added in parallel with the second stage making the second stage comprising of two signal paths. The first one

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is a dc path mainly for a high dc gain, and the other one is an ac path for boosting the high-frequency gain. Also, this topology has a current buffer that creates another high-speed feedback path. By using two high-speed paths, the non-dominant poles are shifted to the high frequencies [7]. Consequently, the gain-bandwidth product or the unity-gain frequency of the amplifier is improved.

Assuming that C_L, C_{m1} and C_{m2} >> C_i, and $g_{mi}R_i$, $g_{mf}R_L$ and $g_{mb}R_1$ >>1, and considering $g_{mb} \approx 2/R_b$, the small-signal transfer function of DACRNMC amplifier can readily be obtained as given in relation (1) where $A_0 = g_{m1}g_{m2}g_{m3}R_1R_2R_3$ is the dc gain and ω_{P1} is the real dominant pole of the amplifier.

Suppose that $A_2(f)$ represents the overall gain of the second stage. Then, by neglecting the effect of the parasitic capacitances, the AC gain of the second stage can be obtained as follows:

$$A_{ac} = \lim_{f \to \infty} \left| A_2(f) \right| = (g_{m2} + g_{ma})(R_a \parallel R_2) \tag{2}$$

The dominant pole is $\omega_{P1} \cong 3/2C_{m1}g_{m2}g_{m3}R_1R_2R_3$ and the gain-bandwidth (GBW) is given by

$$GBW = A_0.\omega_{P1} = \frac{3g_{m1}}{2C_{m1}} \tag{3}$$

By assuming $g_{m3} = g_{mf}$, the slew rate of the DACRNMC amplifier is improved because in this case the output stage can be implemented as a class AB fashion and the small-signal transfer function is simplified as follows:

$$A_v(s) = A_0 \frac{1 + s\left(\frac{2C_{m1}}{3g_{mb}} + \frac{A_{ac}+1}{g_{m2}}C_{m2}\right) + s^2\frac{2(A_{ac}+1)}{3g_{m2}g_{mb}}C_{m1}C_{m2}}{\left(1+\frac{s}{\omega_{P1}}\right)\left[1 + s\frac{A_{ac}+1}{g_{m2}}C_{m2} + s^2\frac{C_{m2}C_LC_1}{g_{m2}g_{m3}C_{m1}}\right]} \tag{4}$$

From (4), the non-dominant poles and zeros are obtained as:

$$\omega_{Z1} = -\frac{3g_{mb}}{2C_{m1}} \tag{5}$$

$$\omega_{Z2} = -\frac{g_{m2}}{(A_{ac}+1)C_{m2}} \tag{6}$$

$$\omega_{P2,3} = -\frac{(A_{ac}+1)g_{m3}C_{m1}}{2C_1C_L}\left(1 \pm j\sqrt{1 - \frac{4g_{m2}C_1C_L}{g_{m3}C_{m1}C_{m2}(A_{ac}+1)^2}}\right) \tag{7}$$

As is seen, the proposed three-stage amplifier has one real dominant pole, two complex non-dominant poles, and two left half plane zeros. Unlike the conventional AC boosting technique, in the DACRNMC amplifier all of the zeros are located at the left half plane resulting in improved phase margin and, hence, the unity gain bandwidth.

The AC boosting gain A_{ac} plays a critical role in the amplifier's design since by increasing A_{ac}, the non-dominant poles are shifted to high frequency so that enhancing the phase margin.

By using a third-order Butterworth response in order to arrange the non-dominant poles of the DACRNMC amplifier similar to that described in [9], the value of compensation capacitances, C_{m1} and C_{m2}, are given by

$$C_{m1} = 2\sqrt{\frac{3g_{m1}C_LC_1}{2g_{m3}(1+A_{ac})}} \tag{8}$$

$$C_{m2} = g_{m2}\sqrt{\frac{2C_LC_1}{3g_{m1}g_{m3}(1+A_{ac})^3}} \tag{9}$$

As is seen from (8) and (9), for a given transconductance of the main gain stages and load capacitance, the value of compensation capacitors, C_{m1} and C_{m2}, are decreased if A_{ac} is increased. Therefore, by increasing the AC boosting gain, the total die area of the amplifier can be decreased.

Since in the small signal relation of amplifier given in (1) the order of the numerator is less than that of the denominator, the stability is determined by the denominator. Thus, by applying the Routh-Hurwitz stability criterion as described in [2] on the characteristic equation (1), the stability condition is obtained as follows:

$$GBW < \frac{g_{m3}(1+A_{ac})}{C_LC_1}C_{m1} \tag{10}$$

By replacing C_{m1} from relation (8) into (10), the stability condition of the DACRNMC amplifier is also given by:

$$GBW < 2\sqrt{\frac{3g_{m1}g_{m3}(1+A_{ac})}{2C_LC_1}} \tag{11}$$

According to (11), for a given load capacitance, C_L, the GBW can be increased if the transconductance of the first and third stages, g_{m1} and g_{m3}, or the AC boosting parameter, A_{ac}, is increased. Since increasing g_{m1} or g_{m3} results in a higher power dissipation, the latter option should be preferred. Thus, A_{ac} is an important parameter in boosting the GBW, decreasing the die area, and moving the non-dominant poles to the high frequency.

$$A_v(s) = A_0 \frac{1 + s\left(\frac{2C_{m1}}{3g_{mb}} + \frac{(g_{m2}+g_{ma})(R_a \parallel R_2)g_{m3}+g_{mf}}{g_{m2}g_{m3}}C_{m2}\right) + s^2\frac{(g_{m2}+g_{ma})(R_a \parallel R_2)g_{m3}+g_{mf}}{3g_{m2}g_{m3}g_{mb}}2C_{m1}C_{m2}}{\left(1+\frac{s}{\omega_{P1}}\right)\left[1 + s\frac{(g_{m2}+g_{ma})(R_a \parallel R_2)g_{m3}+g_{mf}}{g_{m2}g_{m3}}C_{m2} + s^2\frac{C_{m2}C_LC_1}{g_{m2}g_{m3}C_{m1}}\right]} \tag{1}$$

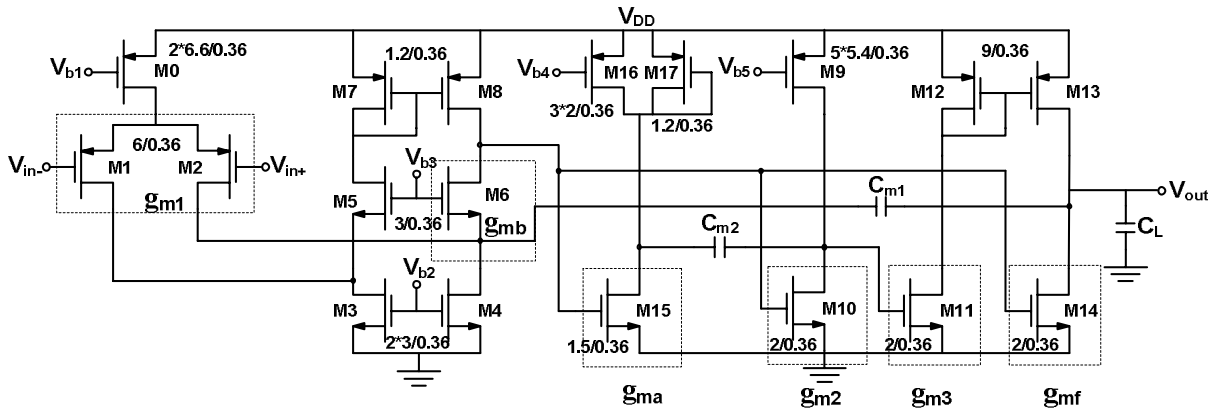

Fig.2: Circuit implementation of a three-stage DACRNMC amplifier.

III. Simulation Results

To prove the effectiveness of the proposed compensation technique, HSPICE simulations are carried out using a 0.18-µm BSIM3v3 level 49 CMOS technology. The amplifier was designed to achieve a dc gain of about 100dB and a phase margin of 60° with a capacitive load of 500 pF and a 1.5-V power supply.

The circuit implementation of the three-stage DACRNMC amplifier is shown in Fig. 2. The first gain stage is realized by transistors M0–M8 with a pMOS input differential pair which is made up of a folded cascode amplifier. The second inverting stage is built of a common source amplifier with an active load, M9-M10. The last non-inverting stage is realized by transistors M11-M14. Moreover, the g_{mb} compensation stage is simply realized by the transistor M6 of the folded cascode input stage amplifier, whereas M15-M17 acts as the AC boosting stage. For the AC boosting stage, the transistor M17 is used to determine the dc common mode voltage at the drain of M15. Finally, the feedforward transconductance stage, g_{mf}, is realized by M14.

The value of designed circuit parameters of the proposed amplifier is shown on the circuit schematic in Fig 2. By using (2), the value of A_{ac} is set at about 10, and according to (8), the Miller capacitance C_{m1} can be 1.15 pF. From (9), we get the Miller capacitance C_{m2} of 0.15pF. To achieve the targeted gain-bandwidth product, we set g_{m1}=97µA/V. Then, we set g_{mb}=205µA/V, g_{ma}=250µA/V, g_{m2}=345µA/V and g_{m3}=g_{mf}=352 µA/V.

Figure 3 shows the simulated open-loop frequency response of the proposed amplifier. The large signal and small signal transient responses of the amplifier in a unity-gain negative feedback configuration are shown in Figs. 4 and 5, respectively. In the large signal transient simulation an input step of 400-mV was applied whereas in the small signal transient simulation the amplitude of the input signal was 40-mV. The resulting dc gain, unity gain-bandwidth and phase margin are equal to 98.5dB, 20.4MHz and 59°, respectively. The total power current consumption is 190µA. Table I summarizes the simulation results of the proposed three stage amplifier.

Two figures of merit, $IFOM_S = GBW \times C_L / I_{dd}$ and $IFOM_L = SR \times C_L / I_{dd}$, have been proposed to characterize and compare the small signal (GBW) and the large signal (slew rate) behaviors of different amplifiers [7], respectively. By using these formulas, the higher IFOM shows the better performance of the amplifier. We shall use these performance metrics to compare our proposed amplifier with the recently reported ones.

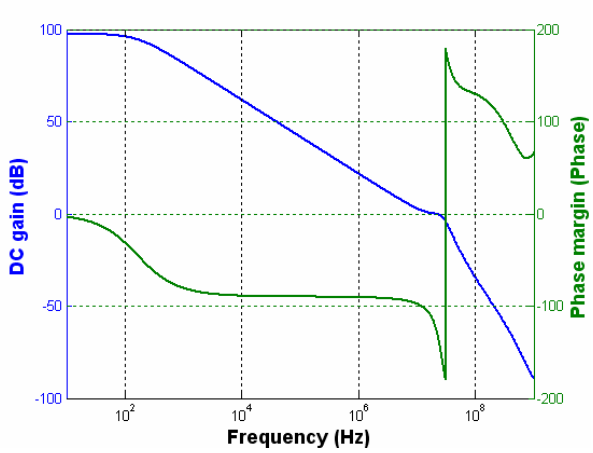

Fig. 3: Simulated open-loop frequency response of the amplifier.

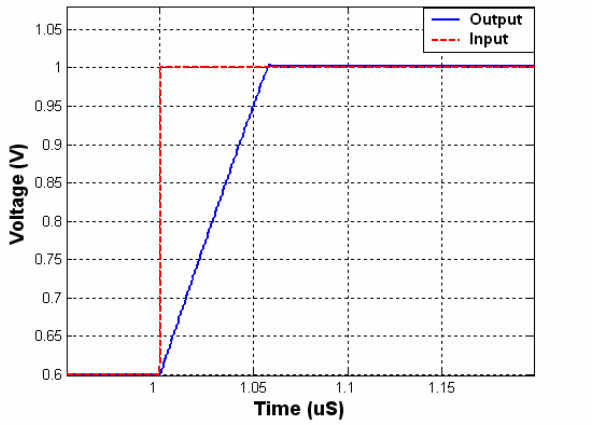

Fig. 4: Simulated transient response of the amplifier.

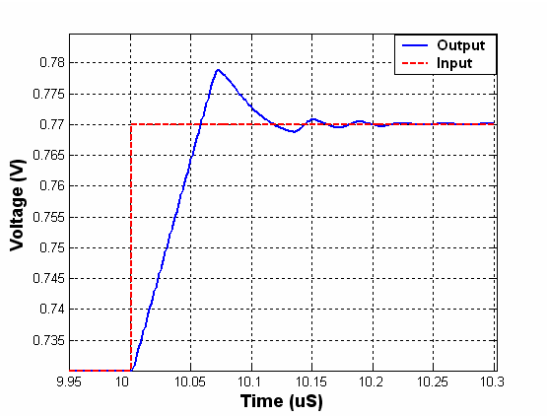

Fig. 5: Small-signal input-output characteristic of the amplifier.

TABLE I
PERFORMANCE SUMMARY OF SIMULATED AMPLIFIER

Parameter	Value
Gain (dB)	98.5
GBW (MHz)	20.4
Phase Margin (degree)	59
Power (µW)	284
Total Current (mA)	0.19
T_S (µs) +/–	0.57/0.46
SR (V/µs) +/–	0.72/1.05
SR (V/µs) (average)	0.885
$IFOM_S$ (MHz×pF/mA)	53684
$IFOM_L$ (V/µs×pF)/mA	2329
C_{m1} (pF)	1.15
C_{m2} (pF)	0.15
V_{DD} (V)	1.5
C_L (pF)	500
Technology	BSIM3v3 Level 49 0.18-µm CMOS

In Table II, the performance of several recently published three-stage amplifiers including the proposed one in this paper have been summarized. As is seen, the proposed DACRNMC amplifier outperforms the other previously proposed techniques and achieves the highest bandwidth.

IV. CONCLUSIONS

In this paper, a new compensation technique called DACRNMC for three stage amplifiers was presented. It was shown that a larger bandwidth compared to the other reported topologies can be obtained without using any passive compensation capacitor. Furthermore, by employing the active compensation capacitors, the die area of the circuit, which is mainly occupied by the compensation capacitors, is significantly reduced. The proposed compensation technique achieves the largest $IFOM_S$ compared to the other previously reported compensation topologies.

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TABLE II: COMPARISON OF DIFFERENT MULTISTAGE AMPLIFIERS

	C_L (pF)	V_{DD} (V)	I_{TOT} (mA)	Power (µW)	GBW (MHz)	SR (V/µs)	Capacitor (pF)	$IFOM_S$ (MHz×pF)/mA	$IFOM_L$ (V/µs×pF)/mA	Technology µm-CMOS
RNMCVBNR [1]	15	3	0.48	1.44	19.46	13.8	C_{m1}=3 C_{m2}=0.7	608	430	-
AFFC [6]	120	2	0.2	0.4	4.5	1.49	C_{m1}=5.4 C_{m2}=4	2700	894	0.8 µm
ACBCF [7]	500	2	0.162	0.324	1.9	1.0	C_{m1}=10 C_{m2}=3	5864	3086	0.35 µm
SMFFC [8]	120	2	0.21	0.42	9	3.4	C_m=4	5143	1943	0.5 µm
PFC [9]	130	1.5	0.19	0.275	2.7	1.0	C_{m1}=15 C_{m2}=3	1915	709	0.35 µm
DLPC [10]	120	1.5	0.22	0.33	7.0	3.3	C_{m1}=4.8 C_{m2}=2.5	3818	1800	0.6 µm
DACRNMC	**500**	**1.5**	**019**	**0.284**	**20.4**	**0.885**	**C_{m1}=1.15 C_{m2}=0.15**	**53684**	**2329**	**0.18 µm**