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A Novel Frequency Compensation Technique in Three Stage Amplifiers with Active Feedback

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Abstract: *This paper presents a dual-active capacitance in reversed nested Miller compensation (DACRNMC) technique for low-voltage and large capacitive load amplifiers. The frequency bandwidth of the DACRNMC amplifier is improved due to the usage of active compensation capacitors. The amplifier's die area is reduced compared to the existing techniques in reversed nested Miller compensation (RNMC) scheme. The architecture also generates two left half plane zeros to increase the phase margin. The simulation results with a 0.18µm standard CMOS process achieve 17.4MHz unity gain bandwidth and 64 degree phase margin for proposed DACRNMC amplifier, while driving 500 pF load from a single 1.5 V power supply.*

Keywords: CMOS multistage amplifiers, nested Miller compensation, and active capacitive feedback.

1. Introduction

Nowadays, with the scaling down of device sizes and supply voltages reduction in sub-micron CMOS technologies, multistage amplifiers are widely used in the analog and mixed signal circuits because conventional cascode topologies are not suitable for low voltage operation due to less voltage swings and output impedance. In contrast, multistage amplifiers have additional frequency poles and zeros resulting in inherently instability and reduced signal bandwidth if any frequency compensation technique is not employed.

There are generally two different compensation schemes in the three-stage amplifiers: Nested Miller Compensation (NMC) and Reversed Nested Miller Compensation (RNMC) [1]-[5]. An RNMC amplifier usually has a higher bandwidth than the NMC one since in the RNMC amplifier the inner compensation capacitor does not load the amplifier's output. However, the RNMC scheme has the stability problem because of appearing a right half plane (RHP) zero in its frequency response. To alleviate this problem, many RNMC techniques have been reported which are basically cancelling the RHP zero such as the RNMC amplifier with voltage buffer and nulling resistor [1], reversed active feedback frequency compensation (RAFFC) [2], RNMC with voltage buffer and resistor [3], RNMC techniques with current follower (CF) and voltage follower (VF) [4], [5].

In this paper, a novel frequency compensation technique called the dual-active capacitance in reversed nested Miller compensation (DACRNMC) is proposed for three-stage amplifiers. This scheme of compensation uses two active compensation capacitors and yields a higher amplifier bandwidth.

The paper is organized as follows. In Sect. 2, the proposed DACRNMC amplifier is described. The circuit implementation of the proposed amplifier as well as its circuit level simulation results are presented in Sect. 3. A comparison of

the proposed amplifier with published compensation techniques is given in Sect. 4 Finally, Sect. 5 concludes the paper.

2. The proposed technique

In this paper, a new frequency compensation technique for three-stage amplifiers called the *dual-active capacitance in reversed nested Miller compensation* (DACRNMC) is proposed. Figure 1 shows the basic block diagram of this technique where g_{m1}, g_{m2}, and g_{m3} comprise the main three-stage amplifier. R_a is the output resistance of the ac path and R_b is the input resistance of the current buffer stage. C_{m2} is the ac coupling capacitor and C_{m1} is the Miller capacitor. g_{ma} acts as the AC boosting path of the second stage to increase the high frequency gain. Besides, the structure has a current buffer stage, g_{mb}, which creates a high speed feedback path and improves the amplifier's bandwidth.

In the DACRNMC amplifier, there is not any passive compensation capacitor. Besides, in this technique an ac amplifier is added in parallel with the second stage making the second stage comprising of two signal paths. The first one is a dc path mainly for a high dc gain, and the other one is an ac path for boosting the high-frequency gain. Also, this topology has a current buffer that creates another high-speed feedback path. By using two high-speed paths, the non-dominant poles are shifted to the high frequencies [7]. Consequently, the gain-bandwidth product or the unity-gain frequency of the amplifier is improved.

Assuming that C_L, C_{m1} and C_{m2} >> C_i, and $g_{mi}R_i$, $g_{mf}R_L$ and $g_{mb}R_1$ >>1, and by considering $g_{mb} = 1/R_b$, the small-signal transfer function of DACRNMC amplifier can readily be obtained as given in relation (1) where $A_0 = g_{m1}g_{m2}g_{m3}R_1R_2R_3$ is the dc gain and ω_{P1} is the real dominant pole of the amplifier.

Suppose that $A_2(f)$ represents the overall gain of the second stage. Then, by neglecting the effect of

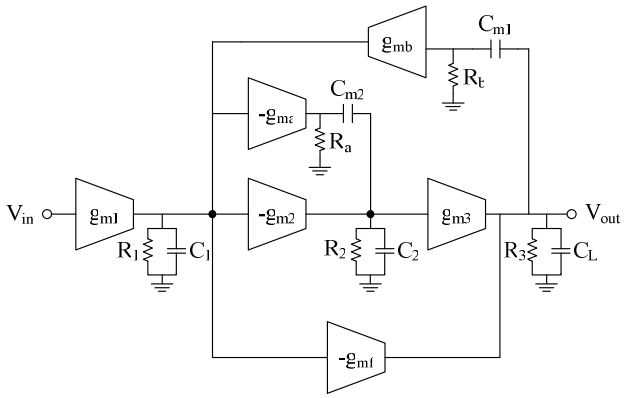

Fig. 1: Proposed dual-active capacitance compensation three-stage amplifier.

the parasitic capacitances, the AC gain of the second stage can be obtained as follows:

$$A_{ac} = \lim_{f \to \infty} |A_2(f)| = (g_{m2} + g_{ma})(R_a \parallel R_2) \qquad (2)$$

The dominant pole is $\omega_{P1} \cong 1/C_{m1}g_{m2}g_{m3}R_1R_2R_3$ and the gain-bandwidth (GBW) is given by

$$GBW = A_0.\omega_{P1} = \frac{g_{m1}}{C_{m1}} \qquad (3)$$

By assuming $g_{m3} = g_{mf}$, the slew rate of the DACRNMC amplifier is improved because in this case the output stage can be implemented as a class AB fashion and the small-signal transfer function is simplified as follows

$$A_v(s) = A_0 \frac{1 + s\left(\frac{C_{m1}}{g_{mb}} + \frac{A_{ac}+1}{g_{m2}}C_{m2}\right) + s^2\frac{A_{ac}+1}{g_{m2}g_{mb}}C_{m1}C_{m2}}{\left(1+\frac{s}{\omega_{P1}}\right)\left[1 + s\frac{A_{ac}+1}{g_{m2}}C_{m2} + s^2\frac{C_{m2}C_LC_1}{g_{m2}g_{m3}C_{m1}}\right]} \qquad (4)$$

From (4), the non-dominant poles and zeros are obtained as:

$$\omega_{Z1} = -\frac{g_{mb}}{C_{m1}} \qquad (5)$$

$$\omega_{Z2} = -\frac{g_{m2}}{(A_{ac}+1)C_{m2}} \qquad (6)$$

$$\omega_{P2,3} = -\frac{A_{ac}+1}{2g_{m2}}C_{m2} \pm j\sqrt{\left(\frac{A_{ac}+1}{2g_{m2}}C_{m2}\right)^2 - \frac{C_{m2}C_LC_1}{g_{m2}g_{m3}C_{m1}}} \qquad (7)$$

$$A_v(s) = A_0 \frac{1 + s\left(\frac{C_{m1}}{g_{mb}} + \frac{(g_{m2}+g_{ma})(R_a \parallel R_2)g_{m3} + g_{mf}}{g_{m2}g_{m3}}C_{m2}\right) + s^2\frac{(g_{m2}+g_{ma})(R_a \parallel R_2)g_{m3} + g_{mf}}{g_{m2}g_{m3}g_{mb}}C_{m1}C_{m2}}{\left(1+\frac{s}{\omega_{P1}}\right)\left[1 + s\frac{(g_{m2}+g_{ma})(R_a \parallel R_2)g_{m3} + g_{mf}}{g_{m2}g_{m3}}C_{m2} + s^2\frac{C_{m2}C_LC_1}{g_{m2}g_{m3}C_{m1}}\right]} \qquad (1)$$

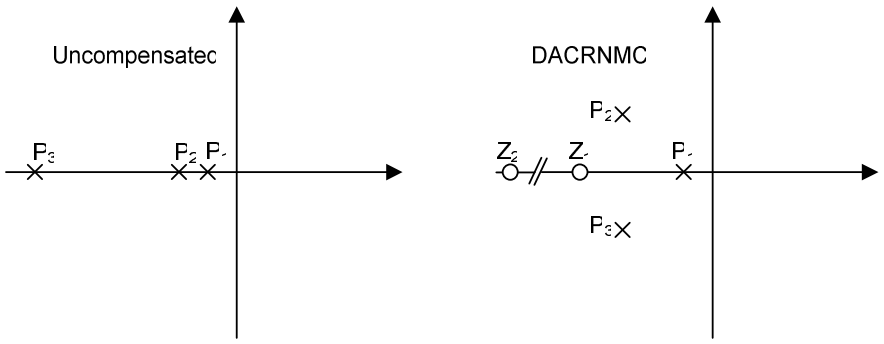

Fig.2 Pole-zero diagrams of Uncompensated and DACRNMC compensated amplifiers.

As is seen, the proposed three-stage amplifier has one real dominant pole, two complex non-dominant poles, and two left half plane zeros. All of the zeros in the DACRNMC amplifier are located at the left half plane resulting in improved phase margin and, hence, the unity gain bandwidth. For illustration, the pole-zero diagrams of uncompensated and DACRNMC amplifiers are shown in Fig. 2.

The AC boosting gain A_{ac} plays a critical role in the amplifier's design since by increasing A_{ac}, the non-dominant poles are shifted to high frequency so that enhancing the phase margin.

By using a third-order Butterworth response in order to arrange the non-dominant poles of the DACRNMC amplifier similar to that described in [9], the value of compensation capacitances, C_{m1} and C_{m2}, are given by

$$C_{m1} = 2\sqrt{\frac{g_{m1}C_L C_1}{g_{m3}(1+A_{ac})}} \tag{8}$$

$$C_{m2} = g_{m2}\sqrt{\frac{C_L C_1}{g_{m1}g_{m3}(1+A_{ac})^3}} \tag{9}$$

As is seen from (8) and (9), for a given transconductance of the main gain stages and load capacitance, the value of compensation capacitors, C_{m1} and C_{m2}, are decreased if A_{ac} is increased. Therefore, by increasing the AC boosting gain, the total die area of the amplifier can be decreased.

Since in the small signal relation of amplifier given in (1) the order of the numerator is less than that of the denominator, the stability is determined by the denominator. Thus, by applying the Routh-Hurwitz stability criterion as described in [2] on the characteristic equation (1), the stability condition is obtained as follows:

$$GBW < \frac{g_{m3}(1+A_{ac})}{C_L C_1} C_{m1} \tag{10}$$

By replacing C_{m1} from relation (8) into (10), the stability condition of the DACRNMC amplifier is also given by:

$$GBW < 2\sqrt{\frac{g_{m1}g_{m3}(1+A_{ac})}{C_L C_1}} \tag{11}$$

According to (11), for a given load capacitance, C_L, the GBW can be increased if the transconductance of the first and third stages, g_{m1} and g_{m3}, or the AC boosting parameter, A_{ac}, is increased. Since increasing g_{m1} or g_{m3} results in a higher power dissipation, the latter option should be preferred. Thus, A_{ac} is an important parameter in boosting the GBW, decreasing the die area, and moving the non-dominant poles to the high frequency.

3. Design Considerations and Simulation Results

To prove the effectiveness of the proposed compensation technique, HSPICE simulations are carried out using a 0.18-µm BSIM3v3 level 49 CMOS technology. The amplifier was designed to achieve a dc gain of about 100dB and a phase margin of 60° with a capacitive load of 500 pF and a 1.5-V power supply.

A judicious distribution of gain among the three stages is the most important consideration in the design of these amplifiers. For high gain amplifiers (>100 dB) the gain is distributed such that *Av1>Av3>Av2*. The gain of the first stage is maximized, with the second stage having very small gain and the final stage having a moderate gain. This results in the second and third pole of the amplifier to be located at higher frequencies due to the high output conductance of the second and third stages. In order to achieve this, the first

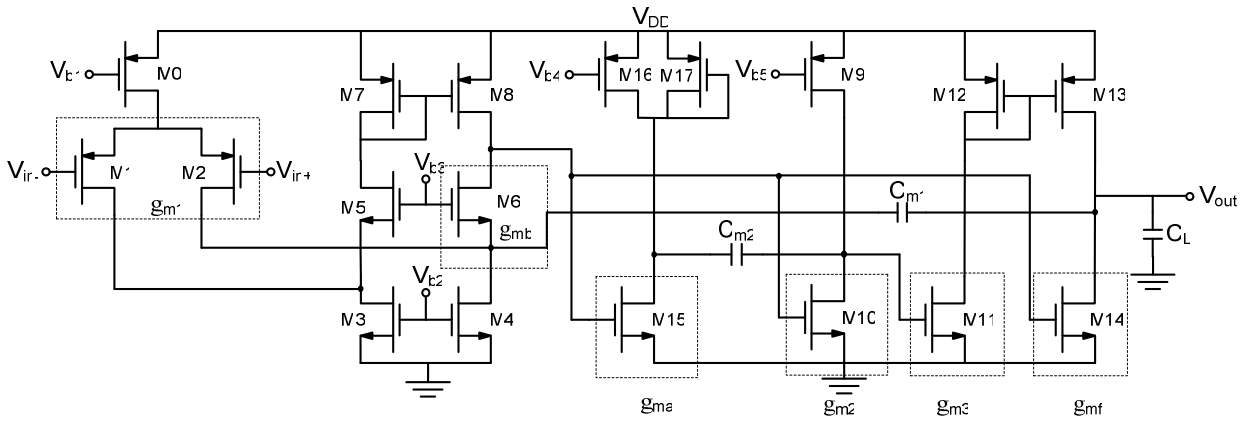

Fig.3: Circuit implementation of a three-stage.

DACRNMC amplifier stage uses a folded cascode topology to enhance the output impedance. For example a 100dB gain from three stages can be distributed as 50dB, 15 dB and 35 dB for first, second and third stage respectively.

The circuit implementation of the three-stage DACRNMC amplifier is shown in Fig. 3. The first gain stage is realized by transistors M0–M8 with a pMOS input differential pair which is made up of a folded cascode amplifier. The second inverting stage is built of a common source amplifier with an active load, M9-M10. The last non-inverting stage is realized by transistors M11-M14. Moreover, the g_{mb} compensation stage is simply realized by the transistor M6 of the folded cascode input stage amplifier, whereas M15-M17 acts as the AC boosting stage. For the AC boosting stage, the transistor M17 is used to determine the dc common mode voltage at the drain of M15. Finally, the feedforward transconductance stage, g_{mf}, is realized by M14.

Table 1
Circuit Parameters

Parameter	Value
M0	2×(6.6/0.36)
M1,M2	6/ 0.36
M3,M4	2×(3/ 0.36)
M5,M6	3/ 0.36
M7,M8	1.2/0.36
M9	5×(5.4/0.36)
M10	2/ 0.36
M11,M14	2/ 0.36
M12,M13	9/ 0.36
M15	2 / 0.36
M16	3×(5.1/ 0.36)
M17	2×(5/ 0.36)

The value of designed circuit parameters of the proposed amplifier is shown in Table 1. By using (2), the value of A_{ac} is set at about 85, and according to (8), the Miller capacitance C_{m1} can be 1.2 pF. From (9), we get the Miller capacitance C_{m2} of 0.2pF. To achieve the targeted gain-bandwidth product, we set g_{m1}=97µA/V. Then, we set g_{mb}=205µA/V, g_{ma}=354µA/V, g_{m2}=345µA/V and g_{m3}=g_{mf}=352 µA/V.

Figure 4 shows the simulated open-loop frequency response of the proposed amplifier. The large signal and small signal transient responses of the amplifier in a unity-gain negative feedback configuration are shown in Figs. 5 and 6, respectively. In the large signal transient simulation an input step of 400-mV was applied whereas in the small signal transient simulation the amplitude of the input signal was 40-mV. The resulting dc gain, unity gain-bandwidth and phase margin are equal to 98dB, 17.4MHz and 64°, respectively. The total power current consumption is 200µA. Table 2 summarizes the simulation results of the proposed three stage amplifier.

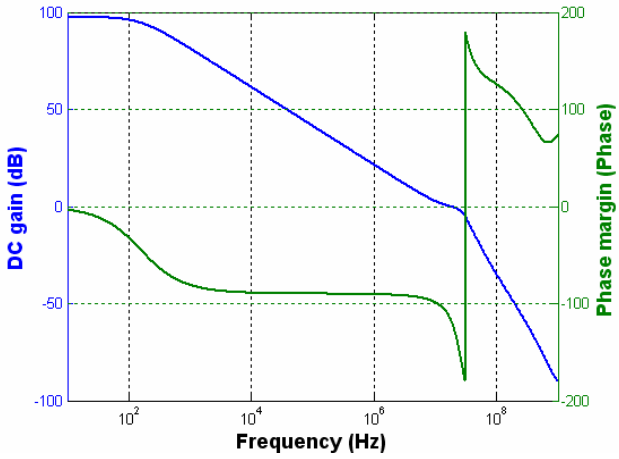

Fig. 4: Simulated open-loop frequency response of the amplifier.

4. Performance Comparison

It is difficult to make accurate evaluations on different amplifiers that are implemented in different technologies with different operating points. However, to provide a clearer picture of the improvement by proposed topology, a comparison of some published compensation topologies with the prepared topology in this paper is shown in Table 3. To evaluate different amplifiers two figures of merit were proposed to characterize small-signal (GBW) and large-signal (slew rate) performances of the amplifier and are given by [11], [12]

$$FOM_S = \frac{GBW \times C_L}{\text{Power}} \tag{12}$$

$$FOM_L = \frac{SR \times C_L}{\text{Power}} \tag{13}$$

By using these formulas, the value of higher FOM shows the better performance of the amplifier. However, when the supply voltages are different to use these formulas for the evaluation is relatively rough. Since the GBW and the SR are directly related to quiescent currents flowing in the relevant transistors. In order to a correct comparison, forming two new formulas, given by [7], [13]

$$IFOM_S = \frac{GBW \times C_L}{I_{dd}} \tag{14}$$

$$IFOM_L = \frac{SR \times C_L}{I_{dd}} \tag{15}$$

Obviously, Measured results shows that the proposed amplifiers have significantly outperformed all the other referenced amplifiers.

5. Conclusions

In this paper, a new compensation technique called DACRNMC for three stage amplifiers was presented. It was shown that a larger bandwidth compared to the other reported topologies can be obtained without using any passive compensation capacitor. Furthermore, by employing the active compensation capacitors, the die area of the circuit, which is mainly occupied by the compensation capacitors, is significantly reduced. The proposed compensation technique achieves the largest FOM_S and $IFOM_S$ compared to the other previously reported compensation topologies.

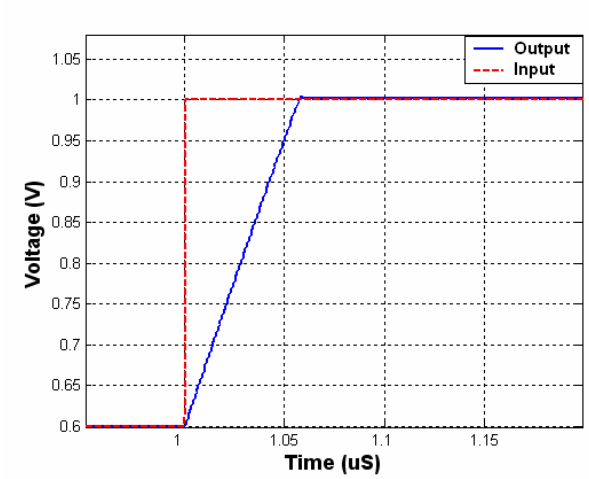

Fig. 5: Simulated transient response of the amplifier.

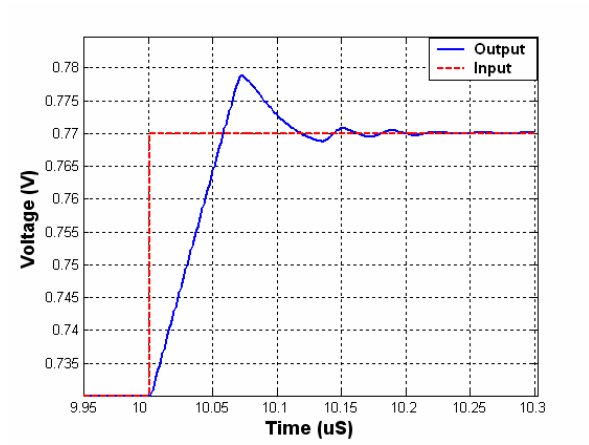

Fig. 6: Small-signal input-output characteristic of the amplifier.

Table 2
Performance Summary of Simulated Amplifier

Parameter	Value
Gain (dB)	98
GBW (MHz)	17.4
Phase Margin (degree)	64
Power (μW)	300
Total Current (mA)	0.2
T_S (μs) +/–	0.6/0.5
SR (V/μs) +/–	0.7/0.95
SR (V/μs) (average)	0.825
C_{m1} (pF)	1.2
C_{m2} (pF)	0.2
V_{DD} (V)	1.5
C_L (pF)	500
Technology	BSIM3v3 Level 49 0.18-μm CMOS

Table 3
Comparison of Different Multistage Amplifiers

	C_L (pF)	V_{DD} (V)	I_{TOT} (mA)	Power (µW)	GBW (MHz)	SR (V/µs)	Capacitor (pF)	FOM_S (MHz×pF/mW)	FOM_L (V/µs×pF)/mW	$IFOM_S$ (MHz×pF)/mA	$IFOM_L$ (V/µs×pF)/mA	Technology µm-CMOS
RNMCVBNR [1]	15	3	0.48	1.44	19.46	13.8	C_{m1}=3 C_{m2}=0.7	209	149	608	430	-
AFFC [6]	120	2	0.2	0.4	4.5	1.49	C_{m1}=5.4 C_{m2}=4	1350	447	2700	894	0.8 µm
ACBCF [7]	500	2	0.162	0.324	1.9	1.0	C_{m1}=10 C_{m2}=3	2932	1543	5864	3086	0.35 µm
SMFFC [8]	120	2	0.21	0.42	9	3.4	C_m=4	2571	971	5143	1943	0.5 µm
PFC [9]	130	1.5	0.19	0.275	2.7	1.0	C_{m1}=15 C_{m2}=3	1276	473	1915	709	0.35 µm
DLPC [10]	120	1.5	0.22	0.33	7.0	3.3	C_{m1}=4.8 C_{m2}=2.5	2545	1200	3818	1800	0.6 µm
DACRNMC	**500**	**1.5**	**0.2**	**0.3**	**17.4**	**0.825**	**C_{m1}=1.2 C_{m2}=0.2**	**29000**	**1375**	**43500**	**2062**	**0.18 µm**

References

[1] K. -P. Ho, C. -F. Chan, C. -S. Choy, and K. -P. Pun, "Reversed nested Miller compensation with voltage buffer and nulling resistor," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1735-1738, Oct. 2003.

[2] A. D. Grasso, G. Palumbo, and S. Pennisi, "Active Reversed Nested Miller Compensation for Three-Stage Amplifiers," *Proc. ISCAS'06*, vol. 1, pp. 911-914, May 2006.

[3] A. D. Grasso, D. Marano, G. Palumbo, and S. Pennisi, "Improved reversed nested Miller frequency compensation technique with voltage buffer and resistor," *IEEE Trans. Circuits and Systems-II*, vol. 54, no. 5, May 2007.

[4] R. Mita, G. Palumbo, and S. Pennisi, "Reversed nested Miller compensation with current follower," *Proc. ISCAS*, pp. 308-311, May 2001.

[5] G. Cataldo, R. Mita, G. Palumbo, and S. Pennisi, "Reversed nested Miller compensation with voltage follower," *Proc. ISCAS*, pp. 827-830, May 2002.

[6] H. Lee and P. K. T. Mok, "Active-feedback frequency compensation technique for low power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 511–520, March. 2003.

[7] X. Peng and W. M. Sansen, "AC boosting compensation scheme for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, Vol. 39, pp. 2074-2077, Nov. 2004.

[8] X. Fan, C. Mishra, E. Sanchez-Sinencio, "Single Miller Capacitor Frequency Compensation Technique for Low power Multistage Amplifiers," *IEEE J. Solid-State Circuits*, Vol. 38, pp. 1735-1738, Oct. 2003.

[9] J. Ramos, X. Peng, M. Steyaert, and W. Sansen, "Three stage amplifier frequency compensation," in *Proc. European Solid-state Circuits Conf.* Lisbon, Portugal, Sept. 2003, pp. 365–368.

[10] H. Lee, K. N. Leung, and P. K. T. Mok, "A dual-path bandwidth extension amplifier topology with dual-loop parallel compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1739–1744, Oct. 2003.

[11] H. T. Ng, R. M. Ziazadeh, and D. J. Allstot, "A multistage amplifier technique with embedded frequency compensation," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 339–347, Mar. 1999.

[12] K. N. Leung, P. K. T. Mok, W. H. Ki, and J. K. O. Sin, "Three-stage large capacitive load amplifier with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits, vol 35*, pp. 221–230, Feb.2000.

[13] X. Peng, W. Sansen, "Transconductance with Capacitances Feedback Compensation for Multistage Amplifiers," *IEEE J. Solid-State Circuits*, Vol. 40, No. 7, pp. 1515-1520, July 2005.