A Reconfigurable Sigma-Delta Modulator for Multi-Standard Wireless Applications

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Abstract: This paper describes the design and implementation of a low power reconfigurable sigma-delta modulator for multi-standard wireless applications in a 90-nm CMOS technology. Both architectural and circuital reconfigurations are used to adapt the performance of the modulator to five different communication standards. The feasibility of the proposed solution is shown using the system-level simulations as well as device-level simulations of the modulator. HSPICE simulation results reveal that the proposed modulator achieves 73/ 75/ 82/ 86/ 91 dB peak SNDR within the five standards of Wi-Fi/ WiMAX/ WCDMA/ Bluetooth/ GSM with the bandwidth of 11MHz/ 10MHz/ 1.92MHz/ 0.5MHz/ 200kHz respectively under power consumption of 37/ 37/ 12/ 5/ 5 mW in 1V supply.

1. INTRODUCTION

Growth of wireless communication standards combined with the limited success of previous generations of cellular systems forced the development of multi-standard terminals requiring reconfigurable building blocks to fulfill the requirements of different standards. One of the most challenging building blocks in a multi-standard receiver is the analog-to-digital converter (ADC), which requires a wide range of sampling rate and dynamic range (DR) to digitize the input signals of different bandwidths.

In this paper, a multi-standard ADC for a typical five modes of a zero-IF receiver is introduced. The receiver should be reconfigured to low-IF in the GSM standard. Table I shows the parameters associated with our targeted standards including Wi-Fi, WiMAX, WCDMA, Bluetooth and GSM. Vast variations in bandwidth and resolution make the design of such a reconfigurable low power solution very challenging. In a multi-standard ADC not only both the power consumption and chip area should be optimized for different operation modes, but also globally robustness against circuit non-idealities and modulator reconfiguration capability should be increased. It means in a multimode ADC, a single circuit is designed efficiently which can adapt to different sets of specifications required for each operation mode. Switched-capacitor (SC) sigma-delta modulators (SDMs) are good candidates for this purpose [1].

2. MULTI-STANDARD MODULATOR

Sigma-delta modulators fall into two main categories. First are the single loop modulators, which benefit from the relaxed circuit elements, but suffer from stability problems in high order modulators which are inevitable in wideband input signals. Second are the multistage noise-shaping modulators (MASH) which are well known for their stability. These solutions suffer from the existing leakage effects, due to mismatching, which degrades the modulator resolution. To reduce this problem in MASH modulators highly accurate analog circuits are required to be matched with the digital filters used at the end if each stage. Recently, a new multi-loop modulator called SMASH architecture was presented [2] which benefits from the stability of simple multi-loop modulators, while the circuit requirements are relaxed like single stage architectures. To implement a multi-standard ADC capable of dealing with five different performance requirements shown in Table 1 a flexible low power SMASH solution is proposed.

The proposed reconfigurable modulator is illustrated in Fig. 1 which is able to process the signals from five distinguishable standards while the sampling frequency changes between only two different values 200MHz and 62.5MHz. The modulator is reconfigured to three architectural modes, each mode satisfying the requirements of one or two operation standards.

In the proposed SMASH modulator, the second stage has a unity STF to ideally eliminate the first stage quantization error and an inter-stage gain of 4 is used to further reduce the second stage quantization noise. It should be noticed that the gain used at the end of the first integrator in the second stage is changed to 1 in WCDMA standard. Table 2 illustrates the specifications of targeted ADC using MATLAB/SIMULINK simulations.

As discussed in [2], the relaxed analog blocks are the main property of SMASH topology compared with MASH architecture. Here the requirements of the operational transconductance amplifiers (OTAs) in different operation modes are shown in Table 3 using MATLAB behavioral simulations [3].

Table 1: Targeted ADC specifications.

Receiver Architecture	Wireless Standard	Signal Bandwidth	ENOB
Zero-IF	IEEE802.11/Wi-Fi	12.5 MHz	11 bits
Zero-IF	IEEE802.16/WiMAX	10 MHz	11 bits
Zero-IF	WCDMA	1.92 MHz	12 bits
Zero-IF	Bluetooth	0.5 MHz	12 bits
Low-IF	GSM	0.2 MHz	14 bits

Table 2: The proposed ADC specifications.

Operation Mode	Input-Signal Bandwidth	Topology	Fs (MHz)	OSR	DR (dB)
Mode I	11 MHz 10 MHz	SMASH 2-2	200 200	8 10	90 92
Mode II	1.92 MHz	SMASH 2-1	62.5	16	94
Mode III	0.5 MHz 0.2 MHz	Second order single-stage	62.5 62.5	64 128	94 108

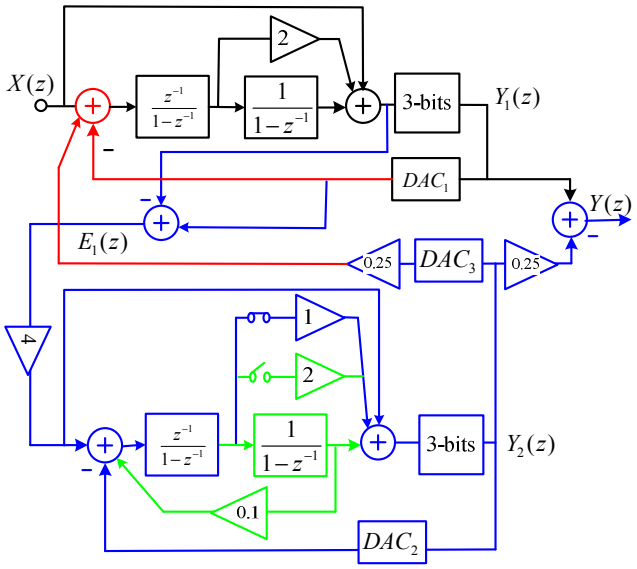

Figure 1: Proposed multi-standard modulator.

Table 3: The required specifications for the first OTA.

Operation Mode	DC-gain (dB)	GBW (MHz)	SR (V/μS)
Mode I	30	500	200
Mode II	30	250	150
Mode III	35	250	150

3. TRANSISTOR LEVEL IMPLEMENTATION

The proposed modulator is implemented using a 90 nm CMOS technology with 1V supply voltage. The circuit implementation of the digital adder in the first stage of the SMASH architecture represented in [2] has some problems. On one hand its delay will decrease the modulator speed and on the other hand using a digital adder with a digital coefficient will need a high resolution digital to analog converter (DAC) in the first loop. To solve these problems, this adder is implemented in the analog form on the first integrator as shown in Fig. 1.

Figure 2 shows the first integrator of the simulated modulator. Its transfer function is given by:

$$V_{o1}(z) = \frac{C_{S1}}{C_{I1}} \frac{1}{1-z^{-1}} \left(z^{-1} V_{in} - V_{DAC1} + \frac{1}{4} V_{DAC2} \right) \qquad (1)$$

which shows delaying and non-delaying integrating combined with adding operation on three signals of V_{in}, V_{DAC1} and V_{DAC2}. Here, dashed lines show the paths which will be eliminated in the third operation mode used for Bluetooth and GSM standards.

According to moderate DC-gain and high gain bandwidth of the amplifiers as shown in Table 3, a pMOS input pair folded-cascode OTA is chosen to be used in the integrators and the second stage active adder. To optimize the modulator area, the same OTAs are used for different standards while their bias circuit is changed from one standard to the other to optimize the power dissipation too. So the modulator contains only six OTAs which are used with three different bias circuits in different standards. Hence the modulator chip area is in the range of a single standard modulator while the power dissipation is also optimized for different operation standards.

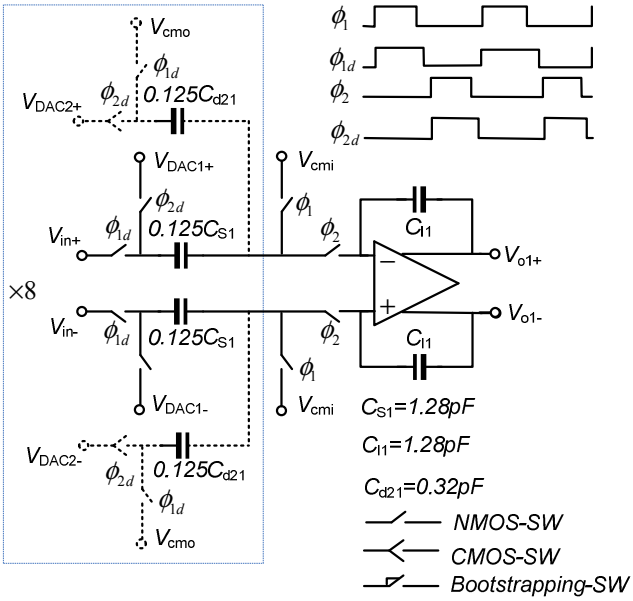

Figure 2: The first integrator circuit in the proposed modulator.

In the modulator architecture different types of MOS switches are used to optimally fulfill the required specifications. As shown in Fig. 2, the bootstrapping technique [4] is used in the input switches of the block to achieve the required linearity and the wide swing input signal makes no problem for the modulator. To further decrease the modulator power consumption, adding node before the first quantizer is realized passively, using a two stage preamplifier combined with input offset storage technique to decrease the effect of comparator offset error in this quantizer.

4. SIMULATION RESULTS

In this section, the simulation results of the reconfigurable multi-standard modulator implemented in a 90nm CMOS technology regarding the thermal noise of the switches and also OTAs are discussed. To evaluate the modulator noise floor in different communication standards, different sinusoidal input signals were applied to the modulator. Figure 3 shows the noise floor for the five operation standards.

Since the maximum value of SNDR is a good metric for the modulator resolution, dynamic range for each standard is simulated using HSPICE simulation results for different values of input signal amplitude as shown in Fig. 4.

The modulator simulation results in three different corner cases are summarized in Table 4. To compare this work with the other multi-standard sigma-delta modulators the following figure of merit (FoM) is used:

$$FoM = \left(2^{ENOB} \times f_s\right) / P \qquad (2)$$

where *ENOB* shows the effective number of bits in the modulator and P and f_s refer to the power consumption and ADC Nyquist rate, respectively. Table 5 compares this work with some of the present multi-standard and state-of-the-art sigma-delta modulators.

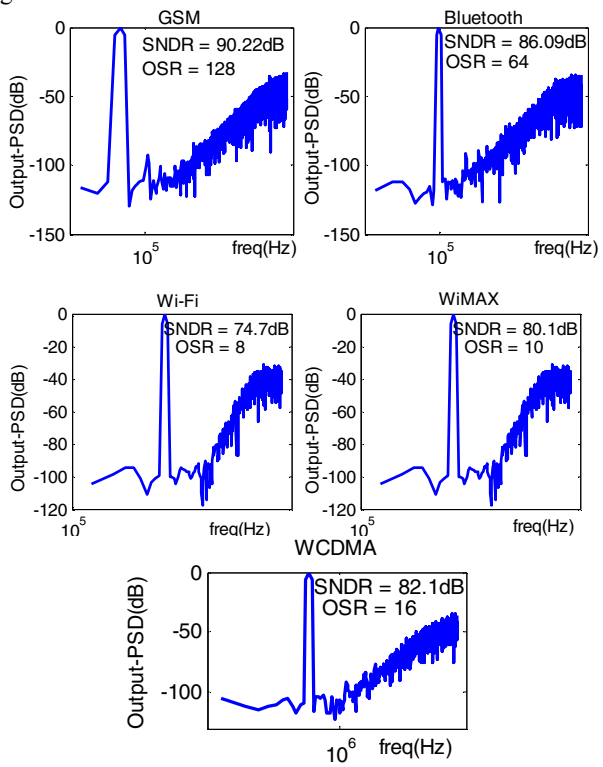

Figure 3: Power spectral density of the modulator output for different operation standards.

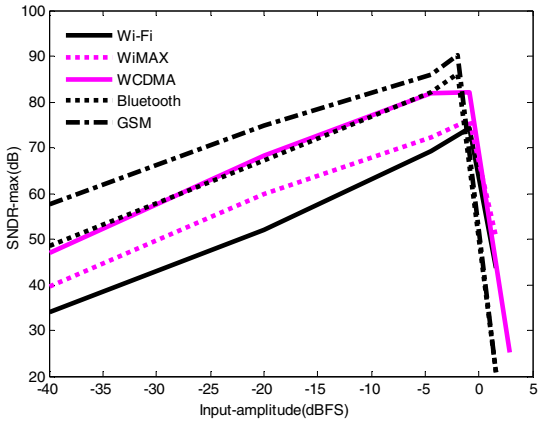

Figure 4: Dynamic Range of the modulator for different operation standards.

5. CONCLUSIONS

A reconfigurable sigma-delta modulator has been proposed in a 90-nm CMOS with 1V supply voltage. The modulator architecture and circuits are reconfigured to fulfill the required specifications of Wi-Fi/ WiMAX/ WCDMA/ Bluetooth/ GSM standards regarding the optimal chip area and power consumption issues. The reconfigurable modulator performance has been strictly verified according to the SNDR versus input signal amplitude for different operation standards.

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Table 4: Simulated multi-standard modulator performance summary.

BW (MHz)	F_s (MHz)	Topology	OSR	$SNDR_{max}$ (dB)			Total Power Consumption (mW)	FoM (Conversion/pJ)
				Slow	Normal	Fast		
12.5	200	SMASH 2-2	8	68	73	75	37	**2.4**
10	200	SMASH 2-2	10	71	75	77	37	**2.5**
1.92	62.5	SMASH 2-1	16	78	82	83	12	**3.3**
0.5	62.5	Second order Single-stage	64	85	86	87	5	**3.28**
0.2	62.5	Second order Single-stage	128	87	91	92	5	**2.3**

Table 5: The proposed multi-standard modulator compared with some previously reported designs.

Work	Technology	V_{DD} (V)	Topology	*BW* (MHz)	$SNDR_{max}$ (dB)	f_s (MHz)	Power (mW)	*FoM* (Conversion/pJ)
This Work*	**90 nm**	**1**	**SMASH 2-2**	**12.5**	**73.6**	**200**	**37**	**2.4**
[5]*	0.18 um	1.8	MASH 2-2-0	10	59	160	49	**0.3**
[6]	0.18 um	1.8	MASH 2-2	10	57	160	42	**0.27**
[7]	0.13 um	1.2	MASH 2-2	10	61.7	240	20.5	**0.8**
[8]	0.18 um	1.8	Second order Single-stage	10	42.9	1000	14.5	**0.14**
[9]	0.18 um	1.8	Fourth order Single-stage	12.5	52	400	18	**0.22**
[10]	0.18 um	1.8	MASH 2-2-2	8	48.5	64	27.5	**0.06**
[11]	0.13 um	1.2	Fourth order Single-stage	15	63.7	300	70	**0.49**
[12]	0.18 um	1.8	Fourth order Single-stage	5	19	26	2.34	**0.03**
This Work*	**90 nm**	**1**	**SMASH 2-1**	**1.92**	**82**	**62.5**	**12**	**3.3**
[10]	0.18 um	1.8	MASH 2-2-2	2	78.9	64	27.5	**0.52**
[13]	0.35 um	2.7	Fourth order Single-stage	1.92	72	153.6	14	**0.44**
[14]	0.18 um	1.8	Third order Single-stage	1	56.8	100	22.2	**0.02**
[15]	90 nm	1.2	MASH 2-1 Multirate	2	65	80 320	6.83	**0.42**
[16]	0.24 um	2.5	Fifth order Single-stage	2	62	128	8	**0.5**
[17]	90 nm	1.2	MASH 2-1 Multirate	2	58	80	6.43	**0.4**
[12]	0.18 um	1.8	Fourth order Single-stage	2.5	24	26	2.34	**0.02**
This Work*	**90 nm**	**1**	**Second order Single-stage**	**0.5**	**86**	**62.5**	**5**	**3.28**
[10]	0.18 um	1.8	MASH 2-2	0.5	76	64	6.3	**0.81**
[15]	90 nm	1.2	Second order Single-stage	0.5	76	90	3.7	**0.69**
[18]	0.5 um	2.5	MASH 2-1-1	0.5	95	64	90	**0.5**
[19]	0.18 um	2.7	Second order Single-stage	0.5	77	23	30	**0.19**
[17]	90 nm	1.2	Second order Single-stage	0.5	76	90	3.7	**1.38**
[12]	0.18 um	1.8	Fourth order Single-stage	0.768	32	26	2.34	**0.02**
[20]*	0.13 um	1.2	MASH 2-1-1	1	70	20	7.3	**0.35**
This Work*	**90 nm**	**1**	**Second order Single-stage**	**0.2**	**91**	**62.5**	**5**	**2.3**
[20]*	0.18 um	1.8	Second order Single-stage	0.2	86	25.6	7.6	**0.43**
[21]	0.13 um	1.2	Second order Single-stage	0.2	70	26	1.4	**0.66**
[13]	0.35 um	2.7	Fourth order Single-stage	0.135	83.5	26	7	**0.23**
[15]	90 nm	1.2	Second order Single-stage	0.1	77	50	3.43	**0.17**
[19]	0.25 um	2.5	Third order Single-stage	0.1	72	104	11.5	**0.05**
[17]	90 nm	1.2	Second order Single-stage	0.1	77	50	3.43	**0.3**
[22]	0.35 um	3.3	Third order Single-stage	0.1	57	6.4	13.1	**0.0008**

*Simulated Results