A MATLAB Toolbox Synthesizing Reconfigurable Delta-Sigma Modulators for Multi-Standard Wireless Applications

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***Abstract*—This paper presents a high-level synthesis MATLAB toolbox for reconfigurable delta-sigma analog-to-digital converters used in multi-standard wireless communication terminals. The main algorithm synthesizing the reconfigurable delta-sigma modulators finds an optimal discrete time architecture which can be reconfigured for different considered communication standards and predicts the parameters of the modulator to achieve the required resolution for different operation modes. Estimating the requirements of analog blocks, combined with power consumption evaluation and extracting an area factor for different delta-sigma modulator architectures makes the proposed toolbox an advantageous alternative for reconfigurable delta-sigma modulator synthesis. As verification, the toolbox is used to verify some of the reconfigurable analog to digital converter (ADC) chips proposed and made for multi-standard wireless applications.**

***Index Terms*—low distortion topology, multi-standard receiver, operational transconductance amplifier, reconfigurable analog to digital converter**

I. INTRODUCTION

The limited success of previous generations of cellular systems and growth of wireless communication technologies forced the development of fourth generation (4G) [1] with multimode terminals requiring reconfigurable building blocks to fulfill the requirements of each standard. One of the most challenging building blocks of a multimode receiver is the Analog-to-Digital Converter (ADC), which requires a wide range of sampling rates and dynamic ranges (*DR*) to digitize the input signals of different standards covered in 4G radios. Switched-capacitor (SC) delta-sigma modulators (DSM) are good candidates for reconfigurable ADCs to be used in these multi-standard communication systems [2]. They can be easily programmed by adjusting some of their parameters, such as oversampling ratio (*OSR*), noise shaping order (*L*) or quantizer resolution (*b*), as can be seen in

$$DR = \frac{1.5\times(2L+1)(2^b-1)^2 OSR^{2L+1}}{\pi^2} \qquad (1)$$

In a reconfigurable DSM not only both power consumption and area occupation should be optimized for different operation modes, but also globally robustness against circuit non-idealities should be increased. It means in a multimode ADC, a single circuit is designed efficiently which can adapt to different sets of specifications required for each operation mode.

Most of previous works on synthesizing DSMs, such as [3], [4] and [5], represent algorithms which introduce a topology that is optimal for only one operation mode, although there are a few design approaches to select a good DSM for multimode applications but these algorithms mostly explore among either only single-stage topologies, such as [6] or only one known family of multi-stage noise shaping (MASH) architectures for example MASH 2-1^p, such as [2], while the Multi Mode Delta-Sigma toolbox (mmdelsig), presented in this paper is able to explore both single-loop and MASH structures to choose the final optimum architecture according to its power consumption and also area. It means you may receive the optimum architecture for example as MASH 2-2 for WiFi, MASH 2-0 for Bluetooth and second order single stage modulator for GSM with other parameters such as OSR, number of quantizer bits determined for each one. So, you can decide to have the optimal architecture exploring just single stage DSMs or just MASH architectures or both of them.

The paper is organized as follows. Section II describes the topologies explored by mmdelsig toolbox and section III introduces the algorithm used in this toolbox to find the optimum reconfigurable solution. Section IV shows mmdelsig toolbox results for several previously developed multimode DSMs. The conclusions are presented in section V.

II. MODULATOR TOPOLOGIES

A discrete time representation of a DSM with additive white noise modeling for quantization error is used as a simple linear modeling of this system. For wideband input signals, the oversampling ratio would be limited by the VLSI technology and power consumption problems so it is not increased unlimitedly. On the other hand, in low oversampling ratios quantization noise and also distortion effects caused by modulator non-ideal blocks play an important role in DR degradation, so it is necessary to have analog blocks with more severe requirements. To reduce this problem, low distortion topology with unitary signal transfer function (STF) is used for both single-stage and multi-stage modulators [7].

A. Single Stage Modulators Topology Evaluation

The two well-known topologies for single stage delta-sigma modulators are Cascode of Integrators with distributed FeedBacks (CIFB) and Cascode of Integrators with distributed FeedForwards (CIFF). There are two major differences between these topologies. Due to the FeedForward (FF) paths, the output swings of the integrators of the FF topology is much smaller than the FeedBack (FB) topology when the same integrator coefficients are used [6]. On the other hand, a fast amplifier is usually needed for the summation node before the quantizer of the FF topology but this power-hungry amplifier can be omitted using different solutions such as capacitive FF summation at the end of the last integrator. So as a total result FF topologies are more power efficient than FB topologies. Then we were focused on this topology to implement both single stage and multi stage

modulators knowing there are some optimal values for infinity norm of the noise transfer function (NTF) as explained in [6].

B. MASH Modulators Topology Evaluation

Mmdelsig sets the number of stages and the order of first stage for each operation mode equal to or less than the modulator selected for the most wideband mode. Hence less architectures are explored for the other standards.

III. PROPOSED TOOLBOX

As shown in Fig. 1, mmdelsig toolbox has some input parameters which must be inserted by its operator considering his favorite applications.

Here there are some system level input parameters and some circuit level parameters. At first, the user should insert the different signal bandwidths (*BW*s) and resolutions (*ENOB*s) considering his application. Then he will select if mmdelsig searches the requested specifications among just single-stage modulators, just MASH DSMs or both architectures (Select). Below, three main sections of the total algorithm used by mmdelsig to find the optimal reconfigurable modulator architecture are described.

Part A: Synthesizing the main modulator architecture

In the first step, suitable noise transfer functions (NTFs) are evaluated according to the specifications of the most wideband standard. Then, desired NTFs are mapped on feasible architectures based on select value to estimate the required specifications for analog building blocks in these architectures.

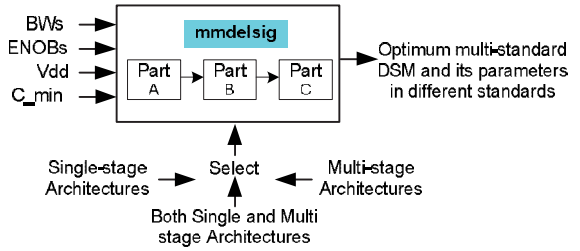

Figure 1. mmdelsig toolbox parameters.

In this step, the most important factors, i.e. DC gain, unity gain bandwidth and slew rate in operational transconductance amplifiers (OTAs) used in integrators, are evaluated which is described in next subsections. In the third step, power consumption and total capacitor value are estimated in possible modulator architectures to choose the best modulator. In multi-standard applications maximum sampling frequency is determined by the most wideband standard. On the other hand, as mentioned before, this sampling frequency is limited by VLSI technology parameters and so the required specifications for the most wideband input signal is obtained by noise shaping order, i.e number of integrators. Hence the most power hungry mode for a multi-standard modulator is when it is used for the most wideband standard. In this case, optimum topology for this mode is a low power consuming modulator architecture but with a total capacitor value as low as possible (as an area factor). Thus at the end of this part of algorithm, possible topologies for this mode are sorted regarding their power consumption and the architecture with least capacitor value is picked among the low power consuming architectures.

Part B: Reconfiguring for the other standards

In this part, the modulator topologies which can be configured on the modulator selected in previous part are considered for the other operation modes. These topologies are limited to those with number of stages equal to or less than the architecture selected for the most wideband standard. Now again, appropriate NTFs are evaluated for the next wideband standard and then analog circuits specifications and modulator power consumption and total capacitor value are estimated in this mode. Finally optimum modulator is selected like previous part.

Part C: Optimizing for the most narrowband standards

Now, an optimum solution for the most narrowband input standard should be evaluated. After appropriate NTFs are evaluated and then mapped on possible topologies for this standard, analog blocks specifications and the whole modulator power consumption and total capacitor value are estimated for all these possible NTFs. Since in multi-standard applications the most narrowband standard needs a high *DR* it is necessary to use large capacitors in this mode to decrease analog circuits and switches thermal noise. Hence the largest capacitors are used for the most narrowband standard and this total capacitor value is a good factor of the area occupation of the modulator. In this case, optimum topology for the most narrowband operation mode is a architecture with a small total capacitor whose power consumption is as low as possible. Therefore at the end of the last part of the algorithm, possible topologies for the most narrowband input standard are sorted regarding their total capacitor value and then the architecture with least power consumption is chosen among the modulators which have low area occupation

A. Noise Transfer Functions Evaluation

The total algorithm used by mmdelsig to evaluate possible NTFs for each input standard is shown in Fig. 2. In this algorithm different NTFs are evaluated starting from the minimum possible values for systematic parameters of modulator, i.e L=2, b=1 and OSR=2 using Delta-Sigma toolbox (delsig) introduced in [8]. The algorithm searches for all possible combinations of these parameters among just single-stage modulators or just MASHs or both topologies as explained before. Then the converter is tested if still reaches the target *DR*, after the circuit noise is added to the quantization noise of the modulator rejects solutions which offer much more *DR* than actually needed.

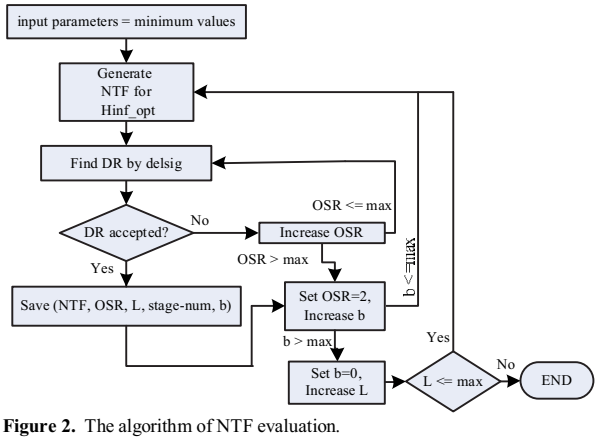

Figure 2. The algorithm of NTF evaluation.

B. Evaluating Capacitor Values

Since total capacitor value is a good factor demonstrating a modulator area occupation, in this section, all available capacitors for each qualified modulator topology are calculated.

The total thermal noise power in a DSM produced by switches and also the OTAs is shaped as,

$$P_{th} = \sum_{i=1}^{L} \frac{4kT\pi^{2(i-1)}}{(2i-1)C_{si}OSR^{2i-1}} \qquad (2)$$

Hence, all sampling capacitors can be evaluated and then integrating capacitors and also the other needed capacitors in the DAC paths and other places can be calculated knowing modulator coefficients and sampling capacitors [1]. The total capacitor value is sum of all available capacitors in the DSM.

C. Evaluating the Specifications of Analog Circuits

After extraction of suitable NTFs, they are mapped on possible single-stage and MASH topologies according to select value. Then required specifications i.e. DC-gain, unity gain bandwidth (*GBW*) and slew rate (*SR*) for different OTAs used in each modulator are estimated as developed in [9].

Here effect of non-idealities of OTAs on modulator performance is briefly reviewed.

DC-gain:

In a SC integrator, finite DC-gain (A_0) of the OTA causes a gain error equal to $A_0/(1+A_0)$ and a shift of NTF zeros from $z = 1$ to a point inside the unity circle. If the signal band is larger than the corner frequency then the noise power within the signal band is only minimally affected by finite DC-gain. In this case DC-gain is estimated for single-stage modulators [9]. In MASH modulators first OTA in each stage is the most critical OTA with DC-gain in the order of the whole modulator *DR* while the other integrators in each stage require less op-amp DC-gain compared to the first one, because of the shaping property.

Gain Band Width & Slew Rate:

GBW and *SR* are two other parameters which affect the modulator performance. Since the integration phase in a SC integrator only lasts $T_s/2$, the output does not reach its final value because of finite *GBW* and *SR* in the OTA and causes an error. To make this error negligible its maximum value must be very smaller than maximum acceptable error in the modulator [9]. Note that the total settling time ($\tau_s = \tau_{sL} + \tau_{sNL}$) must be less than $T_s/2$ in SC integrators (about $0.4T_s$) while $\tau_{sL} = \tau \ln(1/\varepsilon_{\max})$ and $\tau_{sNL} = (V_{final}/SR)$ so *GBW* and *SR* are estimated for each OTA regarding the shaping specifications of DSMs.

D. Power Consumption Estimation

In this step, the power dissipation for all qualified solutions is estimated considering discrete time DSM with SC circuits and class-A amplifiers. Generally, the most power consuming blocks in a DSM are the amplifiers used in SC integrators. These amplifiers must provide the needed DC-gain, *GBW* and *SR* determined for the modulator.

There are two important points about the architecture of OTAs in different DSMs. In some cases, especially the wideband operation modes since the sampling frequency is high, a high *GBW* and *SR* are required for the amplifiers. On the other hand, in MASH topologies high DC-gain is needed for the OTAs, to decrease the quantization noise leakage of the previous stages. Therefore a database consisting of six amplifiers commonly used in DSMs was proposed. These popular amplifiers, called simple two-stage, current mirror two-stage, single-stage folded cascode, two-stage folded cascode as the first stage and common-source as the second stage, single-stage telescopic cascode and two-stage telescopic cascode as the first stage and common-source as the second stage, are selected by toolbox according to the extracted requirements for each OTA. Then the power consumption of the OTA is estimated following the process illustrated in this section.

The power consumption estimation process is described only for folded cascode OTA. At first, the OTA architecture is selected according to the DC-gain requirements then the tail current in that architecture is estimated according to the *SR* and *GBW* requirements. Input transistors' overdrive voltage is then calculated more precisely by to find the current more accurately. If this current satisfies required specifications for the OTA it is saved otherwise it is increased to reach to the favorite value. Finally the power dissipation,

$$P_{opamp} = k_{op} V_{dd} I_{tail} \qquad (3)$$

in that OTA is calculated, where k_{op} is the power factor of the OTA listed in Table I for different OTAs.

TABLE I. POWER CONSUMPTION FACTOR FOR DIFFERENT OTA ARCHITECTURES

OTA architecture	Two-stage simple OTA	Two-stage current mirror OTA	Single-stage folded cascode OTA	Two-stage folded cascode OTA	Single-stage telescopic cascode OTA	Two-stage telescopic cascode OTA
k_{op}	3.5	3	2.5	5	1.5	3.5

IV. SIMULATION RESULTS AND VERIFICATION

The mmdelsig toolbox is used to verify some of the reconfigurable ADC chips proposed and made for multi-standard wireless applications. Table II shows state of art for synthesizing different reconfigurable ADCs. In this table figure of merit ($FoM = \frac{P_d}{2 \times DR \times BW}$) is calculated according to *ENOB*, *BW* and power consumption of each modulator for the most wideband standard. Then, mmdelsig toolbox is used to synthesize optimum architecture for these applications. The results also are summarized in Table II which shows that the proposed toolbox is an advantageous alternative for reconfigurable DSM synthesize.

V. CONCLUSIONS

A MATAB toolbox synthesizing a reconfigurable DSM for different wireless applications has been developed exploring both single-stage and multi stage delta-sigma modulators, for a wide range of over sampling ratio. The proposed toolbox evaluates the total capacitor value in different modulators and also the most critical limiting factors of analog building blocks to estimate the power consumption. Accurate modeling of analog building blocks combined with power consumption estimation and the total capacitor value makes this tool a good alternative for reconfigurable DSMs synthesis.

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TABLE II. STATE-OF-THE-ART MULTI-STANDARD A/D CONVERTERS PERFORMANCE SUMMARY (PROTOYPE)

	State of The Art							*mmdelsig results*				
Ref	***BWs (MHz)***	***ENOBs***	***OSR***	***Topology***	***Bit***	***Power (mw)***	***FOM (e-3)***	***ENOBs***	***OSR***	***Bit***	***Estimated power (mw)***	***Topology***
[10]	10 1.92 0.1	10.8 12.8 14.3	12 16 96	MASH(2-2)	(2,2)	20.5 7.4 2.9	0.55	12 13 15	12 14 34	(2,2)	25.4 8.7 2.9	MASH(2-2)
[11]	1.92 1.5 0.2	9.7 8.5 11.3	8 18 120	MASH(2-2)	(3,3) 3 3	11 5 5.8	3.45	10 8 12	8 16 44	(3,2) 3 3	9 6 3.4	MASH(2-2) Single2 Single2
[12]	3.84 0.2	8.7 12.3	24 192	Single3 Single2	1 1	13.5 11.5	4.25	9 12	22 64	2 2	26 4.8	Single3 Single2
[13]	1.92 0.1	11.3 13.3	10 196	MASH(2-1) Single2	(2,3) 1	4.3 2.4	0.445	11 13	12 54	(3,2) 3	4.3 1.9	MASH(2-1) Single2
[14]	2 0.1	12.8 14.3	16 160	MASH(2-2) Single2	(1,4) 1	17.8 8.3	0.6	13 15	14 140	(2,2) 2	15.6 6.2	MASH(2-2) Single2
[15]	4 2 0.2	10.75 8.8 14.1	16 16 128	MASH(2-1-1) MASH(2-1) Single2	(1,1,1) (1,1) 1	13.3 11.1 7.6	0.95	12 9 14	14 14 176	(1,1,1) (1,1) 1	21.3 10.9 6.8	MASH(2-1-1) MASH(2-1) Single2
[16]	2 0.2	8 12	12 65	Single2 Single2	3 3	2.9 2.4	2.85	8 11	16 32	3 3	3.6 1.9	Single2 Single2
[17]	10 1.92 0.27	11 12.8 15.3	16 64 512	MASH(2-1-1) MASH(2-1) Single2	(1,1,1) (1,1) 1	128 82 58	3.125	12 13 16	14 24 266	(1,1,1) (1,1) 1	146 65 51	MASH(2-1-1) MASH(2-1) Single2
[18]	10 2 0.2	8.7 12.5 15.5	8 16 160	Single3 Single3 Single2	4 4 4	39 23 18	4.7	8 12 15	8 18 90	4 4 3	22 18.8 13.8	Single3 Single3 Single2
[19]	2.5 0.1	8.8 12.3	16 32	Single3	1 1	4	1.8	8 12	20 40	2 2	6.5	Single3