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A Low-Power Inductor-Less Linear Wideband CMOS Balun-LNA Using Current Reuse And Linearity Techniques

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***Abstract*—This brief presents an inductor-less low-power balun-LNA employing negative feedback and post-distortion technique for the purpose of acquiring third-order non-linearity elimination without disturbing second-order intermodulation cancellation. The common gate (CG)-common source (CS) complementary push-pull topology, partially declines the common gate (CG) transistors thermal noise and the balun technique noise cancellation leads to total noise figure (NF) reduction. The post-distortion technique employs auxiliary cross-coupled transistors in weak-inversion region, which not only improves third-order linearity but also boosts voltage gain. The proposed balun-LNA structure designed in 65nm CMOS technology, reveals a noise figure (NF) of 3.25 dB, a S_{11} of less than -11 dB, and a S_{21} of 16.1 dB covers the -1 dB frequency range of 0.3-5 GHz. It achieves mean second-order intercept point (IIP2) and third-order intercept point (IIP3) of +27 dBm and +5 dBm, respectively. The circuit operates at a nominal supply voltage of 1.2 V with a bias current of 2.48 mA, which leads to low-power consumption.**

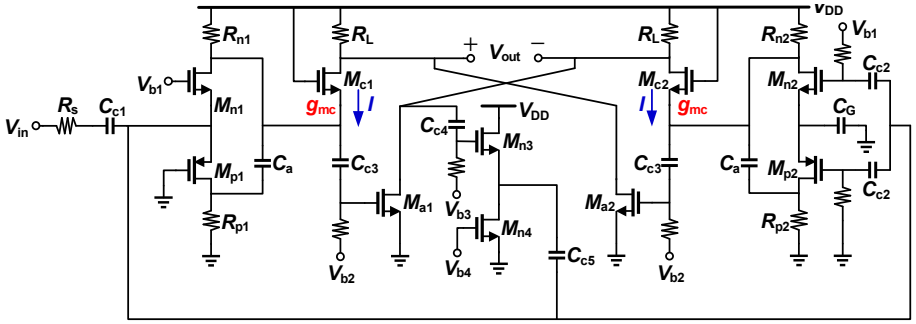
***Keywords*—CMOS balun-LNA, inductor-less, linearity, noise cancellation, post-distortion, IIP2, IIP3, low-power.**

I. Introduction

Low noise amplifier (LNA) role as the first active block in wireless receivers that improves signal to noise ratio (SNR) of the receivers which happens by noise cancellation techniques and simultaneously high amount of gain. The performance of LNAs evaluates by several factors and parameters compatible with the required applications. Some of these factors are sufficient impedance matching, a flat good amount of gain, high linearity, low noise figure (NF) over the entire bandwidth, and low gain and phase mismatch. Over the past decade, balun-LNAs received more attention since demanding differential outputs and provision of lower second-order distortion without using passive baluns that use a lot of area and have a loss.

Recently, linearity factor and noise mitigation techniques have been bold in circuit designers' eyes [1]. creating two different paths from the input to the output with the same gains weakens the noise of the input transistors to a good extent and at the same time increases the gain of the circuit [1, 4, 8, 10, 13]. Various linearization methods have attracted the attention of designers, and according to the improvement of the linearity type, each method can optimize the desired circuit structure. One of the linearization methods used is the derivative superposition technique, which by biasing the auxiliary transistors in the weak-inversion region, the third-order current coefficients of these transistors are similar to those of the main transistors, and IIP3 is significantly improved [1, 4, 3]. The only problem with this method is the degradation in input impedance matching. Another method used is the post-distortion method, which will once again enhance the linearity of the circuit by removing the third-order coefficients [1, 2, 7, 9, 3]. This method suffers from high power loss due to the bias of auxiliary transistors in the strong-inversion region. Symmetrical adoption of the output stage and load resistors is one of the punch lines that must be observed to maintain gain and phase mismatch [5, 6, 7, 11, 14, 17]. from this perspective, the use of balloon structure in designing low noise amplifier circuits shows itself more. utilization of passive balloons is not recommended due to their high cost and losses [15, 16, 18]. LNAs with an inherent balloon are the only choice for cost reduction and optimal design. The most common balloon structure is the mixture of CS and CG transistors at the input, which brings challenges. Matching the input impedance is highly dependent on the CG transistor, and satisfying this action will require choosing a lower transconductance of the CG transistor than the CS, which abolishes the symmetry of the circuit. One of the proposed solutions to prevent this phenomenon is auxiliary transistors in the role of current bleeding, which solves this problem by injecting additional current into the CS transistor, nevertheless causing an increase in power consumption [5, 7, 8]. One of the keys to facing this limitation is to use positive feedback, which adjusts the input impedance without shrinking the CG transistor and establishes symmetry in the circuit [12, 17].

This brief proposed a low-power inductor-less wideband balun-LNA with balanced loads and linearity techniques such as negative feedback and a mixture of derivative-superposition, and post-distortion that improves LNA's IIP3 by consuming negligible additional power. The complimentary CG-CS topology increases IIP2 and affords partial noise cancellation to provide a degree of freedom to design LNA for better linearity conditions. The future sections of the paper are organized as follows. Section II presents the structure of the proposed balun-LNA in detail. Section III provides the simulation results, and finally, the conclusion is given in Section IV.



Component Name	Value (M×F×W/L)
$M_{n1,2}$	1×25×1.2 μm /60 nm
$M_{p1,2}$	4×20×1.2 μm /60 nm
$M_{c1,2}$	1×20×1.2 μm /60 nm
$M_{a1,2}$	1×1×600 nm /60 nm
M_{n3} , M_{n4}	1×1×600 nm /60 nm

Component Name	Value
$R_{n1,2}$, $R_{p1,2}$, R_L (Ω)	2.25 k, 200, 200
C_{c1} , C_G , C_a , C_{c2} , C_{c3} , C_{c4} , C_{c5} (F)	20 p, 20 p, 10 p, 10 p, 5 p, 1 p, 1 p

Fig. 1. Proposed CMOS Balun-LNA.

II. Structure Of The Proposed Balun-LNA

The proposed Balun-LNA circuit illustrates in Fig. 1. The input stage of the LNA is made of the complimentary CG-CS structure, which in addition to removing the thermal noise of the M_{n1} and M_{p1} establishes the second-order linearity to a convenient extent. M_{n2} and M_{p2} are used to create the inherent balloon on the other side of the circuit, which, in addition to eliminating the noise of CG transistors, has the ability to eliminate phase and gain mismatch. In the following, M_{c1} and M_{c2} as cascode transistors are used to establish the symmetry of the circuit, whose bias is established by adjusting the resistance in their source. The total current of the cascode transistors and the bias resistor passes through the input transistors reused, which prevents current bleeding and significantly reduces power consumption. In the next step, to increase the linearity of the circuit, M_{a1} and M_{a2} as auxiliary transistors are used in the weak-inversion region in parallel with the cascode transistors. Due to the auxiliary transistors in the weak-inversion region, they pass a small amount of current and consume a small amount of power. CS transistors intensify the effects of third-order nonlinearity, therefore, to improve IIP3, negative feedback is considered for the transistors. utilizing such a technique, the attenuation loop of the third-order coefficients is formed and creates this degree of freedom that can eliminate third-order intermodulation. the input impedance matching circumstances, voltage gain calculation, noise figure analysis, and linearity of the proposed balun-LNA are represented in the following.

A. Input Impedance Matching

According to the structure of the circuit in Fig. 1, the input of LNA consists of complementary CG-CS, which generally CG transistors are responsible for matching the input impedance. According to these points, the following equation represents the matching of input impedance.

$$R_S = \frac{1}{g_{mn1} + g_{mp1}} \tag{1}$$

In the above relationship, R_S is the resistance seen from the source, g_{mn1} and g_{mp1} are the transconductance of CG transistors. It should be noted that to adjust the bandwidth of the circuit, capacitors C_G and C_{c1} play a key role in flattening the gain, NF, and S_{11}.

B. Voltage Gain

Without considering the drain-source resistance of the transistors and the effect of cross-coupled transistors, taking into account the negative feedback to establish the linearity of the CS transistors, the proposed LNA gain is obtained according to the following equation:

$$A_v = \frac{2(g_{mn1} + g_{mp1})g_{mc1}R_{n1}R_{p1}R_L}{[R_S(g_{mn1} + g_{mp1}) + 1][R_{n1}R_{p1}g_{mc1} + R_{n1} + R_{p1}]} \tag{2}$$

Due to symmetry, the half-circuit gain calculation depicted in (2), where g_{mn1} and g_{mp1} are transconductance of CG transistors, g_{mc1} transconductance of cascode transistors, R_{n1} and R_{p1} drain resistances of CG transistors, R_S source resistance, and R_L load resistance. By adding auxiliary transistors to increase the linearity, the overall gain of the circuit is increased by 1 dB according to (3), and in addition, it improves the phase mismatch.

$$A_v = \frac{2(g_{mn1} + g_{mp1})(g_{mc1} + g_{ma2})R_{n1}R_{p1}R_L}{[R_S(g_{mn1} + g_{mp1}) + 1][R_{n1}R_{p1}g_{mc1} + R_{n1} + R_{p1}]} \tag{3}$$

where g_{ma2} is the transconductance of the auxiliary transistor.

C. Noise Analysis

According to the operation of noise cancellation methods, if the amplification of the two noise paths leading to the output is the same, the noise of the desired elements can be eliminated. Considering the selection of the right transconductances for CG transistors to establish input impedance matching, the optimal dimensions of CS transistors are directly effective in eliminating the noise of CG transistors. Considering that the cascode transistors and the output resistors are designed in the same way due to establishing symmetry in the output, to create the same gain in the CS branch, it is necessary to adjust the resistors R_{p2} and R_{n2}. The noise figure (NF) of the balun-LNA authorizing input impedance matching using equation (1), is calculated with simplification, according to the following equation:

$$NF = 1 + \frac{\gamma}{2}\left[\frac{1 - R_S^2(g_{mn2} + g_{mp2})^2}{(1 + g_{mp1}R_S)}\right]^2 + \frac{2\gamma(g_{mn2} + g_{mp2})}{R_S^3} + \frac{4\gamma g_{mc1}}{R_S^3}\left[1 + \frac{R_{n1} + R_{p1}}{g_{mc1}R_{n1}R_{p1}}\right]^2 + \frac{4R_S(R_{n1} + R_{p1})}{R_{n1}R_{p1}g_{mc1}^2} + 4R_SR_L\left[1 + \frac{R_{n1} + R_{p1}}{g_{mc1}R_{n1}R_{p1}}\right]^2 \tag{4}$$

The second and third term of (4) stands for the thermal noise of M_{n1}, M_{p1}, M_{n2}, and M_{p2} respectively. The fourth term depicted the M_{c1} and M_{c2} thermal noise and the rest of the equation shows the thermal noise of the resistors.

As mentioned before, noise cancellation technique must implement on CS transistors. the condition to satisfy the criteria shows in (5) which improves NF by 2 dB.

$$1 - R_S(g_{mn2} + g_{mp2}) = 0 \tag{5}$$

D. Linearity Analysis

The linearization technique used in this article is a mixture of derivative-superposition and post-distortion. In the conventional derivative-superposition technique, the auxiliary transistors are located in the weak-inversion region and are parallel to the main transistors, which will have a significant effect in matching the input impedance, and also in the conventional post-distortion technique, the auxiliary transistors are parallel to the output cascode transistors, which are They will not directly affect the matching of the input impedance, but due to being in the strong inversion region, they consume high power. According to the above points, in the proposed technique, auxiliary transistors are used in parallel with cascode transistors in the weak inversion region, which will not only have no effect on input impedance matching, but their power consumption will be negligible. In addition, the negative feedback technique has been used to create a loop to eliminate the third-order coefficients of CS transistors in order to increase the linearity of CS transistors. The CS stage linearity of the balun-LNA calculated according to the following equations:

$$V_{in} - V_1 = R_S(g_{mn1} + g_{mp1})V_1 \tag{6}$$

$$I_{out-} = I_{mc2} - I_{ma1} \tag{7}$$

$$\begin{aligned} -I_{mc2} &= I_{mn2} + I_{mp2} \square (g_{mn2} + g_{mp2})V_1 \\ &+ (g'_{mn2} + g'_{mp2})V_1^2 + (g''_{mn2} + g''_{mp2})V_1^3 \end{aligned} \tag{8}$$

Equations (6) and (7) attains by Kirchhoff's voltage and current law, and putting Volterra series to use results relation (8) to accomplish fundamental, second-order, and third-order coefficients of output current an follows.

$$I_{out-,fund} = -\frac{(g_{mn2} + g_{mp2})(g_{mc2} + g_{ma1})R_{n2}R_{p2}}{2(g_{mc2}R_{n2}R_{p2} + R_{n2} + R_{p2})}V_{in} \tag{9}$$

$$\begin{aligned} I_{out-,2nd} &= -(g'_{mn2} + g'_{mp2})(g_{mc1}R_{n1}R_{p1} + R_{n1} + R_{p1})^2 \\ &\times \frac{g'_{ma1}[(g_{mn2} + g_{mp2})R_{n2}R_{p2}]^2}{4(g_{mc2}R_{n2}R_{p2} + R_{n2} + R_{p2})^2}V_{in}^2 \end{aligned} \tag{10}$$

$$\begin{aligned} I_{out-,3rd} &= -(g''_{mn2} + g''_{mp2})(g_{mc1}R_{n1}R_{p1} + R_{n1} + R_{p1})^3 \\ &\times \frac{g''_{ma1}[(g_{mn2} + g_{mp2})R_{n2}R_{p2}]^3}{8(g_{mc2}R_{n2}R_{p2} + R_{n2} + R_{p2})^3}V_{in}^3 \end{aligned} \tag{11}$$

The fundamental relation depicts voltage gain of the balun-LNA which gives in equation (9). From (10) and (11), the second and third non-linearity factors appear that leads to calculation of the non-linearity attenuation by reaching The following relations at the same time.

$$(g'_{mn2} + g'_{mp2})g_{mc1}^2 + g'_{ma1}(g_{mn2} + g_{mp2})^2 = 0 \tag{12}$$

$$(g''_{mn2} + g''_{mp2})g_{mc1}^3 + g''_{ma1}(g_{mn2} + g_{mp2})^3 = 0 \tag{13}$$

According to the relation (13), by biasing auxiliary transistors in weak-inversion region, g''_{ma1} will be positive while g''_{mn2} and g''_{mp2} are negative. As a result, the IIP3 improvement is achievable due to reducing third-order intermodulation terms.

As equation (9) shows, the fundamental relation stands for balun-LNA gain, and it shows that the auxiliary transistors increase the gain by 1 dB. According to the simulation results, which are presented in the next section, the proposed linearization techniques improve IIP3 of the proposed LNA by 7 dB with only 130 µA additional current consumption.

III. Simulation Results

The proposed balun-LNA circuit is designed for wideband applications at the operating frequency of 0.3-5 GHz. The aspect ratios of the LNA transistors are shown in Fig. 1. The circuit was designed in Spectre-RF using 65 nm RF-CMOS technology with a 1.2 V power supply and metal-insulator-metal (MIM) capacitors and poly resistors are used for the circuit structure. The circuit structure provides this capability to establish input impedance matching without the need for passive inductors. The main transistors of the circuit use the complementary CG-CS structure to provide local noise cancellation for the CG transistors in addition to creating second-order linearity. By choosing the optimal dimensions for the CG transistors, the input impedance matching, as well as suitable S_{11} less than -11 dB over the entire bandwidth is obtained shown in Fig. 2.

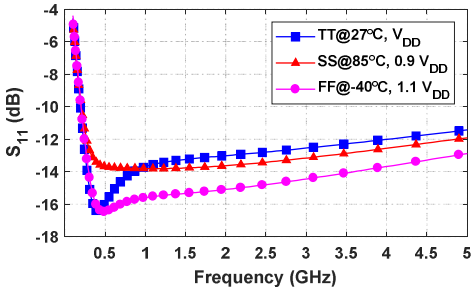


Fig. 2. Simulated S_{11} of the proposed LNA over -1dB gain bandwidth.

In addition to establishing an inherent balun, the path of CS transistors can eliminate the noise of CG transistors by 2 dB, and optimal NF is obtained by choosing their dimensions optimally shows in Fig. 3.

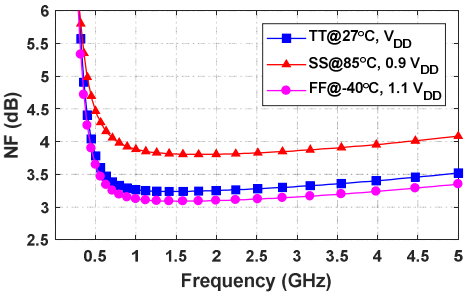


Fig. 3. Simulated NF of the proposed LNA over -1dB gain bandwidth.

The auxiliary transistors in the weak-inversion region are biased with the gate-source voltage to have little power consumption which improves IIP3 by 4 dB. in addition to weakening the third-order intermodulation, the negative feedback path is from the CS transistors to the input capacitor improves IIP3 by 3 dB, which has the task of establishing the third-order coefficient attenuation loop of the CS transistors, which have adopted small dimensions so that, in addition to the low power consumption, they do not disturb the matching of the input impedance. The IIP2 and IIP3 of the proposed LNA illustrate in Fig. 4 and Fig. 5 respectively at typical corner case. The overall gain of the balun-LNA shown in Fig.6. Wide-swing cascode constant-gm structure drives the LNA shown in Fig. 7.

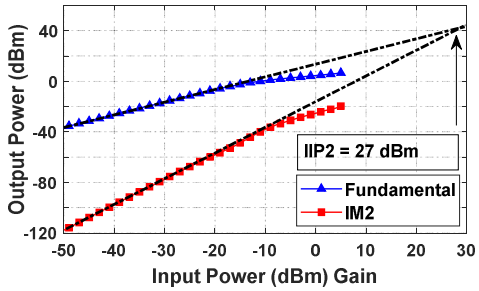


Fig. 4. Simulated IIP2 considering elements mismatches in typical corner.

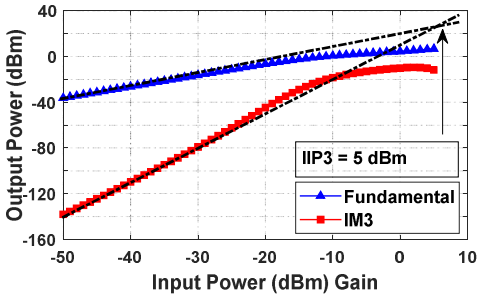


Fig. 5. Simulated IIP3 considering in typical corner.

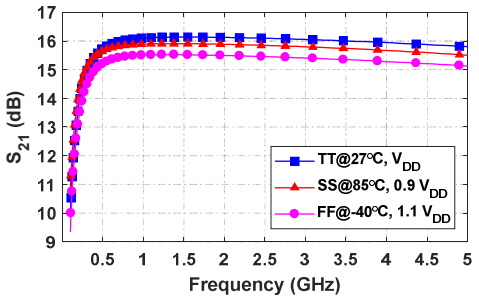


Fig. 6. Simulated S_{21} of the proposed LNA over -1dB gain bandwidth.

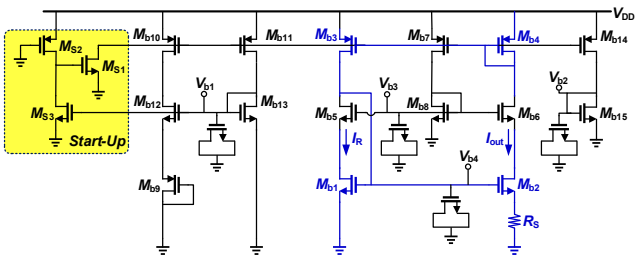


Fig. 7. Proposed constant-Gm bias circuit.

TABLE I: PVT SIMULATION RESULTS

Parameter	TT @ 27°C, V_{DD}	SS @ 85°C, 0.9 V_{DD}	FF @-40°C, 1.1V_{DD}
BW_{-3dB} (GHz)	0.15-10	0.16-9.5	0.14-12
S_{21} (dB)	16.2	15.8	15.5
NF_{min} (dB)	3.32	3.80	3.13
IIP3 (dBm)	+5	+2	+1
IIP2 (dBm)	28	24	30
Power (mW)	2.97	2.5	3.6

Table I summarized the simulation results of the proposed balun-LNA in PVT conditions and it shows the circuit is well designed against PVT variations. To test the stability of the circuit from the Rollet stability factor (K-factor) given in (14). Considering that, for stability of the circuit, K-factor should be greater than 1, and Δ smaller than 1 in the operating frequency of the circuit, the simulation of these parameters has been done up to the frequency of 20 GHz, which indicates the unconditional stability of the circuit shows in Fig. 8.

$$K = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{21}||S_{12}|} \qquad (14)$$

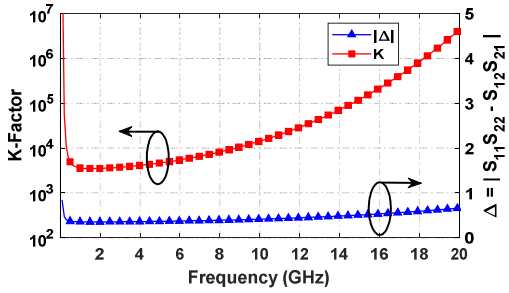


Fig. 8. Simulated the Rollet stability factor (K-factor) and Δ.

Fig. 9(a), Fig. 9(b) Illustrates the Monte Carlo simulation results of IIP3 before and after the linearization technique implementation with the main RF tone at 2 GHz and 10 MHz spacing. The figures indicate the proposed idea improves the IIP3 by the amount of 7 dB. The IIP3 versus the input signal frequency with 10 MHz spacing and also the Monte Carlo simulation results of IIP2 shows in Fig. 9(c) and Fig. 9(d) respectively.

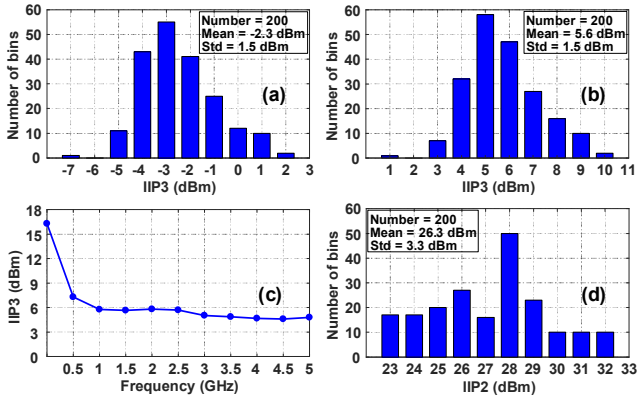


Fig. 9. IIP3 Monte Carlo simulation (a) before and (b) after using the linearity enhancement technique, (c) IIP3 versus the input signal frequency with 10 MHz spacing, (d) IIP2 Monte Carlo simulation results.

Table II represents a comparison between the proposed balun-LNA and some of recent wideband balun-LNAs. As it seems, the proposed structure reaches higher linearity with lower power consumption and yet low NF with extensive

TABLE II: PERFORMACE COMPARISON WITH SEVERAL PREVIOUS WIDEBAND CMOS BALUN-LNA

Reference	CMOS Process	BW (GHz)	S11 (dB)	S21 (dB)	NF (dB)	IIP3 (dBm)	IIP2 (dBm)	Power (mW)	V_{DD} (V)	FoM (dB)
Mejo'15 [2][b]	90 nm	2.4-10.4	<-11.2	9.5	3.5	+13.1	+42.8	14.8	1.2	18.99
TCAS-I'19 [5][#]	65 nm	0.05-1	<-10	24-30	2.3-3.3	-1.7	20	19.8	2.2	16.67
ICEE'20 [7][b]	65 nm	0.65-8.5	<-13	17	2.75-3.5	-1.358	-	7.4	1	16.43
AICSP'20 [8][#]	180 nm	0.1-6	<-10	15.5	3-4	+1.5	-	14	1.8	13.27
TCAS-I'20 [11][#]	65 nm	0.05-2.1	-	24-27.5	2.3-3	-2.2	+19.6	5.7	1	22.42
TCAS-I'21 [12][#]	180 nm	0.1-3.1	-	7.2	2.5-3.4	+17.8	-	23.9	1.8	17.08
TCAS-II'21 [13][#]	65 nm	0.7-2.2	-	21.9-26.8	2.9-3.8	+11.4	-	15.1	1	28.4
TMTT'22 [14][b]	180 nm	0.13-0.93	<-10	16.6-19.6	3.6-5	-8.5	+12	3	1.8	4.25
TCAS-I'22 [15][#]	130 nm	0.05-0.7	-	26.5	<4.25	-11.5	-	33.6	1.2	-3.93
TR'22 [16][#]	180 nm	0.065-0.84	<-10	12.5-15.5	3.2-5	+8.3	+43	6.4	1.8	14.29
TCAS-II'22 [17][b]	65 nm	0.47-3.3	<-10	19.45-22	2.57-3.5	+2.81	29.27	12.5	1.5	19.29
TCAS-II'23 [18][#]	22 nm	2.1-5.2	<-10	12.7-15.7	1.46-1.96	-	-	16	1	-
This Work*[b]	65 nm	0.3-5	<-11	15.4-16.1	3.25-3.7	+5	+28	2.97	1.2	22.89

*-1 dB gain bandwidth [b]Simulation Results [#]Measurement results

bandwidth. The following figure of merit (FoM) defines in [17] represents a better comparison which used in Table II.

$$FoM\,(dB) = 10 \times \log \frac{S_{21}(abs) \times IIP3(mW) \times BW(GHz)}{(F-1)(abs) \times P_{DC}(mW)} \quad (15)$$

In above equation S_{21} is the maximum magnitude of the power gain, BW is the bandwidth of the LNA, F is the magnitude of the minimum NF and P_{DC} is the LNA's power consumption.

IV. CONCLUSION

In this brief, new structure of a low-power balun-LNA employing linearity techniques introduced in 65 nm CMOS technology. The linearization technique not only improves IIP3, but also increase voltage gain with consuming negligible amount of power. Simulation results shows that the circuit operates in 0.3-5 GHz -1 dB bandwidth with, a maximum S_{21} of 16.1 dB, minimum NF of 3.25 dB, IIP3 of +5 dBm, IIP2 of +27 dBm, and a S_{21} less than -11 dB over the entire bandwidth.

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