A Ring-Type ILFD with Locking Range of 91% for Divide-by-4 and 40% for Divide-by-8 with Quadrature Outputs

Najmeh Hajamini and Mohammad Yavari
Integrated Circuits Design Laboratory, Department of Electrical Engineering,
Amirkabir University of Technology, Tehran, Iran
Emails: n.hajamini@aut.ac.ir, myavari@aut.ac.ir

Abstract: *In this paper, a low-power, wide locking range and quadrature output divide-by-4 and divide-by-8 ring-type injection-locked frequency divider (ILFD) is proposed. Two techniques are implemented in a two-stage ring ILFD to provide wide locking range and low power consumption at the same time. To widen the bandwidth, a common-gate tail configuration for injecting the signal is employed. Furthermore, the common-source node sharing topology is used to increase the operating frequency of the ILFD. This ILFD is designed in a 90 nm CMOS technology. Simulation results show that the proposed ILFD can provide the locking range of 91% for divide-by-4 and 40% for divide-by-8 at the incident power of -5 dBm and -10 dBm, respectively. It consumes about 1.57 mW at a supply voltage of 1.2 V.*

Keywords: divide-by-4, divide-by-8, Injection locked frequency divider (ILFD), locking range, ring oscillator.

1. Introduction

In high-speed communication systems, the frequency divider is one of the most critical building blocks for implementation of frequency synthesizers and phase locked loops (PLLs). In a PLL system, the VCO and the first-stage divider operate at the highest frequency and consume high dc power. Therefore, the design of frequency dividers is very important.

Flip-flop based frequency dividers are the basic structures that are selected for this approach. Using simple structures they are broadband and robust over the process variations [1]. But the maximum operating speed of these dividers is limited by the cut-off frequency (f_T) of the transistors and their power consumption is increased with the operation frequency. So, they are not suitable for high frequency purposes [2].

Injection locked frequency dividers (ILFDs) do not have the limitation of f_T. Thus, they can be used for applications at tens of gigahertz frequencies. An ILFD can be defined as an oscillator that is synchronized with an incident signal. There are two types of ILFDs: LC-type ILFDs [3-5] and ring-type ILFDs [6-11]. The problem with LC ILFDs is their narrowband characteristics due to the high quality factor (Q) of the LC tank. In addition, because of using inductors, they occupy large chip areas. On the other hand, with their low Q nature, ring-type ILFDs have large locking range and small chip areas [12]. The problem of low phase noise of the ring oscillators does not appear in the ring ILFDs. In an ILFD with divide ratio of N, the phase noise of the output signal follows that of the input with a $20\times logN$ reduction. So, it is mainly determined by the phase noise of the input source [13].

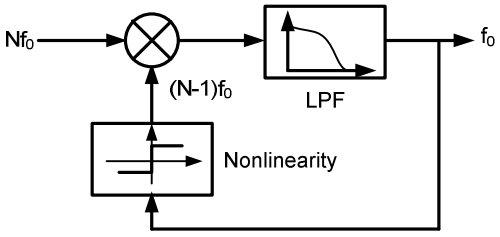


Fig. 1: Conventional ILFD model [6].

In this paper, a two-stage ring oscillator with multiple input injection is selected as the base of the proposed circuit. The two-stage ring oscillator can provide high frequency signals and has a good phase noise performance. It also produces quadrature output waveforms. Moreover, if it is improved with negative resistance load, it will be a power efficient structure [14]. The quadrature output waveform is one of the major requirements of subsequent blocks of frequency synthesizers such as mixers. Multiple input injection topology has been applied to the proposed ILFD to extend the locking range and to produce accurate quadrature outputs [2]. By implementing the common-gate tail configuration and common-source node sharing, we propose a new ILFD which provides wide locking range and low power consumption for division ratios of 4 and 8.

The paper is organized as follows. Section 2 presents a brief description of the convention ILFDs. Section 3 explains different parts of the proposed ILFD. The simulation results of the proposed ILFD are presented in Section 4. Finally, Section 5 concludes the paper.

978-1-4673-5634-3/13/$31.00 ©2013 IEEE

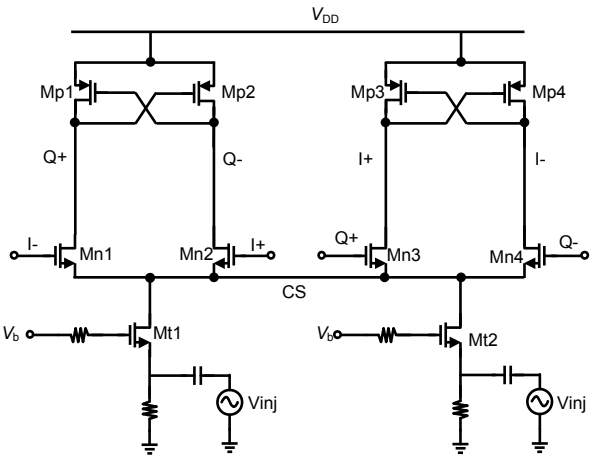


Fig. 2: Proposed ILFD using common-source node sharing topology and common-gate injection scheme.

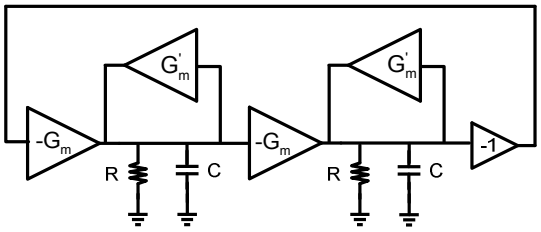


Fig. 3: Linearized model of a two-stage ring oscillator with a positive feedback [14].

2. Conventional ILFD

A conventional ILFD can be modelled as shown in Fig. 1. It consists of a nonlinear block, a low pass filter (LPF) and a mixer. The nonlinear block models all the nonlinearities in the oscillator, including any amplitude-limiting mechanism and the nonlinear transconductance of transistors [15]. In the case of ring-type oscillator, the low-pass behavior is due to the interaction of the output impedance of each buffer with the input capacitance of the following stage [16].

When a signal is injected to an oscillator, it mixes with all the harmonics that are generated from the nonlinear block. However, after passing through the LPF only the harmonics near the fundamental frequency is remained. If one of these harmonics has enough power, the oscillator frequency will be pulled and then it is locked to that harmonic.

If the divide ratio is N and the frequency of injected signal is Nf_0 (f_0 is the fundamental frequency), then the desired harmonic for mixing will be $(N\text{-}1)f_0$. It is clear that for high divide ratios, the desired harmonic is very weak [6]. So, proposing techniques for widening the locking range of these ILFDs is very important.

3. Proposed ILFD

The proposed ILFD is shown in Fig. 2. It is based on a two-stage ring oscillator that each delay cell consists of a differential pair (M_{n1}-M_{n2}) to provide G_m and a cross-coupled structure (M_{p1}-M_{p2}) as negative resistance load. The cross-coupled transistors relax the oscillation condition resulting in lower power consumption. It will be explained in Section 3.1 [14].

In this ILFD, the common-source (CS) node sharing topology is utilized to hold the tail transistor in the saturation region in whole of the period and this will result in covering high frequencies by ILFD [12]. This technique will be explained in Section 3.2.

In addition, since the common-gate tail configuration has the benefit of wide-bandwidth operation, it is employed in the proposed ILFD to widen the locking range [17]. Section 3.3 will describe this technique.

3.1 Two-stage ring ILFD with negative resistance load

Fig. 3 shows the linearized model for a two-stage ring oscillator where each delay cell consists of a transconductance stage (G_m), an RC delay part and an active positive feedback (G'_m). G'_m is equivalent to a negative resistance ($R_n = -1/G'_m$) that compensates the resistive losses and makes the oscillation condition achievable at much lower power consumption.

The open-loop transfer function of this model can be calculated as [14]:

$$H(j\omega) = -\left(\frac{-G_m.R_{eq}}{1+jR_{eq}C\omega}\right)^2 \quad (1)$$

where R_{eq} is:

$$R_{eq} = \frac{R.R_n}{R+R_n} \quad (2)$$

After the calculation of modulus and phase expressions of this transfer function, we will have Equation (3) for the oscillation condition and Equation (4) for the oscillation frequency:

$$G_m = \frac{1}{|R_{eq}|} = \left|\frac{1}{R} - G'_m\right| \quad (3)$$

$$\omega = \frac{G_m}{C} \quad (4)$$

Equation (3) shows that by adding negative resistance load $R_n = -1/G'_m$, a lower value of G_m can satisfy the oscillation condition. Therefore, the required power consumption is decreased in this structure.

In the circuit of Fig. 2, G_m and G'_m replace with $g_{m,n}/2$ and $g_{m,p}/2$, respectively. In order to size the transistors optimally, the proportionality ratio $A = G_m/G'_m$ is defined. In [14], the left and right terms of Equation (3) is plotted versus G_m. It is shown that there is a trade-off between two conditions: 1) obtain the oscillation condition for the smallest possible G_m in the region where $G_m < A/R$, and 2) ensure the oscillation to a maximum extent over $G_m > A/R$. However, our ILFD does not need extremely wide range of bias current since it works with a constant bias. So, it seems that the best choice for the value of A is slightly below 1.

3.2 Common-source node sharing topology

The PMOS cross-coupled loads provide high nonlinear operation in the circuit. It is a good condition for ILFDs because they need strong harmonics to provide large locking range. Therefore, the conventional ILFD model which considers the load as a linear block is not a suitable model to analyze this circuit. Instead, a large signal transient analysis has to be utilized.

Suppose that I^- has a low-to-high transition. Before transition M_{n1} is OFF and M_{p1} is in the triode region. Meanwhile M_{n2} is ON and M_{p2} is OFF. Right after the transition, M_{n1} goes to the saturation region but M_{p1} is still in the triode region and does not permit the parasitic capacitance of Q^+ node to be discharged completely. This state continues until Q^+ goes below (V_{DD}-$|V_{th}|$). After that M_{p2} enters into the saturation region and a positive feedback is set up. Then transitions at both outputs are very fast. Hence, the transition of Q^+ from V_{DD} to (V_{DD}-$|V_{th}|$) mainly determines the time-delay of the delay-cell.

During this transition state, M_{t1} is in the triode region because a part of the current from discharging the capacitance of Q^+ node is absorbed by M_{p1} that has a small resistance in the triode region. So, M_{t1} traverses from the triode to the saturation region at the end of the transition and it causes an additional time-delay. Thus, if the ILFD wants to have high frequency (low time-delay), the tail current must be constant in whole the period. To meet this demand, we can share the CS node of two stages. When one stage is in the transition mode, another one has exited from this state, so the tail current will be constant [12].

To have a wide locking range ring ILFD, an appropriate method is the injection of the input signal into multiple stages. If the injection were to modulate every stage's delay, this approach can be achieved [2].

The optimum input phase differences to achieve the maximum locking range is equivalent to the product of the division ratio and the phase shift contributed by the individual stages without input injections [18]. So, to implement this rule in a two-stage ring ILFD (as the proposed ILFD in this paper) to have a divide-by-4 and divide-by-8 ILFD, the phase difference between the injected signals into two stages is calculated by Equation (5). In this case, the phase shift contributed by the individual stages is /2.

$$\begin{aligned} phase-diff\ (div\,4) &= 4\times \pi/2 = 2\pi \\ phase-diff\ (div\,8) &= 8\times \pi/2 = 4\pi \end{aligned} \tag{5}$$

As can be seen from this equation, the required phase shift is the same in both cases. Because of connecting the tails of two stages in the proposed circuit, it requires the injected signals with the same phase. So, it is a good approach to implement the dividers with the division ratio of 4 and 8 using this ILFD.

In [12], an inequality is derived for the locking range of an ILFD where the injection signal is applied to the gate of the tail transistor. However, it can be used for the proposed circuit of this paper (where the injection signal is applied to the source) with a little change. This expression is calculated using the drain current of tail transistor and it will be the same for the common-gate circuit by replacing g_m with g_m+g_{mb}. Furthermore, this equation is not proportional to the number of ring oscillator stages. So, it is suitable for our ILFD. The locking range is calculated as:

$$\left|1-\frac{\left|V_{thp}\right|}{\left(1-\left(1-\left|V_{thp}\right|/I_B R_{out}\right)^{\frac{f_{osc-fr}}{f_{osc}}}\right) I_B R_{out}}\right| \le \frac{(g_{m,t}+g_{mb,t})V_{inj}}{I_B}\frac{1}{\sqrt{1+\left(\frac{2k\pi}{\ln(1-\left|V_{thp}\right|/I_B R_{out})}\frac{f_{osc}}{f_{osc-fr}}\right)^2}} \tag{6}$$

In this expression, $f_{osc,fr}$ denotes the free-running oscillation frequency and f_{osc} is the oscillation frequency in the injection locked condition. I_B and $g_{m,t}$ are the bias current and the transconductance of the tail transistor, respectively. R_{out} is the output resistance of M_{p1} in the triode region and k denotes the division ratio.

Equation (6) shows that replacing g_m with g_m+g_{mb} increases the locking range. This is one of the reasons to increase the locking range by using the common-gate injection versus the common-source one.

3.3 Common-gate injection scheme

If we consider a common-gate amplifier, it is clear that the simplified expression for its cut-off frequency is calculated as:

$$\omega_{cut-off} = \frac{1}{C_{gs}.1/g_m} \tag{7}$$

where C_{gs} is the gate-source capacitance and g_m is the transconductance of the transistor. The cut-off frequency for a common-source amplifier is much lower due to the gate-drain capacitance (c_{gd}) Miller effect. It is calculated as:

$$\omega_{cut-off} = \frac{1}{[C_{gs}+C_{gd}(1+g_m R_L^{'})+C_{gd}(R_L^{'}/R_s)]R_s} \tag{8}$$

where R_s and $R_L^{'}$ are the input source resistance and equivalent load resistance of the transistor. Consequently, in the case of common-gate amplifier, the cut-off frequency and the resultant bandwidth is larger than the common-source one. Thus, this scheme widens the locking range of the proposed ILFD.

4. Simulation Results

The proposed divider is designed and simulated in a 90-nm CMOS technology by using Spectre RF simulator. The divide-by-4 and divide-by-8 circuits consume 1.3-1.32 mA from a 1.2 V power supply. Fig. 4 shows the sensitivity curves in three cases: 1) conventional two-

TABLE I: Performance comparison between the proposed work and similar state-of-the-art ring ILFDs.

Ref.	Tech.	P_{inj} (dBm)	Freq. Range (GHz)	Locking Range (%)	V_{DD} (V)	P_{diss} (mW)	Division Number	FOM (%/mW)	FOM_T (%/mW^2)
This work	90-nm CMOS	-5	4.4-11.8	91	1.2	1.57	4	231.8	733.69
		-10	10.5-15.8	40			8	203.8	2038.21
[6]	65-nm CMOS	0	9.9-13.7	31.8	1.2	3.9	4	32.61	32.61
			21-24.8	15.1		7.1	8	30.97	30.97
[7]	0.13-µm CMOS	0	22.5-29	25.2	1.2	6	4	16.8	16.8
[8]	0.18-µm CMOS	3	5-8.1	47	1.8	3.6	8	55.3	52.34
[9]	0.18-µm CMOS	0	1.6*	22.2	1.8	6.8	4	13.06	13.06
			0.25*	1.7			8	2	2
[10]	0.18-µm CMOS	0	5.39-6.12	6.3	1.8	——	4	——	——
[11]	0.13-µm CMOS	-2.5	3.6-5.25	37.3	1.2	0.35**	4	426.3	758.06

Locking Range (%) = 100% ×2× (f_{max} - f_{min})/(f_{max} + f_{min})

FOM = [Locking Range (%)× Division number] / [P_{dc} (mW)]

FOM_T = [Locking Range (%)× Division number] / [P_{dc} (mW) × P_{inj}(mW)]

* Centre frequency

** Core P_{diss} only

stage ring ILFD with an in-phase injection signal into the gates of both stages, 2) the two-stage ring ILFD using CS node sharing topology with the injection signal as case (1) and 3) the proposed ILFD using CS node sharing and CG injection scheme with the same phase for two stages.

As can be seen from Fig. 4, at the injection power of 0 dBm, the locking ranges of these three cases are 1.6 GHz (31%), 6.6 GHz (76%) and 8 GHz (87%), respectively. The dc bias of tail transistors is 0.8 V for the first case and 0.6 V for two others.

Fig. 5(a) and (b) show the sensitivity curves of the proposed ILFD under different bias conditions for division ratios of 4 and 8, respectively. They show the best locking range of 4.4-11.8 GHz (91%) at the injection power of -5 dBm and V_b = 0.6 V for divide-by-4 and locking range of 10.5-15.8 GHz (40%) at the injection power of -10 dBm and V_b = 0.6 V for divide-by-8. Producing a wide locking range at low input power is one of the advantages of this ILFD.

TABLE I gives a comparison among the proposed ILFD and similar state-of-art ring ILFDs. It can be seen from this table that both simulated ILFDs achieve the widest locking range at lowest input power in their class. The power dissipation is very low in the proposed ILFD. However, this is calculated from simulation results while the other results (except [10]) are obtained from the measurement. So this is not a fair comparison, especially in power consumption. But the results are good enough, that can be assert if this circuit is fabricated, it still will be one of the best structures. This circuit also has the benefit of the quadrature output similar to the most other divide-by-4 circuits.

For a more detailed comparison, the figure of merit is defined as [19]:

$$FOM_T = \frac{[\text{Locking Range}(\%) \times \text{Division number}]}{[P_{dc}(mW) \times P_{inj}(mW)]} \tag{9}$$

where, P_{inj} and P_{dc} are the input power and dc power dissipation, respectively. The locking range is calculated as:

$$LR = [2(f_{max} - f_{min})/(f_{max} + f_{min})] \times 100\% \tag{10}$$

As can be seen from TABLE I, the FOM_T of the proposed ILFD is extraordinary higher than the others, except for [11]. One of the reasons of that is the benefit of our ILFD to work with low input power especially in the case of divide-by-8. To show the effect of low input power in FOM_T, a figure of merit without considering P_{inj} is presented as follows:

$$FOM = \frac{[\text{Locking Range}(\%) \times \text{Division number}]}{[P_{dc}(mW)]} \tag{11}$$

The results of FOM in TABLE I show that the proposed ILFD still maintains its benefits.

5. Conclusion

An ILFD with division ratios of 4 and 8 with a wide locking range and low power consumption was proposed and simulated in a 90-nm CMOS process. The proposed circuit is based on a two-stage ring oscillator with the common-gate injection scheme and using the common-source node sharing topology. It demonstrates the good

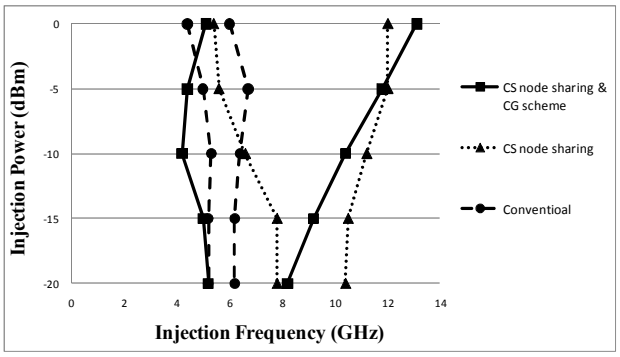
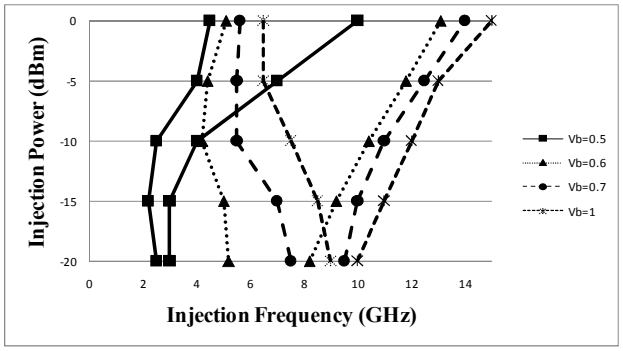
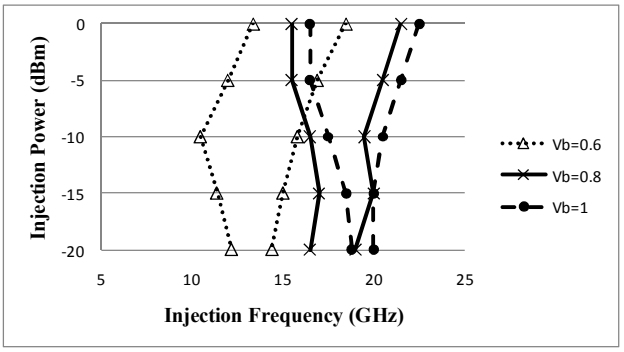


Fig. 4: Sensitivity curves of the divide-by-4 ILFDs in 3 cases



(a)



(b)

Fig. 5: Sensitivity curves of the proposed ILFD, under different bias conditions, in the case of (a) divide-by-4 and (b) divide-by-8.

performance of the wider locking range and lower power consumption than previously reported CMOS frequency dividers in the ratios of 4 and 8. The resultant input locking range is 91% and 40% at -5 dBm and -10 dBm input power for divide-by-4 and divide-by-8, respectively. It consumes only 1.56-1.58 mW at a supply voltage of 1.2 V. In addition to the mentioned advantages, this circuit is simple, small, and without extra control mechanisms.

Acknowledgements

The authors would like to express their sincere thanks to Dr. S. Saeedi for his valuable comments. This work has been financially supported in part by the Iranian Telecommunication Research Centre (ITRC).

References

[1] J. Plouchart, J. Kim, H. Recoules, N. Zsmdmer, T. Yue, M. Sherony, A. Ray, and L.Wagner, "A power-efficient 33 GHz 2:1 static frequency divider in 0.12-µm SOI CMOS," *IEEE Radio Frequency Integrated Circuits Symp.*, pp. 329–332, Jun. 2003.

[2] A. Mirzaei, M. Heidari, R. Bagheri, and A. Abidi, "Multi-phase injection widens lock range of ring-oscillator-based frequency dividers," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 656 – 671, Mar. 2008.

[3] S. L. Jang, J. C. Luo, C. W. Chang, C. F. Lee, and J. F. Huang, "LC-Tank Colpitts Injection-Locked Frequency Divider With Even and Odd Modulo," *IEEE Microwave and Wireless Component Letters*, vol. 19, no. 2, pp. 113-115, Feb. 2009.

[4] S. L Jang, C. F. Lee, and W. H. Yeh, "A Divide-by-3 Injection Locked Frequency Divider With Single-Ended Input," *IEEE Microwave and Wireless Component Letters*, vol. 18, no. 2, pp. 142 - 144, Feb. 2008.

[5] S. L. Jang, C. C. Liu, Y. H. Liao, and R. K. Yang, "A Wide-locking Range Divide-by-2 LC-tank Injection-Locked Frequency Divider," in *Proc. VLSI Circuits Symp.*, pp. 87 – 90, Apr. 2010.

[6] A. Musa, K. Okada, and A. Matsuzawa, "A 20GHz ILFD with Locking Range of 31% for Divide-by-4 and 15% for Divide-by-8 Using Progressive Mixing," *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp. 85-88, Nov. 2011.

[7] C.-C. Chen, C.-H. Wang, B.-J. Huang, H.-W. Tsao, and H. Wang, "A 24-GHz divide-by-4 injection-locked frequency divider in 0.13-µm CMOS technology," *IEEE Asian Solid-State Circuit Conference (A-SSCC) Proceedings*, pp. 340-343, Nov. 2007.

[8] S. Cheng, H. Tong, J. S. Martinez and A. I. Karsilayan "A Fully Differential Low-Power Divide-by-8 Injection-Locked Frequency Divider Up to 18 GHz," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 583-591, Mar. 2007.

[9] M. Acar, D. Leenaerts, and B. Nauta, "A wide-band CMOS injection locked frequency divider," *IEEE Radio Frequency Integrated Circuits Symp.*, Dig., pp. 211–214, Jun. 2004.

[10] S. L. Jang, Y. H. Chuang, S. H. Lee, and J. J. Chao, "Circuit techniques for CMOS divide-*by*-4 frequency divider," *IEEE Microwave and Wireless Component Letters*, vol. 17, no. 3, pp. 217-219, Mar. 2007.

[11] J. Lee, S. Park and S.H. Cho, "A 470-uW 5-GHz Digitally Controlled Injection-Locked Multi-Modulus Frequency Divider with an In-Phase Dual-Input Injection Scheme," *IEEE Transactions on VLSI Systems*, vol. 19, no. 1, pp. 61-70, Jan. 2011.

[12] H. Tong, S. Cheng, A. I. Karsilayan, J. S. Martinez, "An Injection-Locked Frequency Divider With Multiple Highly Nonlinear Injection Stages and Large Division Ratios," *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 54, no. 4, pp. 313, Apr. 2007.

[13] H. Wu, "Signal Generation and Preocessing in High-Frequency / High-Speed Silicon-Based Integrated Circuits," Ph.D dissertion, Univ. California, Pasadena, 2003.

[14] B. Fahs, W. Y. Ali-Ahmad, and P. Gamand, "A two-stage ring oscillator in 0.13-um CMOS for UWB impulse radio," *IEEE T. Microwave Theory and Techniques*, vol. 57, no. 5, pp. 1074-1082, May 2009.

[15] H. R. Rategh and T. H. Lee, "Superharmonic injection-locked frequency dividers," *IEEE J. Solid-State Circuits*, vol. 34, pp. 813–821, Jun. 1999.

[16] R. J. Betancourt-Zamora and S. Verma *et al.*, "1-GHz and 2.8-GHz CMOS injection-locked ring oscillator prescalers," in *Proc. VLSI Circuits Symp.*, pp. 47–50, Jun. 2001.

[17] X. P. Yu, M. A. Do, J. Ma, W. M. Lim, K. S. Yeo, and X. L. Yan, "Sub-1 V Low Power Wide Range Injection-Locked Frequency Divider," *IEEE Microwave and Wireless Component Letters*, vol. 17, no. 7, pp. 528 - 530, Jul. 2007.

[18] J. C. Chien and L. H. Lu, "Analysis and design of wideband injection locked ring oscillators with multiple-input injection," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1906–1915, Sep. 2007.

[19] Y. H. Kuo, J. H. Tsai, H. Y. Chang, and T. W. Huang, "Design and Analysis of a 77.3% Locking-Range Divide-by-4 Frequency Divider," *IEEE Trans. Microwave Theory and Techniques*, vol. 59, no. 10, pp. 2477-2485, Oct. 2011.