High-Speed Three-Stage Operational Transconductance Amplifiers for Switched-Capacitor Circuits

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Abstract— **In this paper, three-stage operational transconductance amplifiers (OTAs) for use in switched-capacitor (SC) circuits using nanometer CMOS technologies are described. Two three-stage OTAs, one with nested-Miller compensation (NMC) as a basic compensation scheme and another with damping factor control frequency compensation (DFCFC) as an advanced compensation scheme are presented. The open-loop small-signal analysis as well as the large signal-analysis for both OTAs are investigated and their speed performance is compared and discussed. Circuit level simulations are carried out using a 90 nm CMOS technology with HSPICE. Simulation results show that the NMC and the DFCFC OTAs achieve a settling time of 17.5 ns and 8.4 ns with 0.02% accuracy, respectively, while consuming 3 mW from a 1.2 V power supply and have the same input-referred thermal noise.**

Keywords- three-stag amplifiers; nested Miller compensation; damping factor control frequency compensation; switched-capacitor circuits.

I. INTRODUCTION

The operational transconductance amplifier (OTA) is a vital building block for analog integrated circuits. With continued CMOS technology scaling, the design of high gain and large swing OTAs has been more challenging because of reduced transistor's inherent gain ($g_m.r_o$) and power supply. To achieve high gain and large swing simultaneously, three-stage OTAs can be used [1, 2]. However, owing to many poles, the frequency compensation of three-stage OTAs is more difficult. Various frequency compensation techniques such as the nested Miller compensation (NMC) [3] and its variants, active feedback frequency compensation (AFFC) [4], damping factor control frequency compensation (DFCFC) [5], and several other structures are presented in literature. These structures are mainly proposed to be used in low droop-out (LDO) regulators, where the amplifier drives a large capacitive load and the required gain-bandwidth is low. Although the use of three-amplifier stages for low-speed, low-power applications is discussed extensively in literature, but there are a few publications that investigate the use of three-stage OTAs for switched-capacitor (SC) circuits [6-8]. In addition, these publications only target the design methodologies to achieve fast-settling three-stage OTAs and do not address the inherent limitations of three-stage OTAs such as the excessive power consumption, large die area, etc.

For instance, to ensure the stability of NMC OTA, the last stage transconductance must be much greater than the first and second stage transconductances to push the non-dominant poles into high frequencies resulting in more power consumption. Besides, in an NMC OTA, the size of the compensation capacitors is large and this increases the die area, as well as it limits the slew rate of the amplifier. As well-known, in SC circuits, the slew rate is among the important performance metrics of an OTA which limits the settling time. Large and small signal limitations of an NMC OTA are mainly because of the nested configuration of compensation capacitors. The variants of an NMC OTA have also these limitations.

To solve deficiency of an NMC OTA, using of DFCFC structure in SC circuits is proposed. The DFCFC structure has been proposed for large capacitive load applications in [5] and is one of the most power efficient three-stage amplifiers already exist in literature. In this paper, the use of DFCFC structure to realize fast-settling three-stage OTAs is investigated and compared with the three-stage NMC OTA.

The rest of the paper is organized as follows. In Sect. II, the basic block diagram and a typical fully-differential implementation of the NMC OTA are described. In Sect. III, the DFCFC OTA is introduced and its basic block diagram as well as its fully-differential implementation are presented. In Sect. IV, the circuit level simulation results are provided and a comparison is performed between the achieved performance of NMC and DFCFC OTAs. Finally, Sect. V concludes the paper.

II. THREE-STAGE NMC OTA

The simplest compensation scheme to stabilize three-stage OTAs is the NMC structure. It is an extended form of the Miller compensation that exploits the pole-splitting technique. The basic block diagram of a three-stage NMC OTA is shown in Fig. 1, where g_{mi}, C_i, and r_{oi} represent the i-th stage transconductance, the equivalent parasitic capacitance, and the output resistance of the corresponding gain stages, respectively. C_L includes the load capacitor as well as the output parasitic capacitor of the third stage. The capacitors C_{m1} and C_{m2} perform the nested Miller compensation providing the closed-loop response stability [3]. A typical fully-differential circuit implementation of the three-stage NMC OTA is shown in Fig. 2 where three differential pairs with active loads are used to realize the amplifier stages. Using three identical gain stages similar to the first stage is another way to implement the NMC

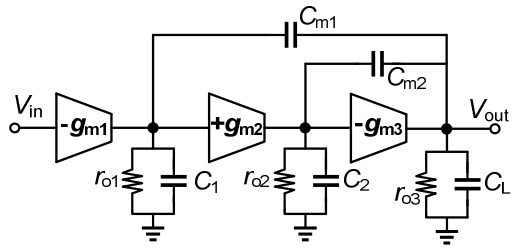

Figure 1. Block diagram of three-stage NMC OTA.

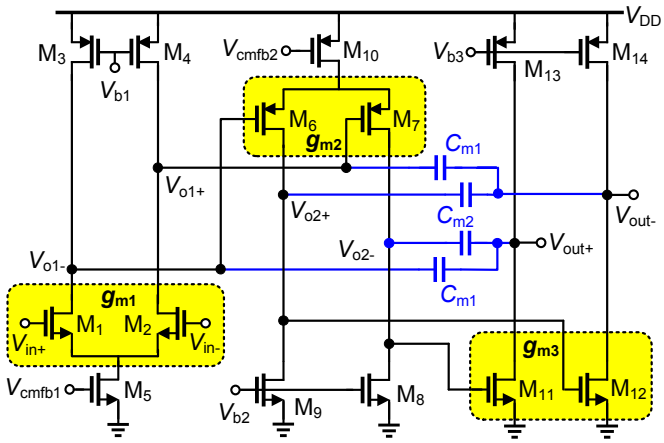

Figure 2. A typical fully-differential circuit implementation of thee-stage NMC OTA (bias and CMFB circuits are not shown for simplicity).

OTA as presented in [1]. But, the implemented NMC OTA in Fig. 2 has large output voltage swing since the tail transistor in the last stage is removed. Two independent switched-capacitor common-mode feedback (CMFB) circuits are used to define the output common-mode voltage of the amplifier stages. The first CMFB circuit determines the output common-mode voltage of the first stage and the second one fixes the output common-mode voltages of both second and third stages in the same CMFB loop. In the second CMFB circuit, the common-mode control signal should be inverted to have a negative feedback loop.

A. Small-Signal Analysis

By assuming high intrinsic dc gain in amplifier stages and compensation and load capacitors are much greater than all parasitic capacitances of the circuit, i.e. $g_{mi}r_{oi} >> 1$ and C_L, C_{m1}, $C_{m2} >> C_{1,2}$, the open-loop signal transfer function of NMC amplifier is given by:

$$A_{NMC}(s) = A_0 \frac{1 - \frac{C_{m2}}{g_{m3}}s - \frac{C_{m1}C_{m2}}{g_{m2}g_{m3}}s^2}{(1 + sr_{o1}g_{m2}r_{o2}g_{m3}r_{o3}C_{m1})} \times \frac{1}{(1 + s\frac{C_{m2}}{g_{m2}} + s^2\frac{C_{m2}C_L}{g_{m2}g_{m3}})} \quad (1)$$

where $A_0 = g_{m1}g_{m2}g_{m3}r_{o1}r_{o2}r_{o3}$ is the dc gain of NMC OTA and $\omega_{p1} = 1/r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}C_{m1}$ is the dominant pole. The gain-bandwidth product (ω_{GBW}) of the OTA is well approximated by the open-loop unity-gain frequency as $\omega_{GBW} = g_{m1}/C_{m1}$. There are two zeros in the transfer function of an NMC OTA where one of them is a right half plane (RHP) zero and another is a left half plane (LHP) zero. The RHP zero can potentially degrade the stability of the amplifier. However, the zeros are located at high frequencies; so their overall effect in the stability is negligible. A number of nested Miller topologies are proposed in literature to alleviate the effect of the zeros [9-11]. The NMC OTA has two non-dominant complex poles with the following natural frequency and damping factor:

$$\omega_n = \sqrt{\frac{g_{m2}g_{m3}}{C_{m2}C_L}} \quad (2)$$

$$\zeta = \frac{1}{2}\sqrt{\frac{C_{m2}}{C_L}}\sqrt{\frac{g_{m3}}{g_{m2}}} \quad (3)$$

According to [6], the damping factor of the non-dominant complex poles has a significant effect in the settling behavior of a three-stage amplifier and a properly adjusted open-loop damping factor is essential to have a fast-settling three-stage amplifier. From (3) it is seen that C_{m2} controls the damping factor of the non-dominant poles. To achieve the required damping factor, the size of C_{m2} can be set according to the following:

$$C_{m2} = 4\zeta^2\frac{g_{m2}}{g_{m3}}C_L \quad (4)$$

Neglecting the effect of the zeros in the phase margin, the size of C_{m1} can be found based on the required phase margin (PM) and damping factor (ζ) as [12]:

$$C_{m1} = 2\zeta\left(\zeta\tan(PM) + \sqrt{\zeta^2\tan^2(PM)+1}\right)\frac{g_{m1}}{g_{m3}}C_L \quad (5)$$

The obtained dimension conditions for C_{m1} and C_{m2} clearly show that in order to have small compensation capacitances, the value of g_{m3} must be much greater than that of g_{m1} and g_{m2}. To hold this condition one way is to consider small values for g_{m1} and g_{m2}. But, this solution limits the slew rate of the NMC OTA and increases the input-referred noise. Another way is increasing the value of g_{m3} that leads to excessive power dissipation. Based on these considerations, the NMC OTA is not a power efficient structure for high-speed applications.

B. Large-Signal Analysis

When a large step is applied to the OTA's input, the step response of OTA has two different behaviors. At the beginning of the step response and due to the limited current of the amplifier stages, the output of the OTA rises with a constant rate. It can readily be shown that during slewing, the differential slew rate at the stages output is given by:

$$SR_1 = \frac{I_{D5}}{C_{m1}} \quad SR_2 = \frac{I_{D10}}{C_{m2}} \quad SR_3 = \frac{2I_{D13} - I_{D5} - I_{D10}}{C_L} \quad (6)$$

where I_{D5}, I_{D10}, and I_{D13} are the drain current of M_5, M_{10}, and M_{13} in Fig. 2, respectively. The minimum of SR_1, SR_2, and SR_3 limits the slew rate of an NMC OTA, i.e. $SR = \min(SR_1, SR_2, SR_3)$. In SC Circuits, the load capacitance is small while because of small-signal considerations, the bias current of the last stage is much greater than that of first and second stages.

So, the first stage most likely will limit the slew rate of the NMC OTA, considering that usually the size of C_{m1} is greater than that of C_{m2}.

III. DFCFC THREE-STAGE OTA

As illustrated in previous section, the presence of C_{m2} in the NMC OTA is necessary to have the appropriate damping factor to prevent the step response of the NMC OTA from oscillating. However, according to (2), C_{m2} lowers the natural frequency of the non-dominant complex poles. Therefore, to push the non-dominant poles into high frequencies and extend the gain-bandwidth, more power must be consumed. To solve this problem, the DFCFC structure can be used to stabilize the three-stage OTA. The block diagram of a three-stage DFCFC OTA is shown in Fig. 3. With respect to the NMC OTA, C_{m2} (connected between input and output of the last stage in Fig. 1) is removed. Instead, a damping factor control (DFC) block is added. The DFC block is simply made up from an inverting amplifier with transconductance g_{m4} and capacitor C_{m2}. A typical fully-differential implementation of a DFCFC OTA is shown in Fig. 4, where transistors M_{11}-M_{14} with capacitor C_{m2} are used to implement the DFC block.

A. Small-Signal Analysis

By the same simplifying assumptions made for open-loop analysis of an NMC OTA, the transfer function of DFCFC amplifier can be obtained as follows:

$$A_{DFCFC}(s) = A_0 \frac{1-\frac{C_{m1}g_{m4}}{g_{m2}g_{m3}}s-\frac{C_{m1}(C_2+C_4)}{g_{m2}g_{m3}}s^2}{(1+sr_{o1}g_{m2}r_{o2}g_{m3}r_{o3}C_{m1})} \times \frac{1}{(1+s\frac{C_Lg_{m4}}{g_{m2}g_{m3}}+s^2\frac{(C_2+C_4)C_L}{g_{m2}g_{m3}})} \quad (7)$$

where $A_0 = g_{m1}g_{m2}g_{m3}r_{o1}r_{o2}r_{o3}$ is the dc gain of DFCFC OTA and $\omega_{p1} = 1/r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}C_{m1}$ is the dominant pole. It is worth to mention that the effect of C_{m2} is canceled in the transfer function due to the existence of a pole-zero doublet at the frequency near $1/(r_{o4}(C_{m2}+C_4))$. The only dimension condition for C_{m2} is that its value must be much greater than that of parasitic capacitance C_2, i.e. $C_{m2} >> C_2$.

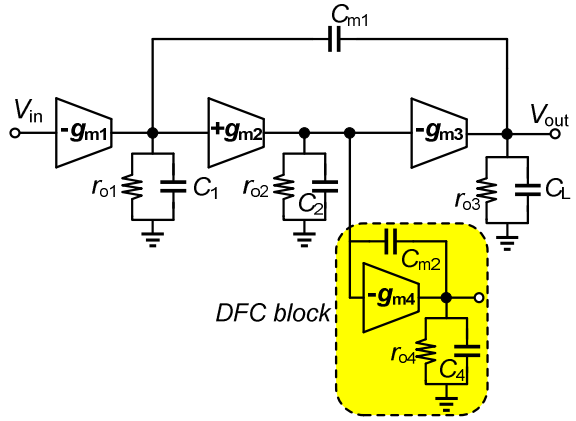

Figure 3. Block diagram of a three-stage DFCFC OTA

The gain-bandwidth of DFCFC OTA is simply given by $\omega_{GBW} = g_{m1}/C_{m1}$. The transfer function also has one LHP zero and another RHP zero. Similar to the NMC OTA, the overall effect of zeros on the stability margin is small and so it can be neglected for simplicity. The damping factor and natural frequency of non-dominant complex poles are as follows:

$$\zeta = \frac{1}{2}\sqrt{\frac{g_{m4}^2}{g_{m2}g_{m3}}}\sqrt{\frac{C_L}{C_2+C_4}} \quad (8)$$

$$\omega_n = \sqrt{\frac{g_{m3}}{C_L}\times\frac{g_{m2}}{C_2+C_4}} \quad (9)$$

The damping factor of DFCFC amplifier can be easily controlled by selecting an appropriate value of g_{m4} and fortunately small g_{m4} is needed for this purpose. In comparison with an NMC OTA, the non-dominant poles are located at higher frequencies since C_2 and C_4 are small parasitic capacitances. Hence, the gain-bandwidth of DFCFC OTA can be extended. Indeed, the power efficiency of DFCFC OTA is mainly because of this issue. It can be easily shown that the gain-bandwidth improvement is given by:

$$\frac{\omega_{GBW,DFCFC}}{\omega_{GBW,NMC}} = \sqrt{\frac{C_{m2,NMC}}{C_2+C_4}} \quad (10)$$

In above equation, it is assumed that both of OTAs have the same phase margin and damping factor. By assumption that the effect of zeros in the phase margin is negligible, the size of C_{m1} can be obtained as:

$$C_{m1} = \frac{g_{m4}g_{m1}}{g_{m2}g_{m3}}\frac{\zeta\tan(PM)+\sqrt{\zeta\tan^2(PM)+1}}{2\zeta}C_L \quad (11)$$

B. Larg- Signal Analysis

The slew rate of an OTA not only depends on the available current for charging or discharging its capacitors, but also depends on the size of its compensation capacitors. From this point of view, the compensation schemes requiring small compensation capacitors are preferable. It can be shown that the slew rate of DFCFC OTA is given by:

$$SR = \min\left(\frac{I_{D5}}{C_{m1}}, \frac{2I_{D17}-I_{D5}}{C_L}\right) \quad (12)$$

where I_{D5} and I_{D17} are the drain current of M_5 and M_{10} in Fig. 4, respectively. In the case of small C_L and owing to large bias current at the last stage of three-stage OTAs, it is expected that the bias current of first stage will limit the slew rate. In comparison with the NMC OTA, for the equal value of g_{m1} and so I_{D5}, the size of C_{m1} can be lowered by the same factor as the gain-bandwidth enhancement given by (10). Therefore, the slew rate of DFCFC OTA would be enhanced by the same factor.

IV. SIMULATION RESULTS

In order to compare the performance of NMC and DFCFC OTAs, two OTAs shown in Fig. 1 and Fig. 4, were designed

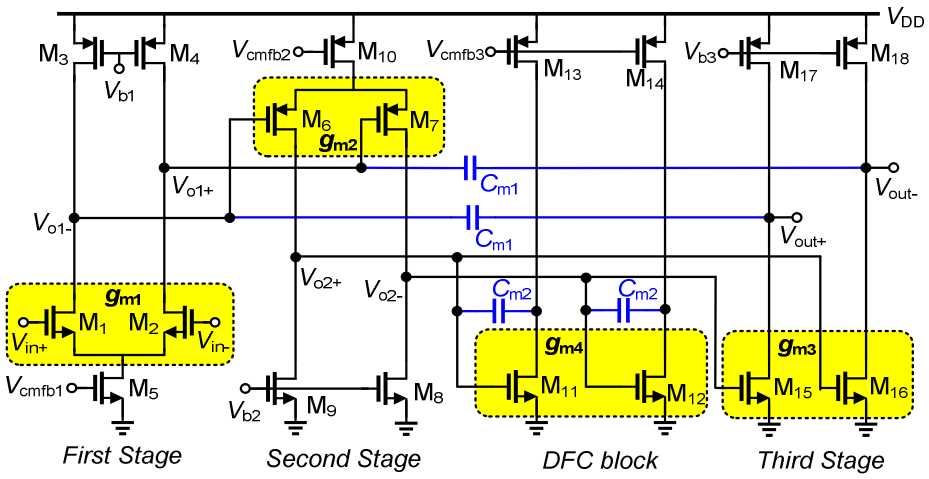

Figure 4. A typical fully-differential circuit implementation of a thee-stage DFCFC OTA (bias and CMFB circuits are not shown for simplicity).

and simulated using a 90 nm CMOS technology with HSPICE. The OTAs are used in a fully-differential flip-around S/H configuration while driving an effective load capacitance of C_L = 2 pF. The S/H circuit is designed to be used in an 11-bit pipelined ADC with 2 V_{pp} differential input and 1 pF sampling capacitor. The OTAs have been designed such that the power dissipation and input-referred noise of both of them to be equal so that the achieved speed performances can be fairly compared. To have the same input-referred noise for two OTAs, dimension of the transistors in the first stages have been chosen identically. In these simulations, the same bias currents have been used and corresponding transistors of amplifier stages have the same overdrive voltages. The designed device dimensions for NMC and DFCFC OTAs are shown in Table I and Table II, respectively. The simulation results are summarized in Table III. The step response of the designed NMC and DFCFC OTAs are shown in Fig. 5 and Fig. 6, respectively. A 1 V input step is applied to the OTAs' input to consider both of linear and nonlinear settling behaviors. Simulation results show that the achieved speed performance metrics (gain-bandwidth, slew rate, and settling time) for the DFCFC OTA are enhanced about 2 times with respect to the NMC one. In addition to improvement of speed, the DFCFC OTA's die area is smaller than that of the NMC OTA because of smaller compensation capacitors.

TABLE I. SIMULATED DEVICE SIZES OF NMC OTA

Parameter	W/L	g_m (mA/V)
M_1, M_2	3×1μm/0.2μm	**1.0 (g_{m1})**
M_3, M_4	3×6μm/0.3μm	1.1
M_5	6×1μm/0.2μm	1.9
M_6, M_7	4×4.5μm/0.2μm	**1.4 (g_{m2})**
M_8, M_9	4×1.5μm/0.3μm	1.2
M_{10}	8×4.5μm/0.2μm	2.7
M_{11}, M_{12}	15×2μm/0.2μm	**10.5 (g_{m3})**
M_{13}, M_{14}	15×12μm/0.3μm	11.4
C_{m1}, C_{m2}	1.4 pF, 0.9 pF	

TABLE II. SIMULATED DEVICE SIZES OF DFCFC OTA

Parameter	W/L	g_m (mA/V)
M_1, M_2	3×1μm/0.2μm	**1.0 (g_{m1})**
M_3, M_4	3×6μm/0.3μm	1.1
M_5	6×1μm/0.2μm	1.9
M_6, M_7	3×4.5μm/0.2μm	**1.0 (g_{m2})**
M_8, M_9	3×1.5μm/0.3μm	0.92
M_{10}	6×4.5μm/0.2μm	2.0
M_{11}, M_{12}	13×2μm/0.2μm	**9.1 (g_{m3})**
M_{13}, M_{14}	13×12μm/0.3μm	9.9
M_{15}, M_{16}	2×2μm/0.2μm	**1.4 (g_{m4})**
M_{17}, M_{18}	2×12μm/0.3μm	1.5
C_{m1}, C_{m2}	0.7 pF, 0.3 pF	

TABLE III. SIMULATION RESULTS SUMMARY

Parameter	NMC			DFCFC		
	TT@ 27°C	**SS@ 85°C**	**FF@ –40°C**	**TT@ 27°C**	**SS@ 85°C**	**FF@ –40°C**
DC gain (dB)	72.9	71.2	74.7	72.8	71.2	74.7
f_{GBW} (MHz)	110.7	92.4	141.7	221.5	184.3	284.9
Phase margin (degree)	61.3	62.9	59.1	61.6	63.4	59.2
0.02% settling time (t_s), @ 1 V input step (ns)	17.5	20.7	14.5	8.4	9.9	7.2
Slew rate (V/μs)	120.9	115.0	127.6	244.5	231.6	259.5
Input-referred noise density @ 100 kHz (nV/√Hz)	68.3	71.1	64.2	68.3	71.1	64.2
Power dissipation (mW)	3.0	2.9	3.0	2.9	2.9	3.0
V_{DD}	1.2 V					
Technology	90 nm CMOS					

V. CONCLUSION

Two three-stage OTAs with NMC and DFCFC compensation schemes were designed and simulated in this paper. For the same power consumption and input-ferreted thermal noise, the achieved speed performance for DFCFC OTA is superior to the NMC one that means DFCFC compensation is more suitable to realize fast-settling three-stage OTAs for high-speed switched-capacitor circuits.

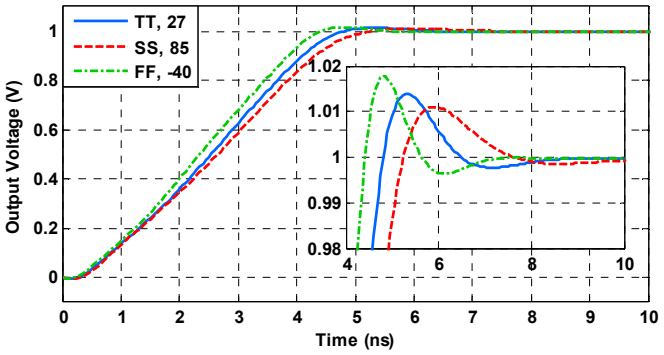

Figure 5. Step responsse of DFCFC OTA to 1 V differential input step.

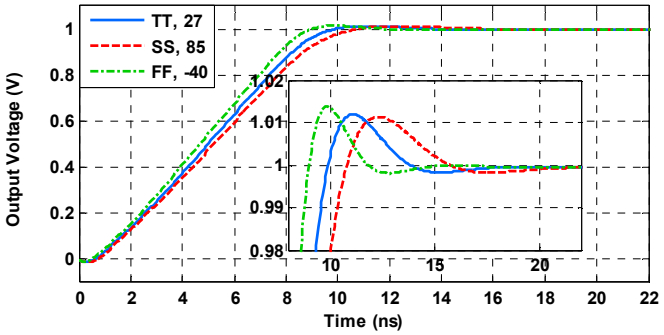

Figure 6. Step responsse of NMC OTA to 1 V differential input step.

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