A Fully Digital Calibration Technique for Nonlinearity Correction in Pipelined ADCs

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***Abstract*— A digital background calibration is proposed to address finite dc gain of amplifier, capacitors mismatch and nonlinearity of amplifier. Two extra comparators and an interpolation filter are utilized to implement a virtual ADC. The proposed calibration, calibrate gain error and nonlinearity of a 1.5 bits per stage pipelined ADC. The difference of virtual ADC and the ADC are utilized to drive a Least Mean Square (LMS) machine to estimate inverse coefficient of Multiplying Digital to Analog Converter (MDAC). The proposed calibration is tested on 12 bit, 100 MS/s pipelined ADC. The capacitor mismatch is set to 0.1% and the amplifier gain is set to 30 dB. The spurious free dynamic range (SFDR) and signal to noise and distortion ratio (SNDR) are both increased from 40 dB and 35.5 dB to 87 dB and 73 dB respectively.**

Keywords- Pipeined ADCs, nonidealities in pipelined ADCs, digiral bcackground calibration, LMS algorithm, Virtual ADC.

I. INTRODUCTION

The advances in wireless communication systems require high-speed and high-resolution analog to digital converters (ADCs). The pipelined ADCs are the best candidate for such a resolution and speed. The resolution and speed of pipelined ADC is limited by capacitors mismatch and amplifier of multiplying digital to analog converter (MDAC) .In order to achieve high-resolution and high-speed pipelined ADCs, a high speed amplifier with high dc gain is needed. However, scaling of CMOS technology reduced intrinsic gain of transistors. Additionally, low voltage CMOS technology deteriorate linearity of amplifier. Hence, design of high gain, high speed and linear amplifier lead to huge power consumption. Moreover, power consumption is an issue for portable devices such as cellular phones [1]-[10].

While scaling CMOS technology deteriorate analog performance, it alleviate digital performance. Scaling CMOS technology lead to high speed and low power digital circuits. Therefore, it is desirable to use simple amplifier in conjunction with digital background calibration [5].

Recently, various digital background calibrations are presented in the literature. In [6] and [7], digital background calibration address gain error and nonlinearity of residue amplifier and need lots of digital processing. The main problem of calibration presented in [6] and [7] is that they take a long time to converge. Method of [1] needs extra phase to perform digital background calibration. However, it utilizes simple model for MDAC that may be easily calibrated. Digital background calibration which is presented in [2] is based on statistical properties of output of ADC and it take a long time to converge. Same method which is used in [2], is used in [3] but method of [3] uses split ADC architecture to reduce the convergence time of calibration. Digital background calibration which is used in [4], [5] and [9] perform calibration in foreground mode and by using nonlinear interpolation filter or prediction filter, these method change calibration into background mode.

In [11], digital background calibration was presented for split ADC architecture. Digital calibration proposed in [11], addressed the gain error of MDAC amplifier and its DAC. The problem of the split ADC architecture is mismatch between two channels. In [11] an extra gain is implemented after the backend ADC of one channel. However, this gain is unable to eliminate mismatch between channels. In [12], a digital background calibration technique is proposed which MDAC has two feature. The first one is conventional structure for MDAC and the second is an amplifier. Based on the output of this feature, nonidealities of MDAC would be estimated. On the other hand, it needs interruption. In order to avoid the problem of split ADC architecture, two extra comparators and an interpolator is added to architecture of the pipelined ADC. Based on the input of the MDAC, one of the two feature of [12] is utilized. By utilizing interpolator and two extra comparators virtual ADC like [13] is achieved.

The paper is organized as follows. In Sect. II, the ADC structure and MDAC modeling is presented. The proposed digital background calibration technique is described in Sect. III. Section IV presents the simulation results. Finally, the conclusions are given in Section V.

II. ADC STRUCTURE AND MDAC MODELING

To examine the proposed calibration technique, as shown in Fig. 1, a 12-bit two-stage pipelined ADC consisting of a 1.5-bit first stage followed by an 11-bit ideal backend ADC is used. Each 1.5-bit stage estimates 1.5-bit digital equivalent of analog input signal with a coarse ADC also called sub-ADC. Then digital value converted back to analog domain with a three level digital-to-analog converter (DAC) also called sub-DAC and subtracted from input signal. Finally the result is amplified ideally by a gain of two to produce residue signal. Subtraction and amplification in each stage is implemented

with a switched-capacitor circuit called multiplying digital to analog converter (MDAC).

Figure 2 shows single-ended implementation of MDAC structure in this paper. Capacitor non flip around (CNFA) structure is used instead of commonly used capacitor flip around (CFA) structure to simplify its modeling with less coefficients [4].

The MDAC of Fig. 2 works in two non-overlapping clock phases, Φ_1 and Φ_2. In Φ_1 phase, it samples the input signal, V_{in}, on sampling capacitor, C_s. In the next phase, Φ_2, capacitor C_F is configured in feedback configuration and C_S is switched to DAC voltage, $V_{DAC}=DV_{ref}/2$, to produce residue signal, $V_{res}=2(V_{in}- DV_{ref}/2)$.

Due to capacitor mismatch and opamp finite gain as non-ideal factor of ε, residue is degraded to $2(1+\varepsilon)(V_{in}-V_{DAC})$. If nonlinearity of opamp is taken into account, high-order terms of $(V_{in}-V_{DAC})$ should be considered in the residue. In practice, nonlinearity up to third-order is enough to model opamp nonlinearity in the residue [4]. So, residue will be:

$$V_{res} = \alpha_1 (V_{in} - V_{DAC}) + \alpha_3 (V_{in} - V_{DAC})^3 \quad (1)$$

where α_1 and α_3 contain circuit imperfection including capacitor mismatch, opamp finite gain and its nonlinearity. In (1), second-order errors are neglected because differential structure is considered for MDAC.

In ideal residue, α_1 and α_3 will be 2 and 0 respectively. However, due to non-ideal factors these coefficients will be different from their ideal values. The residue voltage as function of input signal is depicted in Fig. 3(a). As clear from this figure, due to non-ideal factors, gain error and gain nonlinearity are resulted in residue. The residue V_{res} is digitized into D_{res} by the backend ADC and the whole digital output of the ADC is

$$\begin{aligned} D_{out} &= 0.5(D_{res} + D) \\ &= 0.5\left(\alpha_1 (D_{in} - 0.5D) + \alpha_3 (D_{in} - D)^3 + D\right) \end{aligned} \quad (2)$$

where D_{in} is the ideal quantized value of input signal. According to (2) digital output is far from the ideal digital value of V_{in} due to α_1 and α_3. In other words, only with $\alpha_1=2$ and $\alpha_3=0$ the ideal digital value of V_{in} can be achieved. Digital output of the ADC as function of input signal is shown in Fig. 3(b). It shows that digital output has gaps in decision points of sub-ADC and also it is nonlinear which will degrade the ADC's performance.

III. Prposed Digtal Background Calibration

In order to perform digital calibration, the inverse of *f(.)* should be implemented in digital domain. Inverse function of *f(.)* may be approximated by a third order polynomial [4]:

$$\begin{aligned} V_r &= \beta_1 V_{res} + \beta_3 V_{res}^3 \\ \beta_1 &= \frac{1}{\alpha_1}, \quad \beta_3 = -\frac{\alpha_3}{\alpha_1^4} \end{aligned} \quad (3)$$

We should estimate β_1 and β_3 in order to achieve a digital background calibration. By implementing inverse model of MDAC in the digital domain the nonidealities of MDAC can be calibrated.

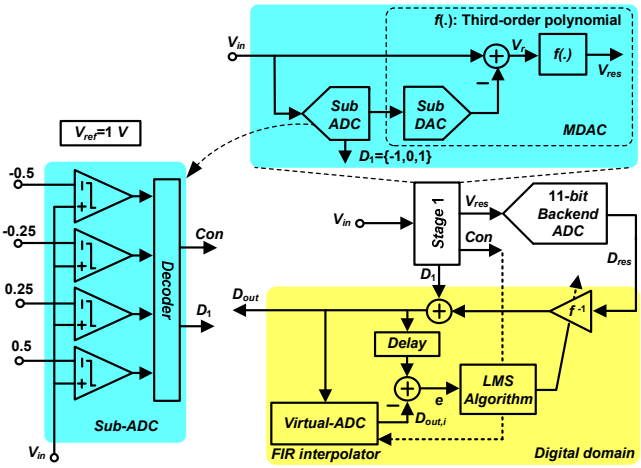

Figure 1. Proposed Virtual-ADC based calibration technique.

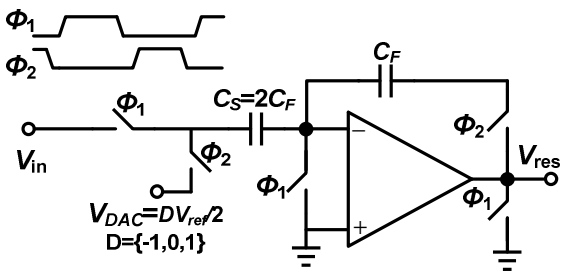

Figure 2. single-ended implementation of CNFA MDAC structure.

A. Underlying Concept

The calibration technique which presented in [12] measures the coefficients in (1) by using a calibration signal. In the following, the measurement process of [12] is described in foreground mode.

In the foreground mode, it is supposed that the ADC is stopped and it can impose the calibration signal. To calibrate the first stage, it is assumed that stage suffers only from the linear error and the backend stages are ideal. In other words, the stage output is perfectly digitized by backend stages, so:

$$D_{out} = D_1 + \beta_1 D_{res} \quad (4)$$

where D_{out} and D_{res} are the digital equivalent of the output of the ADC and the output of backend respectively. Moreover, D_1 is the first stage sub-ADC digital output and β_1 is its linear term inverse coefficient.

To apply the calibration technique, the first stage is configured as a two-mode stage. Consider that a constant calibration signal, V_1, with the value of slightly greater than $0.25V_{ref}$ (comparator threshold voltage) is applied to the stage input. The calibration signal is digitized in two different manners. First, as shown in Fig. 3(a) with stage transfer function, the first stage is configured as 1.5-bit configuration and then its sub-ADC digital output, $D_1=1$, and the digitized output for $0.25V_{ref}$ as the test input signal, D_{res1}, are stored in a memory. Second, as shown in Fig. 3(b), the stage is configured as a multiply-by-two configuration and the digitized output for V_1,

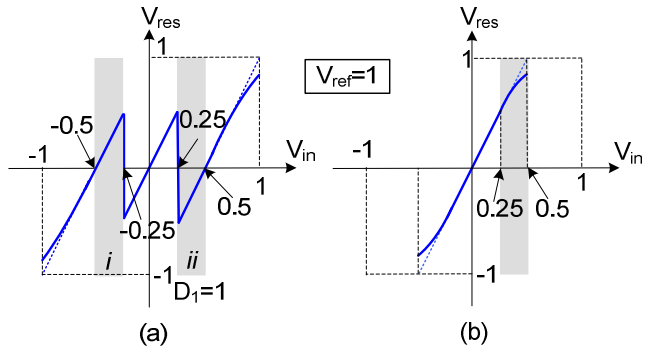

Figure 3. Stage transfer function in calibration (a) 1.5-bit configuration, (b) Multiply-by-two configuration.

D_{res2}, is stored in a memory too. With this two stored data and known β_{3i}=0, it is resulted from (2) that

$$V_{in}=V_1 \rightarrow \quad D_{out1}=D_1+\beta_1 D_{res1}, \quad D_{out2}=\beta_1 D_{res2} \tag{5}$$

Note that the stage input is the same in the two processes (D_{out1}=D_{out2}), so:

$$\beta_1(D_{res2}-D_{res1})=D_1 \tag{6}$$

Therefore, the coefficient can be extracted from two stored values and the stage sub-ADC digital output in 1.5-bit configuration. In other words, with no need for accurate calibration signal, β_1 is extracted. In the first stage coefficient extraction, it was supposed that the stage output is perfectly digitized with backend stage. Extending the applied technique, the nonlinear term coefficient in the stage inverse function can be extracted too. If the full scale input is applied to the amplifier, maximum deviation from ideal input-output function is obtained. With this view, another calibration signal which is equal to $0.5V_{\text{ref}}$ is used too. Since the stage is used in the multiply-by-two configuration, so the maximum input value would be $0.5V_{\text{ref}}$. But, if the amplifier has an offset voltage, the input amplitude would be limited more. So for nonlinear coefficient extraction, the second calibration signal value, V_2, would be slightly less than $0.5V_{\text{ref}}$. Consequently, to extract both linear and nonlinear term coefficients together, V_1 and V_2 are applied to the stage and the results are stored in the memory to be used by the Least Mean Square (LMS) algorithm. With stored results, it yields from (1):

$$\begin{aligned} V_{in}=V_1,V_2 \rightarrow & \begin{cases} D_{out1}=D_1+\beta_1 D_{res1}+\beta_3 D_{res1}^3 \\ D_{out2}=\beta_1 D_{res2}+\beta_3 D_{res2}^3 \end{cases} \\ \Rightarrow & \beta_1(D_{res2}-D_{res1})+\beta_3(D_{res2}^3-D_{res1}^3)=D_1 \end{aligned} \tag{7}$$

So, the coefficient can be extracted with the following equation:

$$\begin{aligned} \beta_1(n+1)&=\beta_1(n)+\mu_1 e(n).(D_{res2}-D_{res1}) \\ \beta_3(n+1)&=\beta_3(n)+\mu_3 e(n).(D_{res2}^3-D_{res1}^3) \end{aligned} \tag{8}$$

where μ_1 and μ_3 are the LMS update step size in the coefficients extraction and *e(n)* is given by:

$$e(n)=1-\beta_1(n)(D_{res2}-D_{res1})-\beta_3(n)(D_{res2}^3-D_{res1}^3) \tag{9}$$

The discussed calibration method of above is turned into background mode by using interpolation filter. In order to avoid interruption in normal operation of ADC, like [13], a virtual based digital background calibration is proposed.

B. Prposed Calibration Technique

The technique of [12] inject a calibration signal to ADC and utilize MDAC in two mode in order to address MDAC nonidealities. In the 1.5-bit stage, decision points are located around $\pm 0.25V_{ref}$. As depicted in Fig. 1, two extra comparators with decision points at $-0.5V_{ref}$ and $0.5V_{ref}$ are added to the stage in order to perform dual-mode utilization of the MDAC. In the normal of operation of the ADC, the ADC works based on the Fig. 3(a). When stage input locates in one of the regions *i* and *ii* of Fig. 3(a), a calibration cycle starts to work. The proposed calibration technique uses the difference of the dual mode utilization of Fig. 3(a) and Fig. 3(b) of the MDAC in region *i* and *ii* to estimate coefficients in (1). In the calibration mode, ADC digitize the input based on the Fig. 3(b). An interpolator is used to produce the output of the ADC based on the Fig. 3(a). Two extra comparators are added to the MDAC in order to determine that input locates in region *i* and *ii* or not.

In order to introduce the calibration process, the Fig. 4 is depicted. In every N samples, after pipelined ADC converts *L* samples, extra comparators are turned off during this conversion, extra comparators are turned on. *L* defines the tap number of interpolation filter. *L* samples are stored in registers to be used in interpolation filter. Then the output bits of these comparators are compared to their counterparts and if they are equal, the calibration process will be started. However, they may not be equal to each other and our algorithm waits till next sample to see whether the input place between two decision levels or not. Consider that if mentioned conditioned does not happen, the *L* registers are updated to be utilized in interpolation filter. Our algorithm waits till the output bits of extra comparators and their counterparts are the same and *L* samples are refreshed every cycle to be used in interpolation filter. If the output bits are the same, the DAC will generate analog voltage based on the bits of two extra comparators i.e. zero voltage. In other words, the ADC generate the output based on the Fig. 3(b) and the interpolation generate the output based on Fig. 3(a). After the mentioned sample happened, the ADC return to its normal operation. Furthermore, the interpolation filter starts to identify the ADC's output based on the decision points of two main comparators

When a sample happens in the calibration region, the L-tap interpolator and the ADC dual mode utilization of MDAC. Then the subtraction of interpolator output and the ADC output drives a LMS machine to estimated coefficients in (1) according to equations (8) and (9).

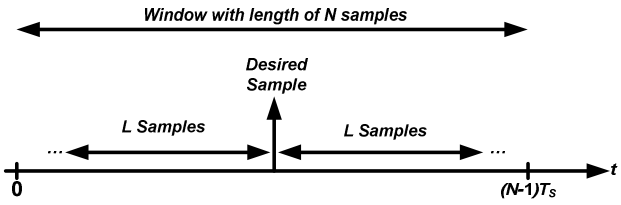

Figure 3. Timing of the proposed calibration method

The calibration will be ended when the ADC and the interpolator produce same outputs since, in ideal case, the redundancy in the 1.5-bit stages removes the effect of shifted decision points. The interpolator limits the input bandwidth of the ADC. To alleviate this problem, the number of interpolation tap should be considered as large as possible.

IV. Simulation Results

The proposed calibration method is tested on a two-stage 12-bit pipelined ADC. For simplicity, only the first stage contains analog imperfections and an ideal 11-bit backend converts the residue voltage of first stage. The gain error, α_1, is set to 1.82 and the nonlinear coefficient, α_3, is set to -0.05. These parameters are chosen such that the design of MDAC amplifier is easy and require negligible power consumption. The offsets of comparators significantly influence parameters in presented simulations. They should be less than $V_{ref}/16$ to be sure that the regions *i* and *ii* can be differed from each other [3]. The number of interpolation tap, L, is set to 64 and N is set to 512. This is because of the number of registers, and memory which store interpolation coefficients are increased as the interpolation tap is increased. Simulation results shows that presented algorithm works properly when the bandwidth of input signal is less than $0.4f_s$. As illustrated in Fig. 5, the SNDR converges after 3×10^5 clock conversions at input frequency of 23.37 MHz which means presented calibration take 3 ms to converge at the clock rate of 100 MS/s. As depicted in Fig. 5 the SFDR and SNDR are enhanced from 40 dB and 35.5 dB to 87dB and 73 dB.

V. Conclusion

In this paper, a new digital background calibration is presented. This calibration uses interpolation filter to determine extra transfer function for the ADC to generate error voltage. Presented algorithm is able to determine gain error and nonlinearity of amplifier. The only overheads of presented technique are two extra comparators and some digital circuits which consume negligible power. Presented algorithm promote ENOB from 5. 6 bits to 11.8 bits.

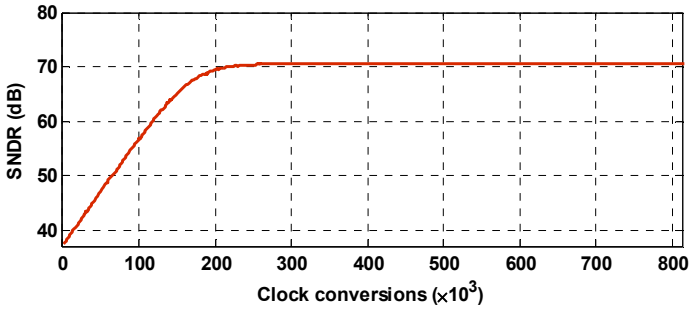

Figure 5. Convergence of SNDR

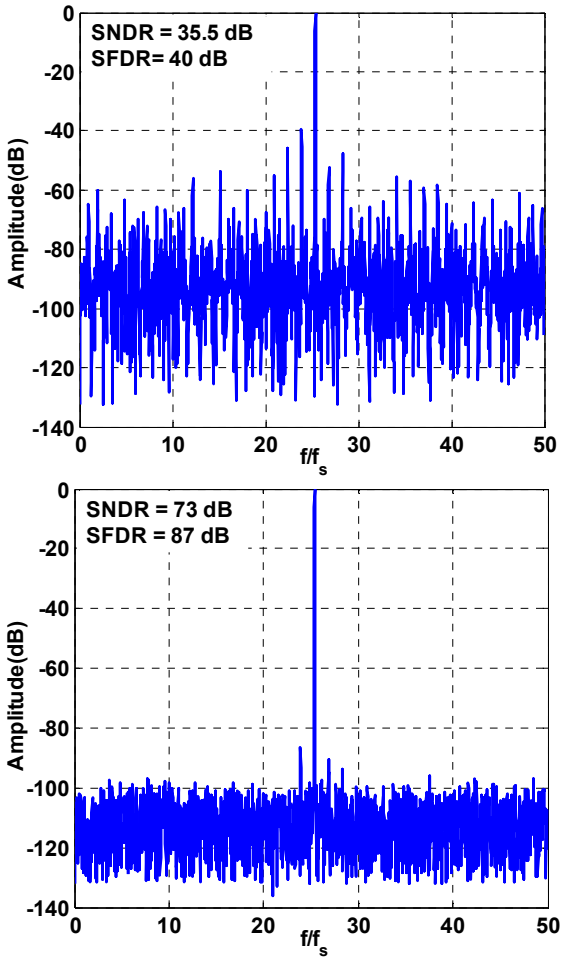

Figure 3. PSD of ADC' output after and before calibration

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