TOPOLOGY SELECTION FOR LOW-VOLTAGE LOW-POWER WIRELESS RECEIVERS

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ABSTRACT

In this paper a study on different architectures of IF receivers is presented. Existing architectures are compared to suggest the most suitable one for low-voltage low-power wireless applications. Due to limitation of portable equipments, e.g. limited battery life, the main focus lies on the power consumption and integration capability. To have a more practical comparison, the feasibility of removing unnecessary blocks as well as integrating external blocks and components are investigated.

1. INTRODUCTION

The role and infrastructure of wireless communication have grown dramatically since the initial deployment of the cellular mobile telephone in 1980s[1]. As the functions of wireless communication are increasing and new demands are emerging, there are more considerations about power dissipation, reliability problems, and cost. Particular engineering attention is directed toward reducing power dissipation and ensuring flexibility in wireless architectures. By increasing the level of integration in the signal path, a receiver can be realized in a more compact form at reduced cost and with greater reliability. In addition higher levels of integration reduce the need for the constituent analog and mixed-signal circuit blocks to drive large pad and package parasitic capacitances, thereby conserving power. Aggressive utilization of VLSI technology also enables the combined integration of a bandpass or baseband analog-to-digital converter (ADC) along with the traditional front-end receiver building blocks. In this manner, the back-end signal processing can be shifted from analog domain into digital domain. By doing this, we eliminate the need for some analog signal processing circuits which can have limited performance due to component mismatch. DSP is not limited by that, since digital hardware can achieve perfect matching between components [2].
First, in section 2, an overview on different topologies of IF receiver is performed. The proposed topologies are compared on the basis of integration feasibility and power consumption. Then, in section 3 possible architectures for analog-to-digital converters are investigated to find out the most appropriate one to be used in a low-power IF receiver or generally for wireless applications. Finally, section 4 presents a conclusion.

2. IF RECEIVER TOPOLOGIES

There are several well known topologies for wireless receivers that are classified on the basis of their way of conversion from RF to baseband. Figure 1 shows a typical wireless receiver. It contains several blocks after antenna.

The first block is the band select filter. This filter should be a selective filter prior to LNA to avoid out of band signals of being amplified. It is typically a high Q bandpass filter; therefore, it should be implemented off-chip. Following that, there is a variable gain amplifier (VGA). VGA or automatic gain control (AGC) helps to achieve a high dynamic range (DR) and relaxes the subsequent blocks like ADC. But it adds noise to signal due to VGA's noise figure and consumes a considerable amount of power. So, to obtain the required DR for wireless applications excess power should be consumed. The next block is the Image Reject (IR) filter. Image rejection is necessary prior to down conversion (mixing) to eliminate image signal from signal band. In general, radio designers must reject image interferes by as much as 80-100 dB[4].
To obtain this amount of image rejection, surely off-chip IR filters are required. However, the drawback of implementing off-chip components, apart from the cost increase, is the increased power consumption. These blocks have to be driven with characteristic impedance, typically 50Ω. Driving signal at or near RF frequencies with such impedance requires power hungry driver blocks [3].

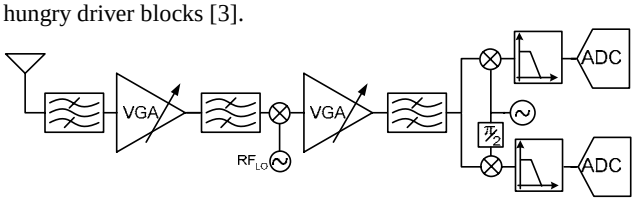

Figure 1. Typical wireless receiver.

2.1. Heterodyne receiver

It is the most well known and most widely used receiver architecture. In this architecture, the RF signal is first down converted into an intermediate frequency (IF) and then, after amplifying and filtering, it will be down converted to baseband. In the baseband, due to bandwidth and required resolution of the signal, Nyquist rate ADCs or oversampling ADCs may be used. In this topology there are substantial trade-offs in choosing IF frequency. The bigger the IF, the more relaxed IR filters are needed. However amplification should be performed at a higher frequency. Sometimes, to overcome some of these problems, multi IF heterodyne receivers are used. However, the implementation of an increasing number of cascaded down conversion stages is generally reflected in the overall power consumption. In this architecture high Q filters are needed which cannot be implemented on-chip. Although there are good reports of high-speed integrated IF filters such as one in[5]; however, they cannot provide enough image rejection and selectivity for wireless communications with reasonable power consumption. Therefore these IF (IR) filters are implemented off-chip and consequently these off-chip components add more power consumption with them. As a result the heterodyne architecture is not suitable for a low-power monolithic receiver.

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Figure 2 shows a typical heterodyne receiver. In this figure only one down conversion stage is depicted. Other down conversion stages can also be existent on the signal path represented by dashed line. Each stage needs a selective filter for image rejection.

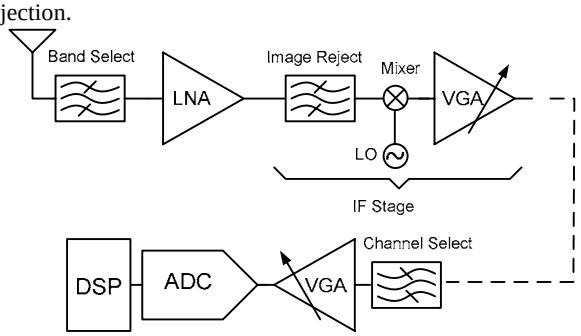


Figure 2. Heterodyne receiver.

The power spectral densities (PSD) of the signals at the input and output of the single-path mixer are depicted in figure 3. In this kind of mixer, input signals are multiplied by $Cos[2\pi(f_{LO}-f_{IF})t]$. This leads to down conversion of image as well as the desired signal[6]. However, if one multiplies the input by $e^{j2\pi(f_{LO}-f_{IF})t}$ instead of $Cos[2\pi(f_{LO}-f_{IF})t]$ the image will be moved out of band of interest[7], as shown in figures 4 and 6. This simply shows the importance of two-path mixing [6] that results in rejection of image without need of a selective off-chip filter. In this case an on-chip filter will provide adequate rejection and power, area, and cost will be saved indeed.

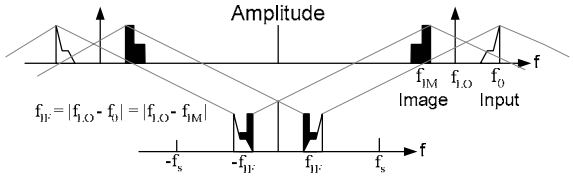


Figure 3. Down conversion in a single-path IF receiver.

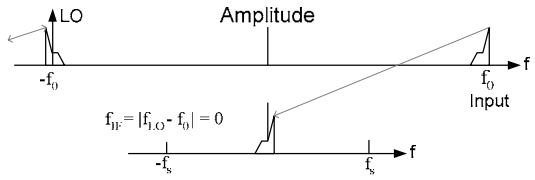


Figure 4. Down conversion in a two-path Zero-IF receiver. (Image Reject mixing).

2.2. Homodyne receiver

In this topology, RF signal is directly converted to baseband. So, no image signal will be shifted into the signal band. But if one uses a single cosine to down convert the RF signal, the signal may alias to itself when SSB scheme modulations are used (which are generally the case). Therefore, a two-path mixer should be used in this architecture. Typical two-path homodyne architecture is shown in figure 5. This topology is sensitive to DC offset and 1/f noise. However, as shown in[8], for wide band signals there is no other way except using this architecture. In this case, one can estimate the DC offset in the DSP. Using this estimate, DC compensation paths can be established to suppress DC offset[8]. Another drawback of this architecture is using two ADCs which accounts for a great amount of power dissipation. Further more, there is a substantial problem with this topology and any other two-path topology. Any imbalances between the two paths, such as component mismatch or gain/phase error in the mixer means that there is a differential error between the two paths. Consequently, signal or noise in the image band will alias into the band of interest. For example, with 2 degrees phase imbalance, the image rejection is only about 35 dB. In order to build a receiver that has image rejection more than 50 dB, the gain imbalance between two paths has to be less than 0.6% and the phase imbalance can not exceed 0.4 degrees[9]. Achieving such requirements seems to be impossible in analog domain.

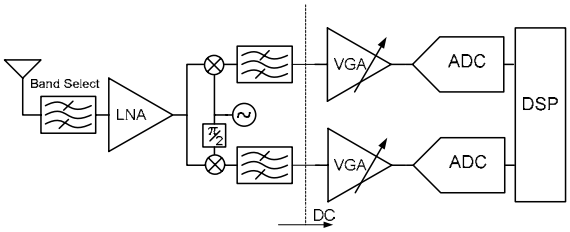


Figure 5. Homodyne (zero IF) receiver.

2.3. Low-IF receivers

This topology is very similar to Homodyne receiver. But here a non-zero IF frequency is used to avoid DC offset and 1/f noise. Therefore there is no need for additional circuits for DC offset and 1/f noise cancellation.

In this low-IF topology, slight image canceling in conjunction with some sort of image cancellation that can be implemented by adding a single zero in some form of complex ADC implementation [6] is sufficient. This is more discussed in section 3.2. Consequently, there is no need for power hungry external image rejection filters. On the other hand, this topology can take advantage of two-path mixing which rejects the image. However, there is still a big concern about imbalances between mixing signals. This situation is more serious here because the frequency responses are asymmetric. Figure 6 depicts the PSD of the input signal in a two-path low-IF receiver prior and after mixing.

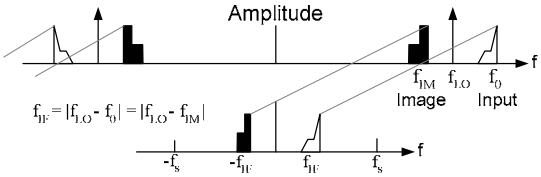


Figure 6. Down conversion in a two-path Low-IF receiver. (Image-reject mixing)

In this topology a slight image filtering prior to mixing may be helpful which can be achieved by means of a simple on-chip filter. On the other hand, the desired signal is located in an IF frequency. Therefore digitization can be performed in the IF frequency and one can take advantage of complex bandpass delta-sigma modulators as opposed to using traditional ADC structures in which two ADCs are required that dissipate more power. In this topology, IF to baseband conversion is performed in digital domain after digitizing the IF signal. Therefore, this could be done perfectly matched in a DSP. On the other hand, moving most of functions to digital domain means that the receiver can be implemented much more compact than ever. Here off-chip power hungry IR filters and intermediate stages, including mixer, off-chip filters, and VGA, all are eliminated

meaning that this topology is optimized for integration as well as low-power operation.
In all kinds of receivers that discussed, demodulation is performed in digital domain. In low IF receiver, further signal processing tasks, including image rejection, channel selection [1], decimation [13], down conversion to baseband [6], and even equalization and mismatch cancellation [4] are shifted to digital domain. Figure 7 shows a typical digital back-end of a low IF receiver.
Low IF receivers are best suited for narrowband signals, such as GSM. However, it can be adapted to multi-standard IF receivers due to its flexibility in programming and since demodulation and down conversion are carried out in digital domain.

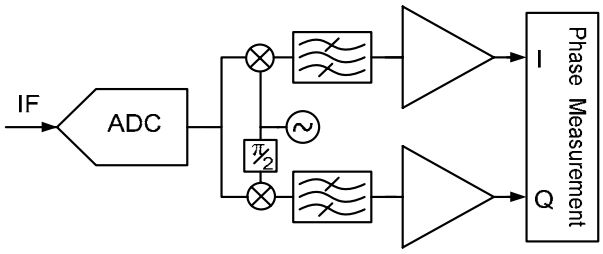


Figure 7. Demodulation of a digital phase modulation scheme in DSP.

It is important to note that several methods have been invented to cancel the imbalance (gain/phase mismatch) between two paths in two-path receivers (mixers) in both analog [10] and digital[4],[9] domain with reasonable power consumption. Therefore there is no concern for image rejection in two-path topologies (e.g. Low-IF receivers) and it can be performed almost perfectly.

2.4. Low-IF vs. Zero-IF

The advantages of a low-IF receiver compared to a zero-IF receiver mostly concern with DC offset problems since the desired signal is not located around DC. This also includes the problem of local oscillator (LO) leakage. LO leakage causes the product of LO multiplied with itself which is suited around resulting in a DC and low-frequency signal with a very small bandwidth (less than 1kHz) [8]. It is clear that the low-IF topology is free from all these phenomena. However, the disadvantage of low-IF receivers is that the suppression of image must be higher in comparison with zero-IF receivers. In this case, the image can be 30dB higher than desired signal. Here, proper choice of IF is too important which can place the image signal between two transmission channels. When using low-IF topology with limited filtering (only anti-aliasing) high specs of analog parts are shifted to ADC [8]. Fortunately such ADCs are realizable at the moment[11].

3. ADC SELECTION

In the case of using zero-IF, depending on the channel bandwidth, we can use either Nyquist rate or oversampling Analog-to-Digital converters (ADC). It is evident that for audio and narrowband signals (e.g. GSM signals), high resolution can be achieved with consuming lower power if we use oversampling ADCs. On the other hand, using oversampling ADCs means much more relaxed requirements for Anti-Aliasing (AA) filters. In low-IF receivers, due to limited band of interest, the best candidate is bandpass delta-sigma. Nyquist rate ADCs that cover the entire band from DC to IF are not needed. Although baseband ADCs consume less power in comparison to bandpass ADCs due to their much more relaxed Op-Amp considerations; however, it should be noted that in zero-IF receivers, several filtering prior to digitization are needed due to the down conversion to baseband and it can increase the overall power consumption of zero-IF receivers. Therefore low-IF topology with bandpass delta-sigma ADC can yield in overall lower power dissipation since there is no need for extra IF (IR) filters.
There is still a problem with choosing bandpass delta-sigma ADC architecture. Several architectures exist each having its own trade-offs between analog and digital parts. This will be discussed in the next sections.

3.1. Conventional fs/4 architecture

In this architecture digital IF frequency is located at fs/4 where f_s is the sampling frequency. Due to real transfer function of this architecture, symmetrical (conjugate) placement of poles and zeros in the Signal Transfer Function (STF) and Noise Transfer Function (NTF) is required which means consuming more power than necessary. Here for realizing unnecessary poles and zeros, e.g. complex conjugate ones, extra active devices, Op-Amp, must be used. It means a great amount of power dissipation. However, it has the advantages of easy digital demodulation. To convert the digitized signal into baseband, it must be multiplied by $e^{j\omega_0 t}$ where $\omega_0 = 2\pi f_s / 4$. This means that it is only enough to multiply the digitized signal by ± 1 which makes the hardware requirement even more relaxed.
However, a major drawback of using conventional bandpass delta-sigma modulator is that two ADCs must be used, one for each path, and this of course means more power consumption.

3.2. Quadrature (Complex) architecture

In this architecture, STF and NTF poles and zeros are not placed symmetrically (complex-conjugate form). In real bandpass modulators, poles and zeros are placed in complex conjugate form while only the poles and zeros in the signal band are required and their conjugate are not needed. On the other hand, implantation of each pole/zero requires one Op-Amp (active element) in switched-capacitor (SC) circuits requiring a significant amount of power. So, implementing complex-conjugate poles means paying power penalty. Hence, by making complex STF's and NTF's [12], some power can be saved while it is in trade-off with complexity of digital portion. Outputs of two-path mixers (I, in-phase & Q, Quadrature-phase) can be directly fed into the complex bandpass delta-sigma modulator (After anti-aliasing filtering, if needed). It is well shown in figure 10. So, in comparison with real bandpass delta-sigma modulators, in complex bandpass delta-sigma modulators just one ADC is needed when using complex bandpass delta-sigma modulators resulting in more power saving besides the other advantages of complex bandpass delta-sigma modulators. Figure 8 depicts typical pole/zero placement schemes for real and complex modulators. As can be seen in figure 8, one or more of NTF zeros can be implemented in the image band. This will help the suppression of image in complex bandpass modulators when a mismatch exists between the I and Q paths.

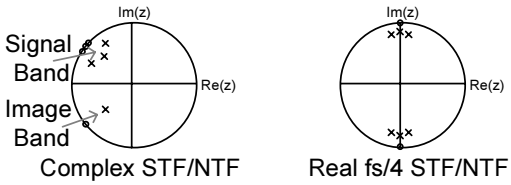
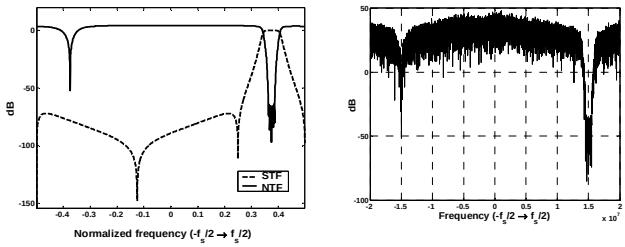


Figure 8. Complex and Real modulators.

Figure 9 shows the transfer function of complex bandpass delta-sigma in which an image-band zero is implemented in NTF.



(a) (b)

Figure 9. Transfer function of a complex bandpass delta-sigma (a) NTF & STF, (b) Output spectrum of modulator.

3.3. Continuous-time quadrature architecture

A typical delta-sigma modulator can be built employing a continuous-time (CT) filter inside the modulator loop [14],[15]. It can be shown that anti-aliasing is an inherent property of CT delta-sigma modulators. Therefore, if a quadrature CT bandpass delta-sigma modulator is used instead of a switched-capacitor implementation, anti-aliasing (AA) filter can be removed [15]. Hence more power can be saved. On the other hand, if f_T is the maximum transistor speed in a process, SC modulators are limited to maximum clock rate which is in the order of $f_T/100$ while CT modulators could be clocked up to an order of magnitude faster in the same technology [15]. Higher IF means relaxed specification of IR filter. In other words, in CT modulators the restriction on Op-Amp bandwidth and slew-rate (if any op-amp are even used) are more relaxed since waveforms vary continuously and signal frequency can be up to unity-gain bandwidth of op-amp. Therefore CT designs generally consume less power than SC designs. Figure 10 depicts and compares both types of receivers.

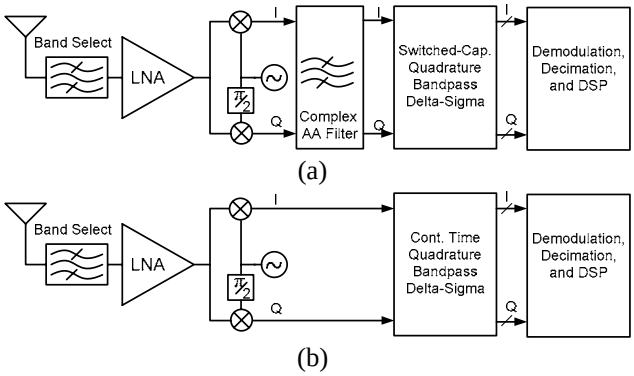


Figure 10. Wireless receiver using (a) SC Quadrature delta-sigma modulator, (b) CT Quadrature delta-sigma modulator.

4. CONCLUSION

In this paper several architectures for wireless receivers are investigated and the best topology with emphasis on low-power operation and integration feasibility is opted. Although there are several open issues and a fair comparison among different architectures needs more extensive research, in this paper it is suggested that the low-IF topology with continuous time quadrature bandpass delta-sigma modulator may have the best performances. It has more digital and less analog parts than conventional topologies. In this combined architectures, several tasks are shifted to digital domain.

5. ACKNOWLEDGEMENT

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