Minimum Detectable Capacitance in Capacitive Readout Circuits

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Abstract— In this paper, accurate equations are presented to calculate the capacitance resolution in the readout circuits exploiting different techniques to reduce the circuit low-frequency noise. The circuit parameters and trade-offs affecting the capacitance resolution are comprehensively involved in these equations. Transistor level simulations are performed with a 0.18 µm CMOS technology using Spectre RF to verify the obtained equations. The results of comparing two utilized common techniques, so called correlated double sampling (CDS) and chopper stabilization (CHS), reveal that employing the combination of these techniques results in the minimum resolution variation as the input parasitic capacitance is changed.

I. INTRODUCTION

Noise reduction is an important requirement in the capacitive sensor interfaces to improve the sensor resolution. In this approach, the correlated double sampling (CDS) and chopper stabilization (CHS) techniques are widely used in switched-capacitor (SC) capacitive readout circuits to reduce the op-amp offset and low-frequency noise [1-3]. These methods considerably remove the 1/f noise while the power spectral density (PSD) of the output noise increases significantly due to the aliasing of the wideband circuit noise which is inherent to the sampling process. Therefore, considering the aliasing effect is crucial in finding the accurate resolution equations for capacitive readout circuits. Among the relevant literature, only one study has been reported, to the best of our knowledge, concerning the calculation of the resolution for different readout configurations [4]. However, the equations presented in this study are rather rough and imprecise, because the foldover components of white noise dominated in SC circuits are not taken into consideration in this analysis.

This paper presents accurate equations to determine the minimum detectable capacitance by considering the aliasing of the amplifier thermal noise. These analytical equations are described in Sect. II for three different low-frequency noise reduction techniques commonly used in sensor interfaces. In Sect. III, the transistor level simulations are performed in a 0.18 µm CMOS technology using Spectre RF to verify the obtained equations. The results of analytical equations are shown in this section to be in close agreement with the simulation results. Furthermore, the resolution of different noise reduction techniques is compared in this section. Finally, conclusions are presented in Sect. IV.

II. ANALYTICAL EXPRESSIONS

A simplified schematic diagram of a SC capacitive readout circuit is shown in Fig. 1. The circuit detects the capacitance change (ΔC_s) in two non-overlapping clock phases, Φ_1 and Φ_2. In the sampling phase, Φ_1 = high and Φ_2 = low, the sense capacitors, C_S and C_R, are charged up with $0.5V_{DD}$ and the amplification capacitor, C_A, is discharged to zero. In the amplification phase, Φ_1 = low, Φ_2 = high, the charges stored in the sense capacitors are transferred to C_A. The minimum detectable capacitance change (ΔC_s) is limited by the noise sensitivity of the circuit. In order to reduce the low-frequency noise of the operational transconductance amplifier (OTA) three common techniques are used in the capacitive readout circuits as illustrated in Fig. 2.

In CDS scheme as shown in Fig. 2(a), the CDS capacitors (C_{CDS}) accumulate the amplifier offset and 1/f noise on Φ_1 in order to subtract it from a new sample of the amplifier noise in the amplification phase [1]. Fig. 2(b) shows another low frequency noise reduction technique called CHS [2]. In this topology, the low frequency noise is transposed to the high frequencies by modulation with a square wave. To further reduce the amplifier noise and circuit mismatch, other interface circuits are applied using both CHS and CDS schemes as shown in Fig. 2(c) [3].

Using KCL at isolated nodes V_{i1} and V_{i2} in Fig. 2, the differential output voltage (ΔV_o) is calculated as the following [1]:

$$\Delta V_o = \frac{\Delta C_s}{C_A} V_{DD} . \quad (1)$$

Equation (1) is used to calculate the minimum detectable capacitance (resolution) from the output noise voltage [4] as:

$$\Delta C_{\min} = \frac{C_A \cdot V_{noise}}{V_{DD}} . \quad (2)$$

where V_{noise} is the root mean square (RMS) value of the output noise power obtained by integrating the output PSD of the circuits from dc to infinite frequency.

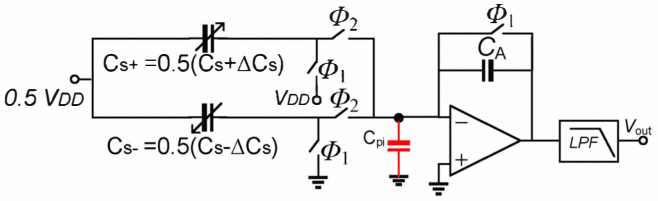

Figure 1: Simplified schematic diagram of a SC capacitive readout circuit [1].

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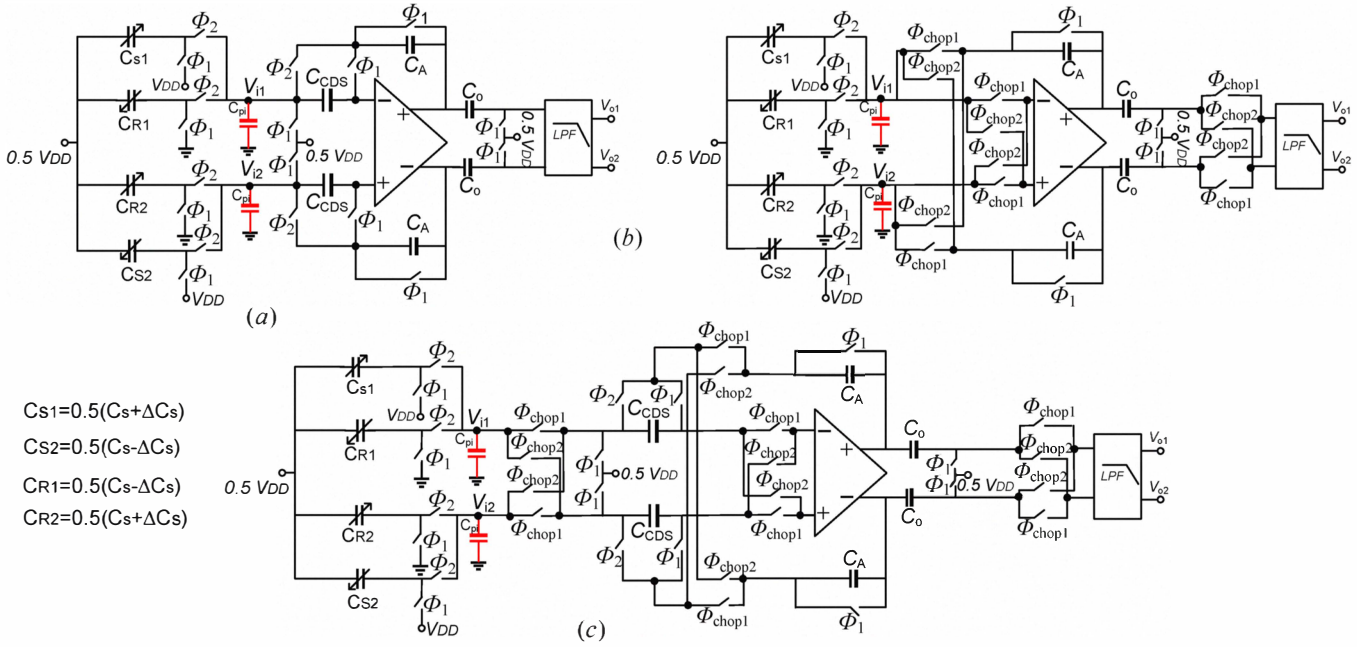

Figure 2: Fully differential capacitive readout circuits using different low frequency noise reduction techniques. (a) CDS [1], (b) CHS [2], and (c) combination of CHS & CDS techniques.

In the following, the output PSD and corresponding resolution equations are calculated separately for the circuits using the three noise reduction techniques shown in Fig. 2.

A. CDS Technique

According to Pimbley et al. [5], the output PSD of the CDS circuit is equal to:

$$S_{out}(f) = 4\cdot\left(\frac{\sin(\pi f T_s)}{\pi f T_s}\right)^2 \times\sum_{n=-\infty}^{n=\infty}\frac{S_{in}(f-n/T_s)}{\beta^2}\left(\sin\left(\frac{\pi T_s(f-n/T_s)}{2}\right)\right)^2. \quad (3)$$

where T_s is the sampling period, β is the feedback factor of the amplifier, and $S_{in}(f)$ is the input-referred PSD of the amplifier noise. Equation (3) shows that the input spectrum is multiplied by $sin^2(\pi T_s f/2)$; therefore the 1/f noise is removed considerably. But, due to the sampling process, the output noise is dominated by the white noise folding which is described by an infinite summation in (3). The exact PSD expression by considering the effect of the circuit noise aliasing can be obtained by using the following identity to calculate the summation of the infinite series in (3).

$$\sum_{n=-\infty}^{n=\infty}\frac{e^{in\alpha}}{(n-\chi)^2+\gamma^2}=\frac{\pi}{\gamma} \times\frac{e^{i\chi(\alpha-2\pi)}\sinh(\gamma\alpha)+e^{i\chi\alpha}\sinh(\gamma(2\pi-\alpha))}{\cosh(2\pi\gamma)-\cos(2\pi\chi)}. \quad (4)$$

Since the amplifier 1/*f* noise is significantly reduced, $S_{in}(f)$ can be considered as a first order low-pass filtered white noise, which is given by (5) [5].

$$S_{in}(f)=\frac{S_{no}}{1+(f/f_c)^2}. \quad (5)$$

where S_{no} represents the white noise component of the OTA, and $2\pi f_c$ is the amplifier closed-loop bandwidth. Replacing (5) in (3) and then using (4), the output noise PSD is calculated as the following:

$$S_{out}(f)=\frac{2\pi f_c T_s S_{no}}{\beta^2}\cdot\left(\frac{\sin(\pi f T_s)}{\pi f T_s}\right)^2 \times\frac{\sinh(\pi f_c T_s)\left[\cosh(\pi f_c T_s)-\cos^2(\pi f T_s)\right]}{\sinh^2(\pi f_c T_s)+\sin^2(\pi f T_s)}. \quad (6)$$

The sampled switch noise (kT/C) is another major noise source in SC circuits which is dominated by amplification capacitor (C_A) in Fig. 2. Using C_o at the output of the first stage cancels the kT/C_A noise. This capacitor samples the switch noise and then subtracts it from the amplifier output [6-7].

Multiplying the PSD in (6) by a low-pass filter with the bandwidth equal to the capacitance detection bandwidth (BW) of the sensor and integrating the result over the entire frequency, the power of the output noise is obtained. Substituting the RMS voltage value of the output noise in (2), the minimum detectable capacitance for CDS interface circuit is calculated as follows:

$$\Delta C_{\min}=\frac{C_A}{V_{dd}}\frac{1}{\beta}\sqrt{BW} \times\sqrt{2\pi f_c T_s S_{no}\left(\frac{\cosh(\pi f_c T_s)-1}{\sinh(\pi f_c T_s)}\right)}. \quad (7)$$

B. CHS Technique

In this technique, the amplifier output noise is modulated by a square-wave signal with the period of $T_{chop}=1/f_{chop}$. So, the output noise PSD can be expressed as:

$$S_{out}(f)=\left(\frac{2}{\pi}\right)^2\sum_{\substack{n=-\infty\\ n\neq 0\\ n\ odd}}^{n=\infty}\frac{1}{n^2}\frac{S_{no}}{\left(1+\frac{\left(f-n\cdot f_{chop}\right)^2}{f_c^2}\right)\beta^2}. \quad (8)$$

where f_{chop} is the chopping frequency. By following the procedures explained in part A, the resolution equation is approximated as:

$$\Delta C_{\min}=\frac{C_A}{V_{dd}}\frac{1}{\beta}\sqrt{S_{no}BW\left(1-\frac{2}{\pi}\frac{f_{chop}}{f_c}\tanh\left(\frac{\pi f_c}{2f_{chop}}\right)\right)}. \quad (9)$$

C. Combination of CHS & CDS Techniques

The proposed model illustrated in Fig. 3 describes the noise reduction principle in combination of CHS & CDS techniques. Firstly the amplifier input-referred noise is modulated with period of $T_{chop}=1/f_{chop}$, and then it is sampled by the period of $T_s=1/f_s$ on CDS capacitors. Hence, the output noise PSD of the amplifier can be expressed as the following:

$$S_{out}(f)=4\cdot\left(\frac{\sin(\pi fT_s)}{\pi fT_s}\right)^2 \times\sum_{n=-\infty}^{n=\infty}\left(\frac{4}{\pi^2}\sum_{\substack{k=-\infty\\ k\neq 0\\ k\ odd}}^{k=\infty}\frac{1}{k^2}\frac{S_{no}}{\left(1+\frac{\left(f-k\cdot f_{chop}-n/T_s\right)^2}{f_c^2}\right)\beta^2}\right)\left(\sin\left(\frac{\pi T_s\left(f-n/T_s\right)}{2}\right)\right)^2. \quad (10)$$

The first and second infinite series in (10) account for the sampling process and the chopping technique, respectively. After some calculations explained in part A, the resolution equation for the circuit using the combination of CHS & CDS techniques is calculated as follows:

$$\Delta C_{\min}=\frac{C_A}{V_{dd}}\frac{1}{\beta}\sqrt{\frac{8f_cT_sS_{no}}{\pi}} \times sqrt\left[\left(\frac{BW\left(\cosh(\pi f_cT_s)-\cos(\pi f_{chop}T_s)\right)}{\sinh(\pi f_cT_s)}\right)-\left(\frac{1}{2\pi BT_s}\times\frac{\sin^2(\pi BWT_s)\sin(\pi f_{chop}T_s)\sinh(\pi f_cT_s)}{\sinh^2(\pi f_cT_s)+\sin^2(\pi f_{chop}T_s)}\right)\right]. \quad (11)$$

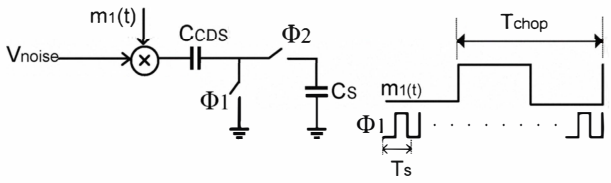

Figure 3: Proposed model for noise reduction principle in combination of CHS & CDS techniques.

III. Comparision & Simulation

The Analytical expressions in equations (7), (9), and (11) comprehensively describe the trade-off between the minimum detectable capacitance and circuit parameters such as T_s, f_{chop}, and f_c. One of the important challenges in the capacitive readout circuits is their susceptibility to the parasitic capacitances (C_{pi}) between the sensors and their interface circuits, which affect the amplifier cut-off frequency by the following relation:

$$f_c=\frac{C_A}{C_s+C_{pi}+C_A}f_{GBW}. \quad (12)$$

where $2\pi f_{GBW}$ is the unity gain bandwidth of the amplifier. By substituting (12) in resolution equations, (7), (9), and (11), the effect of the parasitics variations on the minimum detectable capacitance can be found. The results for CDS, CHS and the combination of CHS & CDS techniques are plotted in Figs. 4-6, respectively. To verify these equations, the transistor-level simulations of the interface circuits shown in Fig. 2, are performed in Spectre RF using the periodic steady state (PSS) and periodic noise (PNOISE) analyses with a 0.18µm CMOS technology. The time varying capacitances (representing the sense capacitors) are modeled using Verilog-A [8]. The circuit level simulation results for different values of C_{pi} are also plotted in Figures 4-6. As illustrated, the presented analytical expressions are in good agreement with the simulation results.

The interface circuit parameters such as the sampling frequency, f_s, bandwidth of the low-pass filter (BW), sense capacitors, and amplification capacitors are equal to 500 kHz, 1.5 kHz, 10 pF and 1 pF, respectively similar to [1]. The amplifier used in front-stage of the circuits is a fully-differential folded-cascode OTA with 70 dB DC gain and 5 MHz unity gain bandwidth. Using the folded-cascode amplifier topology, the equivalent input noise of the OTA, S_{no}, can be expressed as (13) in the analytical expressions [3]:

$$S_{no}=\frac{16k_BT}{3g_{m,in}}\times\lambda. \quad (13)$$

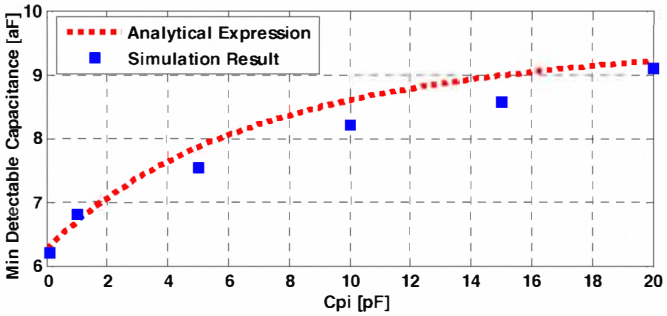

Figure 4: Resolution for CDS interface circuits as the input parasitic capacitance is changed.

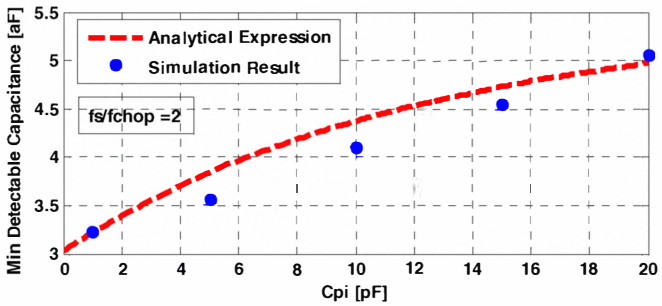

Figure 5: Minimum detectable capacitance for interface circuits using CHS technique versus the input parasitic capacitance.

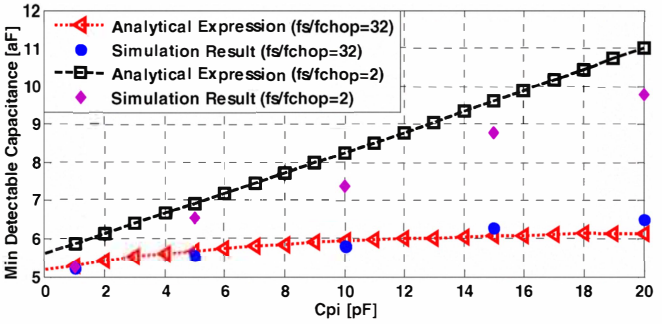

Figure 6: Capacitance resolution for capacitive readout circuits using combination of CHS & CDS techniques as the parasitics change.

In (13), k_B is the Boltzmann's constant, T is the temperature in Kelvin, and $g_{m,in}$ is the transconductance of the amplifier input transistors which are the major noise sources of the folded cascade OTA [3]. Also the factor λ in (13) accounts for the noise contribution of the output current source transistors.

The ratio of the sampling frequency over the chopping frequency, f_s/f_{chop}, is another important parameter in the capacitive readout circuits. For both simulation and analysis of the chopper-stabilized circuit which the results are shown in Fig. 5, this ratio is assumed to be 2 as reported in [2]. For the combination of CHS and CDS techniques the results for two values of f_s/f_{chop} = 2 and 32, are plotted in Fig. 6. As is seen, for larger ratios of f_s/f_{chop}, there is much more agreement between the simulation results and the presented analytical expression.

Figure 7 shows the capacitance resolution versus C_{pi} for the circuit using the combination of CHS and CDS techniques for various ratios of f_s/f_{chop}. The resolution variation is

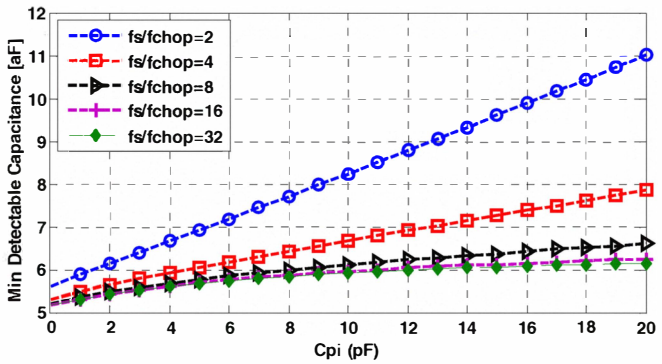

Figure 7: Resolution for capacitive readout circuits using both CHS & CDS techniques for various ratios of f_s/f_{chop} as input parasitics change.

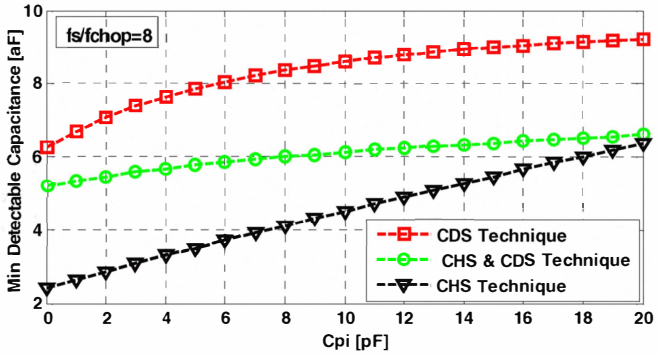

Figure 8: Comparison between the capacitance resolution of the three noise reduction techniques versus the input parasitic capacitance.

approximately constant when $f_s/f_{chop} \geq 8$, and has its maximum value for f_s/f_{chop}=2; so, this ratio is not recommended in the design of the capacitive readout circuits. The comparison between the resolution expressions of the three noise reduction techniques for f_s/f_{chop}=8 versus the input parasitic capacitance is shown in Fig. 8. The resolution improves for CHS technique, while the resolution changes for the combination of CHS and CDS methods has the smallest value among other topologies.

IV. Conclusions

In this paper accurate expressions for the capacitance resolution in capacitive readout circuits using three different noise reduction techniques have been presented. In the obtained equations the aliasing of the amplifier thermal noise which is dominant in the SC circuits is carefully considered. Simulation results have been performed in a 0.18µm CMOS technology and are in good agreements with the achieved resolution expressions. Comparison of obtained equations has shown that the combination of CHS and CDS techniques in capacitive readout circuits results in the minimum resolution variation as the input parasitic capacitance between the capacitive sensor and its interface circuit is changed.

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