On the Design and Optimization of a Switched-Capacitor Interface Circuit for MEMS Capacitive Sensors

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***Abstract*- In this paper a switched-capacitor (SC) interface circuit that is intended for MEMS capacitive sensors is proposed and designed. In the proposed architecture, both correlated double sampling (CDS) and chopper stabilization (CHS) noise reduction techniques are applied to the interface circuit to reduce the amplifier offset and low frequency noise. The effects of parasitic capacitances between the sensor and its interface circuit which are usually larger than the sense capacitances are carefully analyzed and used to optimize the readout performance. In other words, by analyzing the circuit offset and noise performance in presence of these parasitic capacitances, the suitable values of the circuit parameters such as sampling frequency, chopping frequency, and amplifier unity gain bandwidth are calculated. In comparison to the circuit using only CDS or CHS technique, the resolution variation of the proposed readout circuit is less than 1aF in presence of parasitic capacitances varying up to 20 pF.**

Keywords- Capacitive interface circuit; noise reduction techniques; residual offset analysis; resolution variation; MEMS capacitive sensors.

I. INTRODUCTION

Micro-electro-mechanical system (MEMS) capacitive sensors are recently used in a wide range of application including navigation and guidance, space, automotive, biomedical, and military industry due to their main advantageous of high sensitivity, low power, simple structure and robustness [1-4]. In the capacitive sensors, sense capacitances vary in response to the physical signals such as acceleration (in accelerometers) and angular speed (in gyroscope); the capacitance variations are then detected and amplified by the following readout circuits. Several readout architectures have been proposed for MEMS capacitive sensors such as switched capacitor (SC) circuit [1, 2], continuous-time voltage sensing (CTV) [3], and continuous-time current sensing (CTC) [4]. Among these architectures, the SC circuits are more commonly used because of their primary features including CMOS compatibility, good voltage linearity, good accuracy of time constants, and good temperature characteristics [5].

The sense capacitance changes in the high-precision MEMS capacitive sensors are very small (on the order of few or few tens of atto Farads). Therefore, it is crucial to design a low noise interface circuit to achieve high resolution readout. Correlated double sampling (CDS) and chopper stabilization (CHS) techniques are two commonly used approaches to reduce low frequency noise and offset in the readout circuits [1-6]. Furthermore, one of the key challenges in the capacitive readout circuits is their susceptibility to the parasitic capacitances between the sensor and its interface circuit, which change the minimum detectable capacitance of the circuit as parasitic capacitances change [6]. In many applications which the MEMS sensors and their interface circuits are integrated on separate chips, these parasitic capacitances are typically much larger than the sense capacitances for example as large as 20 pF. Therefore, it is essential to take into consideration the undesirable effects of these parasitics in the design of the interface circuits.

In this paper, a switched capacitor interface circuit which uses both CDS and CHS noise reduction techniques is proposed and designed. Offset and noise performance of the circuit in presence of these parasitics are analyzed in order to optimize the readout circuit performance. In addition, the readout IC performance is compared to the circuit using only one of CDS or CHS methods. In Sect. 2, the circuit description, offset, and noise analyses are presented. The simulation results and comparisons are given in Sect. 3. Finally, Sect. 4 concludes the paper.

II. CIRCUIT DESCRIPTION AND ANALYSIS

The architecture of the proposed interface circuit is shown in Fig. 1. It consists of front-end and back-end blocks followed by the MEMS sensor shown in the shaded area. The circuit reads the capacitance changes of the capacitive sensor and produces a voltage signal proportional to the capacitance variation. A low-noise and low-offset front-end detects and boosts the sense capacitance changes, and a SC low-pass filter (LPF) in the back-end block limits the bandwidth of the front-end output.

The differential MEMS sensor is modeled as two pairs of differential sense capacitances C_{S1}, C_{R1}, C_{S2} and C_{R2}, and two parasitic capacitances, C_{Pi}. The sense capacitors are composed of a fixed component, C_S and a variable portion, ΔC_S, which changes responding to the physical signals. The front-end circuit detects the capacitance variations in two phases, Φ_1 and Φ_2. During the sampling phase, Φ_1, the sense capacitors are charged up with $0.5V_{DD}$ and the amplification capacitors, C_A, are discharged to zero. During the amplification phase, Φ_2, the charges stored in the sense capacitors are transferred to the amplification capacitors. Since the sense capacitors are charged with different polarities, the charges transferred to the

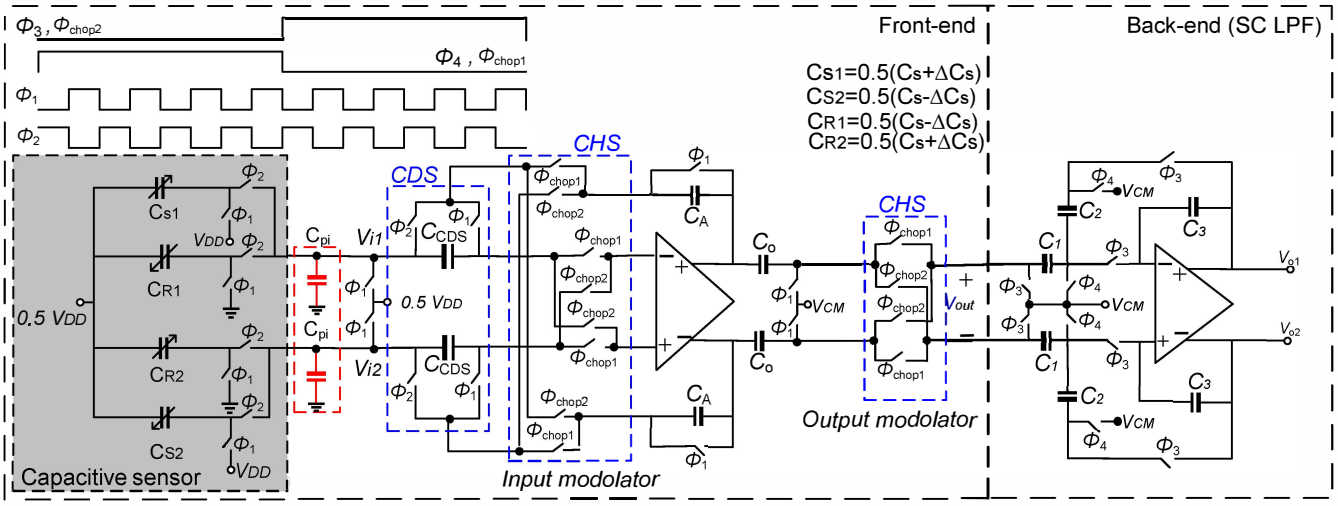

Figure 1. Proposed fully differential capacitive readout circuit using both CDS and CHS noise reduction techniques.

amplification capacitors are proportional to the difference between the sense capacitors. Therefore, by using charge conservation law at isolated nodes, V_{i1} and V_{i2} in Fig. 1, the front-end differential output voltage can be expressed by:

$$V_{out} = V_{DD}\frac{\Delta C_s}{C_A}. \quad (1)$$

Equation (1) shows that the minimum detectable capacitance of the sensor (ΔC_{min}), resolution, is related to the output noise voltage as:

$$\Delta C_{\min} = \frac{C_A \cdot V_{noise}}{V_{DD}}. \quad (2)$$

where V_{noise} is the root mean square (RMS) value of the output noise power. Therefore, noise reduction is an important requirement in the capacitive readout circuits to improve the sensor resolution. In this design, both CDS and CHS techniques are applied to the front-end in order to reduce the low-frequency noise and instant offset of the operational transconductance amplifier (OTA). The input signal is transposed to higher frequencies where there is no flicker noise by the input modulator implemented and chopping clocks, Φ_{chop1} and Φ_{chop2}, and then modulated back to the baseband by output modulator. The amplifier low frequency noise is also modulated by the chopper implemented after CDS capacitors, and then sampled by the period of $T_s=1/f_s$ on the CDS capacitors. The CDS capacitors (C_{CDS}) accumulate the modulated low frequency noise on Φ_1-phase in order to subtract it from a new sample of the amplifier noise on $_2$-phase. The noise reduction principle using the combination of CDS and CHS techniques is illustrated in Fig. 2 [7], where V_n is the OTA input-referred noise.

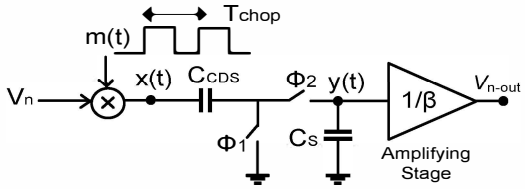

Figure 2. Noise reduction principle of the interface circuit.

A. Noise Analysis

By using procedures explained by the authors in [7], the output noise power, $V^2_{n\text{-}out}$ can be approximated as:

$$V^2_{n\_out} = \frac{8}{\pi}\frac{f_c T_s S_{no} BW}{\beta^2}\frac{\left(\cosh(\pi f_c T_s) - \cos(\pi f_{chop} T_s)\right)}{\sinh(\pi f_c T_s)} \quad (3)$$

where T_s is the sampling period, BW is the bandwidth of the sensor, f_{chop} is the chopping frequency, β is the feedback factor of the amplifier, $2\pi f_c$ is the amplifier closed-loop bandwidth, and S_{no} represents the white noise component of the OTA. By substituting the output noise power, $V_{n\text{-}out}$, in (2), the capacitance resolution is given by:

$$\Delta C_{\min} = \frac{C_A}{V_{dd}}\frac{1}{\beta}\sqrt{\frac{8 f_c T_s S_{no} BW}{\pi}\frac{\left(\cosh(\pi f_c T_s) - \cos(\pi f_{chop} T_s)\right)}{\sinh(\pi f_c T_s)}}. \quad (4)$$

In (4), the amplifier unity gain bandwidth, $\omega_{GBW} = 2\pi f_{GBW}$, is related to f_c and β by equation (5).

$$f_c = \beta f_{GBW} = \frac{C_A}{C_s + C_{pi} + C_A} f_{GBW}. \quad (5)$$

As it is obvious from (5), the parasitic capacitance, C_{pi}, affects the amplifier cut-off frequency; and hence, causes resolution variations as it changes. The resolution equation expressed in (4) is plotted in Fig. 3 for various ratios of f_s/f_{chop}, as the parasitic capacitance varies. The ratio of sampling frequency to the chopping frequency, f_s/f_{chop}, is an important parameter in the interface circuit design. It is illustrated that for $f_s/f_{chop} \geq 8$ the resolution variation is approximately constant, and has its maximum value for $f_s/f_{chop}=2$. Therefore, the ratio of two is not recommended in the circuit design and the ratio of eight is the best option for both reducing the power consumption and minimizing the resolution variations in the presence of large parasitic capacitors. It should be mentioned that another major noise source in SC circuits is the sampled

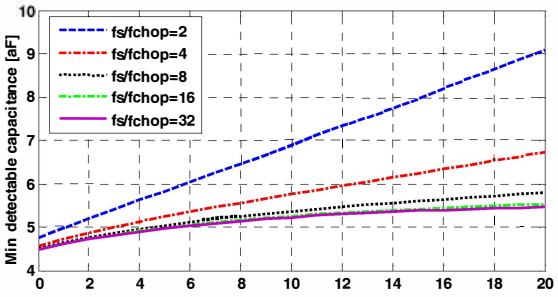

Figure 3. Minimum detectable capacitance expressed in (4) for various ratios of f_s/f_{chop} as C_{pi} changes.

switch noise (kT/C) which is dominated by the amplification capacitor (C_A) in Fig. 1. The kT/C_A noise is canceled by using C_o at the output of the first stage [8]. In fact, this capacitor samples the switch noise and then subtracts it from the amplifier output.

B. Offset Analysis

The clock feed through introduced by the input modulator switches is the dominant source of residual offset in circuits using chopper technique [9]. A certain amount of charge ΔQ is injected on the parasitic capacitances at each switching instant and cause spike signal with peak voltage of $V_{inj}=(\Delta Q)/(C_{pi}+C_{in})$,where C_{in} is the input capacitance of the amplifier. The injected charge will then discharge exponentially to the original value with time constant τ. The signal after demodulator is the product of this spike signal and the demodulation signal. By assuming the output modulator is ideal, the output residual offset is equal to the mean square value of both amplified and demodulated spike signals. The output residual offset is calculated as (6) as it is explained in Appendix. I.

$$V_{off} = \frac{2V_{inj}A_0}{T_{chop}} \cdot \frac{\tau f_c}{1-2\pi\tau f_c} \times \left[2\pi\tau \tanh\left(\frac{T_{chop}}{4\tau}\right) - \frac{1}{f_c}\tanh\left(\frac{\pi f_c T_{chop}}{2}\right) \right]. \quad (6)$$

where A_0 and f_c are the amplifier closed-loop gain and cut-off frequency.

One of the important requirements in SC circuits using chopper technique is choosing the amplifier bandwidth such as to have sufficient gain for the modulated signal while rejecting most of the spikes' spectral components, and also providing proper settling of amplifier. Another important parameter in these circuits is the chopping frequency. As one can understand from (6), although increasing f_{chop} transposes the corner frequency of flicker noise to the higher frequency, but this increases the circuit output residual offset. In order to acquire the proper values of chopping frequency, f_{chop}, and amplifier unity gain-bandwidth, f_{GBW}, the normalized offset contribution expressed in (6) is plotted in Fig. 4 versus $f_{GWB}\times T_{chop}$ for several values of parasitic capacitances. The relation between f_{GBW}, f_c and C_{pi} is expressed in (5). The values of V_{inj} and A_0 in (6) have been normalized to $V_{inj}=1$ and $A_0=1$.

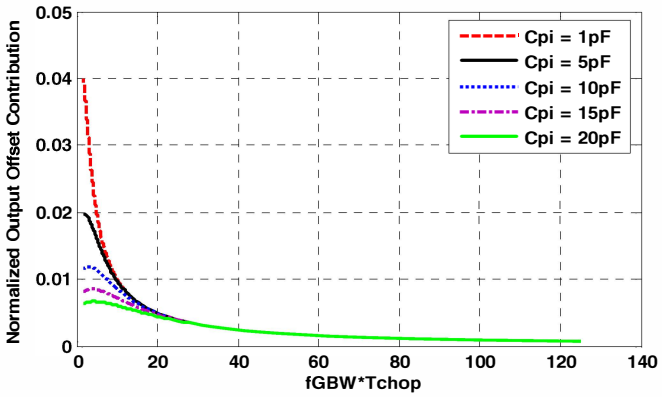

Figure 4. Normalized output offset contribution expressed in (6).

As it is illustrated, for $f_{GWB}\times T_{chop}$ approximately greater than 40, the output residual offset changes constantly for various values of C_{pi}, and has significant changes for values lower than 20. Therefore, the ratio of 40 is recommended for reducing the power consumption and minimizing the output residual offset in presence of parasitics.

C. Back-End LPF

A first-order SC LPF shown in Fig. 1 with the bandwidth equal to the sensor -3 dB bandwidth (200 Hz) is used in the back-end to do filtering at the front-end output voltage. The continuous time equivalent transfer function of the LPF is equal to $H(s) = A_1/(1+s/\omega_{-3dB})$ [5]. The DC gain, A_1, and -3dB bandwidth, ω_{-3dB} are two parameters by which a first-order LPF is determined. Where $A_1=C_1/C_2$ and $\omega_{-3dB}= (C_1/C_3)\times f_{chop}$. The C_1, C_2, and C_3 are the forward capacitance, feedback capacitance, and integration capacitance, respectively, as shown in Fig. 1. The OTA used in all building blocks is a folded-cascode amplifier which uses PMOS transistors in the input stage and is designed to minimize the flicker noise. Also, all of the switches are implemented with transmission gates. The aspect ratio of PMOS transistors in transmission gates is considered to be 4 times larger than NMOS transistors in order to maintain relatively constant on resistance.

III. Simulation Results and Comparisons

The proposed readout circuit is designed in a 0.18 µm CMOS process. It operates with 1.8 V power supply and 0.5 MHz sampling frequency, f_s. In order to evaluate the results from theoretical offset and noise analyses, the OTA with three different unity gain bandwidth, 10 MHz, 5 MHz, and 2.5 MHz is designed and used in the proposed readout circuit. In addition, two values of chopping frequency, 250 kHz and 62.5 kHz are chosen to create six different operating conditions for the circuit. These different cases are summarized in Table. I. The minimum detectable capacitance of the interface circuit for various values of C_{pi} and for the two worst and best cases of these six different conditions are shown in Fig. 5. The output noise and hence the corresponding capacitance resolution of the readout circuit are calculated by running PSS and Pnoise analyses in Spectre RF. The minimum detectable capacitance is calculated by integrating the measured output noise spectrum over entire frequency and then substituting the

noise power RMS value at (2). The time varying capacitances (representing the sense capacitors) are modeled using Verilog-A [10]. As it is illustrated from Fig. 5 and predicted by the analytical expressions, in comparison to other operating conditions, for f_s/f_{chop}= 8 and f_{GBW}/f_{chop}= 40, the readout can detect sense capacitance changes less than 3 aF and has only 1aF variation as C_{pi} changes.

Moreover, the readout performance when only CDS or CHS noise reduction technique is applied to the front-end is investigated and compared to the proposed readout performance. The results are shown in Table. II, which demonstrates that by setting circuit parameters, f_s, f_{chop}, and f_{GBW} to consume the same power for different noise reduction implementations, the combination of CDS and CHS techniques would result in much smaller resolution variation compared to the case of using only CDS or CHS techniques. However, using only CHS technique improves the minimum detectable capacitance, ΔC_{min}, of the readout circuit.

TABLE I. DIFFERENT OPRATING CASES OF THE CIRCUIT.

Parameters	f_{GBW} 10MHz	f_{GBW} 5MHz	f_{GBW} 2.5MHz	$*f_s/f_{chop}$
f_{chop}= 250kHz	f_{GBW}/f_{chop} = 40	f_{GBW}/f_{chop} = 20	f_{GBW}/f_{chop} = 10	2
f_{chop}=62.5kHz	f_{GBW}/f_{chop} =160	f_{GBW}/f_{chop} = 80	f_{GBW}/f_{chop} = 40	8

* f_s=0.5 MHz

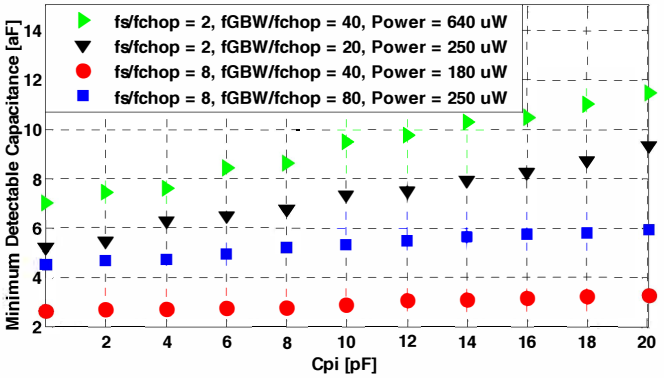

Figure 5. Minimum detectable capacitance of the proposed interface circuit for various operating conditions as input parasitic capacitances change.

TABLE II. SUMMAY OF PERFORMANCE AND COMPARISION.

Noise Reduction Technique	f_{GBW}/f_s	f_{GBW}/f_{chop}	f_s/f_{chop}	ΔC_{min} [aF]	Resolution variation [aF]	Power [µW]
Only **CDS**	20	-	-	10	12.8	640
Only **CHS**	-	* 40	-	3.9	8.5	640
Both **CDS** and **CHS**		40	2	7.1	5.3	640
Only **CDS**	10	-	-	7.4	9.6	250
Only **CHS**	-	* 20	-	3.4	6.3	250
Both **CDS** and **CHS**	-	20	2	5.1	3.7	250
Only **CDS**	5	-	-	4.6	6.2	180
Only **CHS**		* 10		1.8	4.9	180
Both **CDS** and **CHS**	-	40	8	2.4	1	180

* f_{chop}=250 kHz

IV. CONCLUSIONS

In this paper, a new SC architecture for readout IC in MEMS capacitive sensors was proposed and implemented. The front-end of the circuit uses both CDS and CHS noise reduction techniques to reduce the amplifier offset and flicker noise. A first-order SC low-pass filter is used in the back-end block to limit the output bandwidth of the sensor. Residual offset and noise analyses in presence of large parasitic capacitances are presented and used to optimize the proposed readout circuit performance in order to achieve both better capacitance resolution and less resolution variation as parasitic capacitances change. The performance of the interface circuit is compared to the cases which only one of the CDS or CHS techniques is applied to the front-end. The simulated readout circuit can detect less than 3 aF sense capacitance changes with 1 aF resolution variation as input parasitic capacitances vary up to 20 pF

APPENDIX. I

The output residual offset is equal to the mean square value of the both amplified and demodulated spike signals as follows [9]:

$$V_{off} = \frac{1}{T_{chop}} \int_0^{T_{chop}} A(n\omega) \cdot x_{spike}(t) \cdot m(t)\, dt.$$

$$= \sum_{k=1}^{\infty} \sum_{n=1}^{\infty} \frac{1}{T_{chop}} \int_0^{T_{chop}} [A_n X_n \cos(n\omega t + \phi_{X_n} + \phi_{A_n}) \times M_k \cos(k\omega t + \phi_{M_k})] dt. \quad \text{(I.1)}$$

Since the demodulation signal, $m(t)$, and spike signal, $x_{spike}(t)$, are both periodic with $T=1/f_{chop}$, they are represented by their Fourier series in (I.1). M_k and φ_{Mk} are the Fourier coefficients of demodulation signal, and X_n and φ_{Xn} are the coefficients of spike signal. Each component of $x_{spike}(t)$ is shaped both in amplitude and phase by the amplifier followed by the modulator. In fact, A_n and φ_{an} are the amplitude and phase response of the amplifier's transfer function at $n\omega$, $A(nw)$. For n≠ k, the average of cross-product term is zero, then (I.1) can be simplified to:

$$V_{off} = \sum_{n=1}^{\infty} A_n X_n M_n \frac{1}{2} \cos(\phi_{X_n} + \phi_{A_n} - \phi_{M_n}). \quad \text{(I.2)}$$

Fourier coefficients of the square-wave modulation signal, M_n and φ_{Mn}, are equal to $4/n\pi$ and $-\pi/2$, respectively, for odd value of n and zero for even value of n. In addition, the Fourier coefficients of exponentially shaped spikes are given by [9]:

$$X_n = \begin{cases} \frac{4\tau}{T_{chop}} V_{inj} \frac{1}{\sqrt{1+(n\omega\tau)^2}}, & n\,odd \\ 0, & n\,even \end{cases}, \varphi_{Xn} = \begin{cases} -\arctan(n\omega\tau), & n\,odd \\ 0, & n\,even \end{cases} \quad \text{(I.3)}$$

The amplifier used in the front-end is the folded-cascode OTA. Hence, the transfer function of a first-order amplifier is given by:

$$A(f) = \frac{A_0}{1 + j\frac{f}{f_c}} \tag{I.4}$$

By substituting the corresponding value of X_n, A_n, and M_n in (I.2), the residual offset is given by:

$$V_{off} = \frac{8\tau V_{inj} A}{\pi T_{chop}} \cdot \sum_{\substack{n=1 \\ n\ odd}}^{\infty} \frac{\frac{1}{n} \cdot \left(\frac{2\pi n\tau}{T_{chop}} + \frac{n}{T_{chop} f_c} \right)}{\left(1 + \left(\frac{2\pi n\tau}{T_{chop}} \right)^2 \right) \left(1 + \left(\frac{n}{T_{chop} f_c} \right)^2 \right)} \tag{I.5}$$

By using identity expressed in (I.6), the output residual offset is calculated as (I.7).

$$\tanh\left(\frac{\pi x}{2}\right) = \frac{4x}{\pi} \sum_{k=1}^{\infty} \frac{1}{(2k-1)^2 + x^2} \tag{I.6}$$

$$V_{off} = \frac{2V_{inj} A_0}{T_{chop}} \cdot \frac{\tau f_c}{1 - 2\pi\tau f_c} \times \left[2\pi\tau \tanh\left(\frac{T_{chop}}{4\tau}\right) - \frac{1}{f_c} \tanh\left(\frac{\pi f_c T_{chop}}{2}\right) \right] \tag{I.7}$$

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