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A Nanowatt Low Voltage Subthreshold CMOS Voltage Reference Based On 2-T

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***Abstract*— This article presents the design and implementation of a nanowatt CMOS voltage reference circuit capable of operating with a low supply voltage and functioning over a wide temperature range for IoT and biomedical applications. The core of the proposed voltage reference circuit is based on a two-transistor structure. By utilizing the PMOS leakage current biasing technique, the circuit achieves ultra-low voltage operation. This method does not rely on on-chip resistors or operational amplifiers (opamps), thereby reducing complexity and improving reliability. The design is implemented using 0.18-µm CMOS technology. The circuit consumes approximately 69 nA from a minimum supply voltage of 0.9 V at room temperature. The untrimmed output voltage is 560 mV, exhibiting an average temperature coefficient (TC) of 43.4 ppm/°C over the temperature range of -40°C to 85°C. The line-voltage sensitivity (LS) is measured 0.303%/V when the input supply voltage varies from 0.9 V to 1.8 V. Finally the DC power supply rejection ratio (PSRR) at 100 Hz is -81.5 dB.**

Keywords*— nanowatt, CMOS voltage reference circuit, IoT applications, PMOS leakage current, low voltage, reliability.

I. Introduction

In many electrical circuits, ranging from amplifiers to analog-to-digital converters (ADCs), digital-to-analog converters (DACs) and phase-locked loop (PLL) circuits, require stable and constant voltage and current reference sources. The term constant refers to the fact that the reference voltage or current should be independent of the power supply and insensitive to temperature variations. The supply voltage of a circuit can vary within an allowable range. However, this voltage often contains a significant amount of noise due to current variations in different circuit components caused by switching or voltage range fluctuations, among other factors. When a constant reference source is required, it is necessary to design the reference source in such a way that it remains independent of the circuit's power supply and unaffected by its variations. This independent reference source is referred to as a source independent of the power supply.

Various methodologies for designing CMOS voltage references (CVR) have been explored in the literature [1]–[16]. The widely adopted approach uses a bandgap voltage reference (BGR) employing parasitic BJTs (bipolar junction transistors). BGR using BJT is a commonly used type of voltage reference that generates a reference voltage with minimal variation due to process, voltage, and temperature (PVT) effects. However, BGRs are not well-suited for applications requiring low supply voltage and low power consumption [1, 2, 10, 11]. This technique combines two voltages with opposite temperature characteristics, a complementary-to-absolute-temperature (CTAT) voltage and a proportional-to-absolute-temperature (PTAT) voltage, to generate a temperature-independent output voltage. Alternatively, some designs utilize the combination of PTAT and CTAT currents, rather than voltages, to achieve a temperature-independent output voltage [3]–[6]. Replacing bipolar transistors with diode-connected MOS transistors biased in the subthreshold region is a suitable alternative in other methods [7]–[9]. The obtained voltage in this case is much lower than the emitter-base voltage of bipolar transistors, allowing them to be used in low-voltage applications. A two-transistor (2-T) subthreshold CVR, as described in [9], obtains the reference voltage by comparing the threshold voltages of two distinct transistor types, resulting in picowatt power consumption and a minimum supply voltage of 0.5 V. Nonetheless, the autonomy of the reference voltage concerning the supply voltage may be compromised by the channel-length modulation effect on the upper transistor linked to VDD in this 2-T structure circuit.

This paper proposes an ultra-low nanowatt voltage reference with sufficiently high line sensitivity (LS) using only seven transistors. In order to protect the delicate core from V_{DD} and to enable circuit operation at high temperatures, a temperature-dependent cascode current generator has been introduced. The suggested system exhibits exquisite performance metrics over the supply voltage range of 0.9 V-1.8 V in a 180-nm prototype.

The structure of the paper is organized as follows: In Section II, the CMOS voltage reference architecture and operational principles are introduced. Section III outlines simulation results, including a comparison with previous work, and finally, Section IV concludes the paper.

II. Proposed CMOS Voltage Reference

A. Circuit Description

The conventional structure of a subthreshold voltage reference circuit based on 2-T is illustrated in Fig. 1(a). In this configuration, a native transistor with a threshold voltage close to zero (NVT) is employed as the bias of M_{10}. Since transistor M_{11} is an NVT transistor and its gate is connected to ground, it operates in the subthreshold region,

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producing a very small current that results in generating a relatively low voltage. To generate higher voltages, the structure in Fig. 1(b) can be utilized. In this arrangement, instead of an nMOS, a pMOS with a moderate threshold voltage (MVT) is used as the bias. Similar to the previous circuit, this structure also encounters issues such as low line sensitivity, PSRR, and other challenges which will be discussed in the following section. The proposed subthreshold CVR circuit based on 2-T is shown in Fig. 1(c). In this arrangement, an attempt has been made to enhance the performance metrics by introducing a few transistors to structure (b). To fulfill the criteria of limited space, reduced voltage, and minimal power usage in internet of things (IoT) applications, all components in this design function in the subthreshold zone. The efficiency of the suggested circuit is additionally improved by the exclusion of operational amplifiers and passive elements like resistors and capacitors.

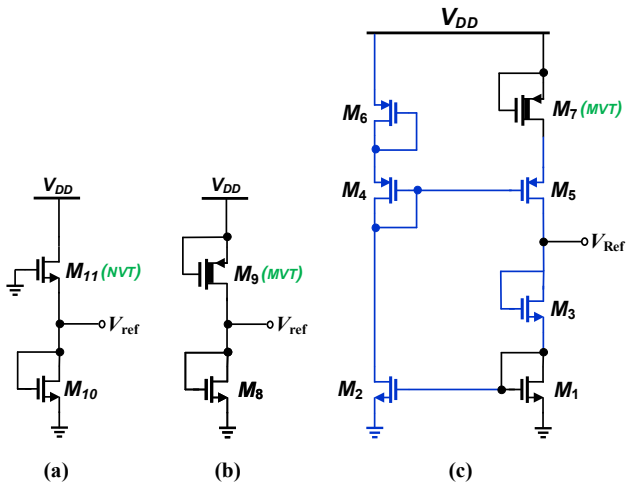

Fig. 1: Schematic of (a) Conventional 2-T CVR used in [9] and (b) 2-T CVR using MVT pMOS and (c) Proposed CVR based on 2-T.

When the voltage across the drain and source of a transistor is sufficiently higher than the thermal voltage (V_T), the subthreshold current can be defined as follows:

$$I_{sub} = \mu C_{ox} \frac{W}{L} (\zeta - 1) V_T^{\,2} \exp\left(\frac{V_{GS} - V_{TH}}{\zeta V_T}\right) \qquad (1)$$

where μ is the mobility and C_{ox} is gate oxide capacitance per unit area. W and L represent the width and length of the transistor, respectively. ζ is subthreshold slope factor ($\zeta = 1 + C_d/C_{ox}$ where C_d is depletion capacitance per unit area), V_T is thermal voltage (kT/q), V_{GS} is gate-source voltage and V_{TH} is transistor threshold voltage. In the proposed configuration, by considering the similarity between their depletion capacitance (C_d) and gate oxide capacitance (C_{ox}), their subthreshold slope factors can be assumed to be equal. Furthermore, by equalizing the currents flowing through M_1 and M_7 , we can write:

$$\mu_n C_{ox} (\frac{W}{L})_1 \exp\left(\frac{V_{REF}/2 - V_{TH,1}}{\zeta V_T}\right) = \mu_p C_{ox} (\frac{W}{L})_7 \exp\left(\frac{0 - |V_{TH,7}|}{\zeta V_T}\right) \qquad (2)$$

Then, the output reference voltage can be expressed as:

$$V_{Ref} = 2 \times \left[|V_{TH,7}| - V_{TH,1} + \zeta V_T \ln\left(\frac{\mu_p}{\mu_n} \frac{(\frac{W}{L})_7}{(\frac{W}{L})_1}\right)\right] \qquad (3)$$

The threshold voltage difference between nMOS and pMOS transistors can be expressed below [12].

$$V_{TH,1} - |V_{TH,7}| = \Delta V_{TH}(T_0) + (\alpha_1 - \alpha_7) T_0 - (\alpha_1 - \alpha_7) T \qquad (4)$$

Here, $\Delta V_{TH}(T_0)$ represents the variation in threshold voltage between M_1 and M_7 under normal room temperature conditions. α_1 and α_7 represent the temperature factors associated with $V_{TH,1}$ and, $|V_{TH,7}|$ respectively. Since α_7 is greater than α_1, the disparity in the threshold becomes directly PTAT. It is crucial to ensure that W_7 is more petite than W_1 to achieve a CTAT in the last term of equation (3). Consequently, After compensation, the zero-temperature coefficient (ZTC) V_{Ref} will be:

$$V_{Ref} = 2 \times \left[|V_{TH,7}(T_0)| - V_{TH,1}(T_0) + (\alpha_7 - \alpha_1) T_0 \right] \qquad (5)$$

B. Line sensitivity and PSRR

As illustrated in Fig. 1(b), the bias transistor M_9 operates in the subthreshold region with its gate and source linked to VDD, serving as a biasing component. Consequently, during startup, as the input voltage increases, the current also increases, causing the output reference voltage to reach its final value. It is worth noting that The drain terminal of transistor M_9 is likely connected to a constant voltage (V_{Ref}), while its source terminal is connected to V_{DD}. Thus, the ripple present in the power supply is directly reflected in the drain-source voltage of transistor M_9; even if the channel length and drain-source voltage are maximized, the sensitivity and Power Supply Rejection Ratio (PSRR) are low due to the channel length modulation effect. Hence, the objective of transistor M_5 is to decouple the output from the drain of transistor M_9, where the drain-source voltage of transistor M_9 is maintained independently of the power supply by configuring the bias network in such a way that variations can be transferred to the drain. The biasing of transistors M_6 and M_7 is achieved by mirroring of the primary circuit branch current. By appropriately sizing M_6 and M_7 transistors, the input voltage variations that directly appeareing at the output in the two-transistor structure can be significantly reduced by adding the left-side path. As a result, this approach increases PSRR and improves LS. By considering the exponential term of the subthreshold current effect, the output voltage reference can be redefined as follows:

$$V_{\text{Ref}} = 2\times\left[\,|V_{TH,7}| - V_{TH,1} + \zeta V_T \ln\left(\frac{\mu_p}{\mu_n}\frac{(\frac{W}{L})_7}{(\frac{W}{L})_1}\right) + \zeta V_T \ln\left(1-\exp(\frac{V_{SG5}-V_{SG6}-V_{SG7}}{V_T})\right)\right] \quad (6)$$

Unlike the 2-T structure, where the expression V_{DD} was present internally, in this configuration, the output reference voltage related to the gate-to-source voltage difference, leading to an enhancement in line sensitivity.

Considering the small-signal equivalent circuit of the 2-T structure, which is essentially a resistive divider, the PSRR can be expressed as follows:

$$PSRR\big|_{2\text{-}T} = \frac{1/g_{m8}}{1/g_{m8}+r_{ds,9}} = \frac{1}{1+g_{mn}r_{dsp}} \quad (7)$$

g_{mn} represents the transconductance of nMOS transistors and r_{dsp} denotes the output resistance of pMOS transistors. Fig. 2 depicts the proposed AC equivalent model for calculating the PSRR of the proposed structure which PSRR can be evaluated as below:

$$\frac{V_{Ref}}{V_{dd}} = \left(\frac{g_{m1}+g_{m3}}{g_{m3}}\right)\left(\frac{1}{1+g_{m5}r_{ds5}}\right)\left(\frac{g_{m4}+g_{m6}}{g_{m4}+g_{m6}+g_{m4}g_{m6}r_{ds2}}\right) \times\left(\frac{g_{m1}g_{m4}g_{m6}(1+g_{m5}r_{ds5})}{g_{m1}g_{m4}g_{m6}(1+g_{m5}r_{ds5})-g_{m5}g_{m2}(g_{m4}+g_{m6})}\right) \quad (8)$$

If we assume $I_2 / I_1 = \beta$ hence, $g_{m2,4,6} = \beta\,(g_{m1,3,5,7}) = g_{mn}$ and $r_{ds2,4,6} = (1/\beta)\ r_{ds1,3,5,7} = (1/\beta)\ r_{dsp}$. ultimately, PSRR can be reformulated as follows:

$$PSRR\big|_{\text{Proposed}} = (1+\frac{1}{\beta})\times\frac{1}{1/\beta g_{mn}r_{dsn}}\times\frac{2}{2+g_{mn}r_{dsn}}\times\frac{g_{mn}r_{dsn}}{g_m r_{dsn}-2} \approx \frac{2\beta}{g_{mn}r_{dsp}\times g_{mn}r_{dsn}}\times(1+\frac{1}{\beta}) \quad (9)$$

By comparing equations (7) and (9), the improvement in PSRR can be determined.

$$PSRR\big|_{\text{Proposed}} = \frac{2(\beta+1)}{g_{mn}r_{dsn}} PSRR\big|_{2\text{-}T} \quad (10)$$

The enhancement will be significant depending on β and $g_{mn}r_{dsn}$. Scaling down increases the PSRR compared to the 2-T structure. However, increasing β leads to higher power consumption. Therefore, a careful selection of β and $g_{mn}r_{dsn}$ can achieve both high PSRR and low power dissipation.

III. Simulation Results

The 0.18-µm CMOS process is employed to simulate the voltage reference circuit being discussed, and the specific device dimensions can be found in Table 1. The size ratios are fine-tuned to optimize the line sensitivity and temperature coefficient of the V_{Ref} output. TC is a significant parameter of a voltage reference circuit. It evaluates the level of independence of the output reference voltage concerning temperature variations. Fig. 3 shows the variations of the output reference voltage concerning temperature at different corner cases. By examining the extent of voltage fluctuations within the temperature spectrum, one can ascertain TC using the subsequent formula:

$$TC = \frac{V_{Ref,\max} - V_{Ref,\min}}{V_{Ref,average}} \times \frac{1}{T_{\max} - T_{\min}} \quad (11)$$

Where $V_{Ref,max}$ represents the maximum value of the reference voltage, $V_{Ref,min}$ denotes the minimum value of the reference voltage and $V_{Ref,average}$ is the average output reference voltage within the temperature range from T_{min} to T_{max}. Considering that the temperature coefficient is on a micro-scale, it is typically multiplied by one million and reported in parts per million (ppm). Fig. 4 shows the output reference voltage versus temperature with different power supply which demonstrates that the proposed voltage reference circuit is independent of the input voltage.

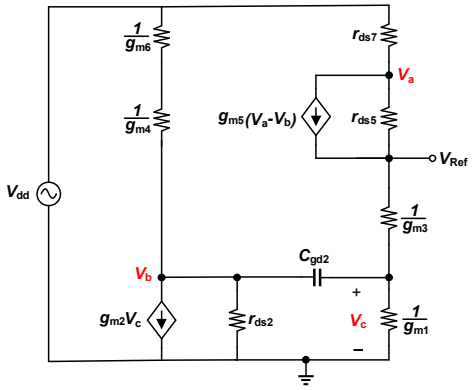

Fig. 2: AC equivalent circuit diagram exploited for PSRR calculation.

TABLE I: TRANSISTOR SIZES OF THE PROPOSED CIRCUIT.

Transistors	W [µm]	L [µm]	M
$M_{1,2,3}$	9	18	9
M_4	14	2.2	1
M_5	70	2.2	1
M_6	0.22	5	1
M_7	45	5	2

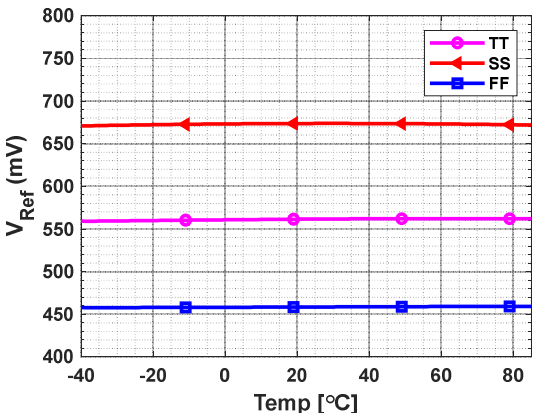

Fig. 3: V_{Ref} vs. temperature with different corner cases @ 1.8 V supply.

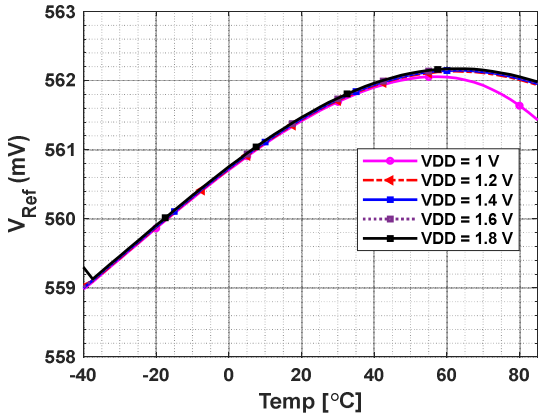

Fig. 4: V_{Ref} vs. temperature with different input supply voltage.

The LS parameter can be calculated based on Fig. 5 which compares the dependency of V_{Ref} on V_{DD} for the 2-T and modified structure. The LS parameter actually evaluates the independence level of V_{Ref} with to supply voltage and can be defined as follows:

$$LS = \frac{V_{Ref,\max} - V_{Ref,\min}}{V_{Ref,average}} \times \frac{1}{V_{DD,\max} - V_{DD,\min}} \qquad (12)$$

Where $V_{DD,max}$ and $V_{DD,min}$ are the maximum and minimum values of the input supply voltage, respectively. The minimum value of supply voltage in this structure is 0.9 volt.

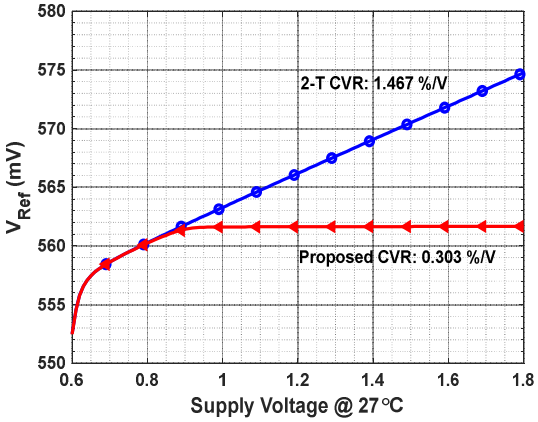

Fig. 5: V_{Ref} vs. supply voltage of the proposed CVR compared with 2-T.

In Fig. 6 the PSRR is graphed against frequency under room temperature conditions, considering various corner cases and a 1.8 V input supply voltage. The chart reveals that the PSRR exhibits strong attenuation at low frequencies, approximately -85 dB for frequencies up to 100 Hz. Notably, at higher frequencies, the PSRR performance gradually diminishes, reaching approximately -50 dB at 1 MHz. Fig. 7 illustrates the startup waveform of the output voltage reference when the input voltage changes from 0 to 0.9 volts. Based on the depicted waveform, the startup time of the voltage reference circuit is approximately 6 ms. Fig. 8 shows the noise spectrum of V_{Ref} with a 1.8 V supply at room temperature, where no load capacitor is present. The output noise level is measured at 0.56 µV/ √Hz at 1 Hz, and the integrated noise over the frequency range of 0.1 Hz to 10

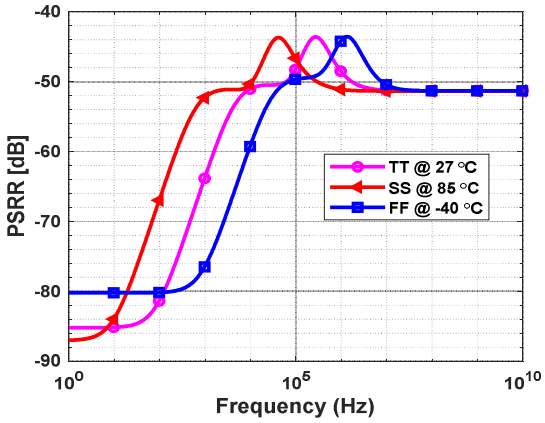

Fig. 6: Assessed the PSRR of the CVR under various corner cases @ 1.8 V supply.

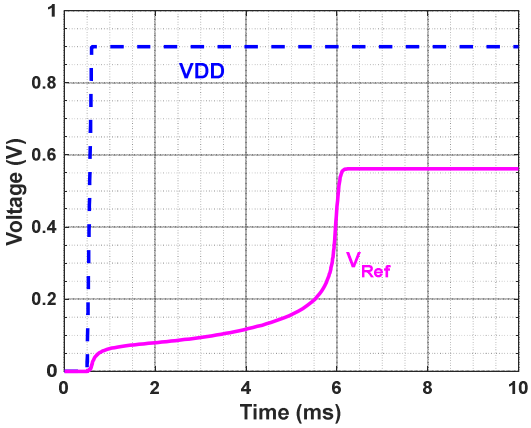

Fig. 7: Start-up response of V_{Ref} in room temperature at @ 0.9 V supply.

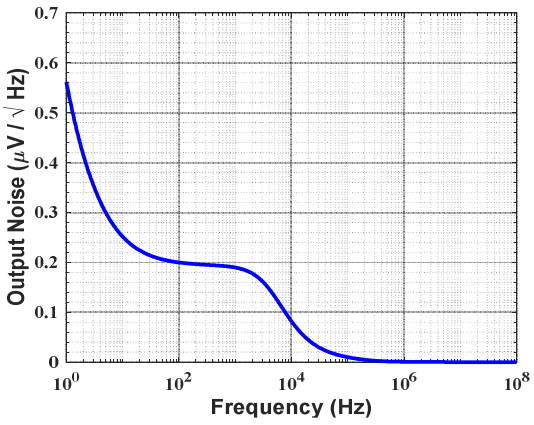

Fig. 8: Output noise for TT corner @ 1.8 V supply.

Hz amounts to 3.366 µV.

Table II provides a summary and compares the performance of the proposed design with suggested designs in recent years. In brief, the temperature coefficient and line sensitivity are enhanced. The improvement of PSRR was achieved by incorporating of transistor M_5 into the circuit, and finally, this method exhibits exceptionally low noise. The proposed circuit is more suitable compared to other references in terms of TC and PSRR. Furthermore, [13, 14, 15,17] have an appropriate LS, but relatively low PSRR, and the proposed circuit also has a similar LS to [16].

TABLE II: PERFORMANCE SUMMARY AND COMPARISON WITH OTHER WORKS.

Reference	[9]	[13]	[14]	[15]	[16]	[17]*	This work*
Technology (nm)	130	180	180	180	180	180	180
Minimum Input Voltage (V)	0.5	0.4	1.5	0.9	0.5	0.6	0.9
Reference Voltage (mV)	174.9	151	985	261	288	0.3078	560
Temp. Range (℃)	-20~80	-40~125	-40~85	-40~130	-10~100	-20~80	-40~85
LS (% / V)	0.033	0.0154	0.003	0.01	0.23	0.02	0.303
TC (ppm / °C)	231	89.83	60.86	62	90	24.8	43.4
PSRR [dB]	-53 @ 100 Hz	-47 @ 1 kHz	-93 @ 10 Hz	-73.5 @ 100 Hz	-45 @ 100 Hz	-54 @ 100 Hz	-81.5 @ 100 Hz
Power (nW)	0.0022	1	63	1.8	0.5	0.0214	61.59
No. Transistors	2	6	36	12	5	6	7

*SIMULATION RESULTS

IV. CONCLUSION

A highly efficient CMOS voltage reference with 0.56 V output voltage has been introduced, utilizing a 0.18-µm CMOS process. The proposed structure introduces improvements in certain evaluation parameters by incorporating a number of transistors into the two-transistor (2-T) configuration. The proposed subthreshold CMOS voltage reference achieves a remarkable temperature coefficient (TC) across a wide temperature range. Simulation results confirmed the high line sensitivity (LS), power supply rejection ratio (PSRR), and low output noise.

REFERENCES

[1] A. P. Brokaw, "A simple three-terminal IC bandgap reference," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 388–393, Dec. 1974.

[2] B.-S. Song and P. R. Gray, "A precision curvature-compensated CMOS bandgap reference," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 634–643, Dec. 1983.

[3] H. Banba, H. Shiga, A.Umezawa, T.Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference circuit with sub-1V operation," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 670–674, May 1999.

[4] K. N. Leung and P. K. T. Mok, "A Sub 1 V 15 ppm C CMOS bandgap voltage reference without requiring low threshold voltage device," *IEEE J. Solid-State Circuits*, vol. 37, no. 4, pp. 526–530, Apr. 2002.

[5] A. Boni, "Op-amps and startup circuits for CMOS bandgap references with near 1 V supply," *IEEE J. Solid-State Circuits*, vol. 37, no. 10, pp. 1339–1343, Oct. 2002.

[6] J. Doyle, Y. J. Lee,Y.-B. Kim,H.Wilsch, and F. Lombardi, "A CMOS sub-bandgap reference circuit with 1 V power supply voltage," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 252–255, Jan. 2004.

[7] P. Kinget, C. Vezyrtzis, E. Chiang, B. Hung, and T. L. Li, "Voltage references for ultra-low supply voltages," in Proc. *IEEE Custom Integr. Circuits Conf*, 2008, pp. 715–720.

[8] L. Magnelli, F. Crupi, P. Corsonello, C. Pace, and G. Iannaccone, "A 2.6 nW, 0.45 V temperature-compensated subthreshold CMOS voltage reference," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 465–474, Feb. 2011.

[9] M. Seok, G. Kim, D. Blaauw, and D. Sylvester, "A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5 V," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2534–2545, Oct. 2012.

[10] B. Ma and F. Yu, "A Novel 1.2–V 4.5-ppm/°C Curvature-Compensated CMOS Bandgap Reference," *IEEE Trans. Circuits and Sys. I: Reg. Papers*, vol. 61, no. 4, pp. 1026-1035, April 2014.

[11] H. Chen, C. Lee, S. Jheng, W. Chen and B. Lee, "A Sub-1 ppm/°C Precision Bandgap Reference With Adjusted-Temperature-Curvature Compensation," *IEEE Trans. Circuits and Sys. I: Reg. Papers*, vol. 64, no. 6, pp. 1308-1317, June 2017.

[12] Wang and C. Zhan, "A 0.7-V 28-nW CMOS Subthreshold Voltage and Current Reference in One Simple Circuit," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 9, pp. 3457-3466, Sept. 2019.

[13] J. Lin, L. Wang, C. Zhan and Y. Lu, "A 1-nW Ultra-Low Voltage Subthreshold CMOS Voltage Reference With 0.0154%/V Line Sensitivity, " *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 10, pp. 1653-1657, Oct. 2019.

[14] Y. Chen and J. Guo, "A 42nA IQ, 1.5–6V VIN, Self-Regulated CMOS Voltage Reference With –93dB PSR at 10 Hz for Energy Harvesting Systems," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* pp. 1-5, Early Access, Feb. 2021.

[15] C. -Z. Shao, S. -C. Kuo and Y. -T. Liao, "A 1.8-nW, −73.5-dB PSRR, 0.2-ms Startup Time, CMOS Voltage Reference With Self-Biased Feedback and Capacitively Coupled Schemes, " *IEEE Journal of Solid-State Circuits*, vol. 56, no. 6, pp. 1795-1804, June 2021.

[16] J. Wang, X. Sun and L. Cheng, "A Picowatt CMOS Voltage Reference Operating at 0.5-V Power Supply With Process and Temperature Compensation for Low-Power IoT Systems, " *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 4, pp. 1336-1340, April 2023.

[17] L. Colbach, T. Jang, and Y. Ji, "A 21.4 pW Subthreshold Voltage Reference with 0.020 %/V Line Sensitivity Using DIBL Compensation," Sensors, vol. 23, no. 4, p. 1862, Feb. 2023.