A Low-Power High-Precision Low-Dropout Regulator For Biomedical Implants

Vahid Baghbani Khezerlu
Integrated Circuits Design Laboratary, Electrical Engineering Depatment of Amirkabir University of Technology (Tehran Polytechnic),
Tehran, Iran
Email: v.baghbani@aut.ac.ir

Mohammad Yavari
Integrated Circuits Design Laboratary, Electrical Engineering Depatment of Amirkabir University of Technology (Tehran Polytechnic),
Tehran, Iran
Email: myavari@aut.ac.ir

Mortaza Mojarad
Microelectronics Research Laboratary, Electrical Engineering Depatment of Urmia University
Urmia, Iran
Email: m.mojarad@urmia.ac.ir

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***Abstract*— This article presents a new low-power, high-gain and high-precision output capacitor-less low-dropout (LDO) regulator for biomedical implants. The proposed LDO regulator consists of an adaptive biased super class-AB recycling folded-cascode error amplifier which provides a high and almost constant gain for the system over the output current range. Due to the specific structure of the proposed regulator, a novel compensation method has been designed and utilized to guarantee the system's stability over various conditions of load and process. The proposed LDO regulator has been simulated in TSMC-0.18µm CMOS technology with a quiescent current of 1.99 µA at no load. The regulator's output voltage is 1.8V with 200mV dropout voltage, and the maximum output current of the LDO is 10 mA. Furthermore, simulation results shows improved line and load regulations, which equals 3 mV/V and 20 µV/mA, respectively.**

Keywords*— Low-dropout (LDO) regulator, Adaptive biasing, Super class-AB error amplifier, Low-power, Biomedical implants

I. Introduction

Low dropout (LDO) voltage regulators are one of the essential components in the power management unit of complex and highly integrated systems like biomedical implants. In implantable biomedical applications, the main goal of implanting a system inside the body is to record and analyze biological signals in better quality. Therefore, providing a stable, clean, and accurate power supply in these systems is an inevitable task. Recently, due to increasing attends to system-on-chip (SoC) applications like biomedical implants, various versions of LDO regulators for these applications have been introduced. In [2] a flipped voltage follower-based structure with a 50 mV dropout voltage has been introduced. In this work, the major idea is to improve power efficiency by reducing the dropout voltage in all output current ranges. Furthermore, a self-supplied differential error amplifier (EA) has been designed and utilized for higher power supply rejection (PSR). However, the structure introduced in [2] suffers from a poor line and load regulation because of small loop gain; its minimum quiescent current is 33 µA which is unsuitable for power-limited applications like biomedical implants. In [4] the bulk modulation technique has been introduced. In this work, the bulk voltage of the output transistor is controlled by a separate high bandwidth feedback loop to improve the load and line regulation. However, the quiescent current of this work is 99 µA and is not appropriate for portable applications. In [1], a telescopic-cascode output structure is utilized at the output stage of the regulator instead of the push-pull amplifier to improve the loop gain. In addition, a dual-path active-feedback frequency compensation scheme is exploited to enhance both the stability and gain bandwidth (GBW) of the LDO regulator. Nonetheless, the obtained line and load regulations have not been improved significantly, and the regulator consumes a relatively large quiescent current of 14 µA. This paper focuses on improving the transient response by using a super class-AB error amplifier , providing a high precision output voltage and introducing an appropriate frequency compensation using adaptive biasing scheme to achieve higher gain-bandwidth product and sufficient stability. The rest of this article is organized as follows. Section II reviews the systematic structure of the proposed regulator. Circuit implementation of proposed regulator is introduced in Section III. Section IV presents the simulation results and finally, Section V provides the conclusion.

II. Systematic Structure

Fig. 1 shows the structure of the proposed three-stage LDO regulator, which consists of a two-stage super class-AB error amplifier, a power MOSFET (M_p) as the output stage, compensation loops, adaptive biasing circuit and a MOS feedback network (M_{s1}, M_{s2} and M_{s3}). The load is modeled by a capacitor C_{out} , representing the load capacitance and a current source, I_{Load}. Eventually, V_{DD}, V_{out}, V_{ref} represent unregulated input voltage, regulated output voltage, and the reference voltage of the regulator, respectively.

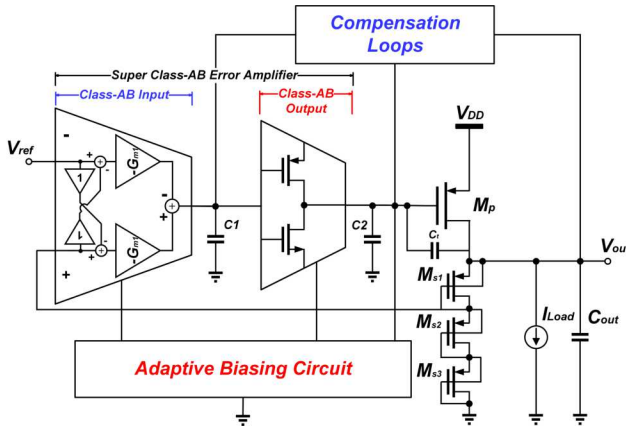

Fig. 1. Proposed LDO voltage regulator architecture.

To realize high output current for the regulator the dimension of the pass transistor is needed to be large in comparison with other transistors in the circuit. Thus, the parasitic capacitance at the gate of the power transistor (C_2) is large, which causes longer charge and discharge time in load transient and a poor transient response. To overcome this problem without increasing bias current of the error

amplifier, an error amplifier with class-AB output stage is used to charge and discharge the gate capacitance of the pass transistor. Moreover, to improve the transient response of the proposed regulator, a class-AB input stage has been used to realize the dynamic biasing technique and boost the current bias of the error amplifier in transient mode. Unlike previous versions of dynamic biasing circuits [3], the proposed method of realization of dynamic biasing does not need any additional decoupling capacitor or any output voltage sensing circuit, and it improves both the circuit's small and large signal behavior. Moreover, the proposed method for the realization of dynamic biasing is not sensitive to the amount of output voltage changes and operates in negative and positive output current steps. Furthermore, an adaptive biasing circuit, which changes the internal block's bias current proportional to output current, is added to the structure to improve transient and frequency responses. Due to the deployment of dynamic biasing, to enhance transient response, it is not necessary to create significant changes in bias current using the adaptive biasing technique, which results in an almost constant gain and improved line and load regulation. In this work adaptive biasing technique has been used to improve frequency response by changing poles location which will be discussed in section III.

III. Circuit Implementation

This section will present a high gain, output-capacitor-free LDO, which combines the adaptive biasing and the dynamic biasing technique using a super class-AB error amplifier and an adaptive biasing circuit to improve the transient response. First, we will discuss the implementation of a high gain error amplifier, which is naturally implementing dynamic biasing techniques. Then, we will present the implementation of the adaptive biasing technique. The last part of this section will provide the proposed regulator's stability analysis, which uses a new compensation method.

A. High gain super class-AB error amplifier

Loop gain plays a crucial role in closed-loop systems like LDO voltage regulators. It is shown in previous works that parameters such as line and load regulation, which indicate the accuracy of the regulator, improve with increasing the closed-loop gain of the regulator [7]:

$$\text{Line Regulation} = \frac{\Delta V_{out}}{\Delta V_{IN}} \approx \frac{g_{mp} r_{op}}{L_o} + \frac{1}{\beta}.\left(\frac{\Delta V_{REF}}{\Delta V_{IN}}\right)$$
$$\text{Load Regulation} = \frac{\Delta V_{out}}{\Delta I_{out}} = -\frac{r_{op}}{1 + L_o} \quad (1)$$

Where L_o is low-frequency loop gain, β is the feedback factor of the system and g_{mp} and r_{op} are the transconductance and output resistance of the power PMOS transistor, respectively.

Also, it is shown that the PSRR of the regulator, which indicates the regulator's ability to eliminate fluctuations of the input voltage, improves with high closed-loop gain [10]:

$$PSRR \approx \frac{1}{L_o} \quad (2)$$

Where L_o is low-frequency loop gain of the structure.

Recently one of the most commonly used architectures, whether as a single-stage or first stage in multi-stage amplifiers and regulators, had been the folded cascode (FC) amplifier for its high gain and reasonably large signal swing in the present and future low voltage CMOS processes. However because of its slow behavior in transient state, many modified FC versions has been introduced. One of the most efficient structures of modified FCs, is the recycling folded cascode (RFC) [11]. In this structure the idea is to use idle devices in the signal path to achieve an enhanced transconductance, gain, and slew rate. Despite improvement in gain and slew rate in RFC compared to FC, its slew rate is still limited by the bias current. One of the best solutions to eliminate the slew rate dependence to bias current is to use a class-AB input structure. Fig. 2 shows the proposed structure in this work.

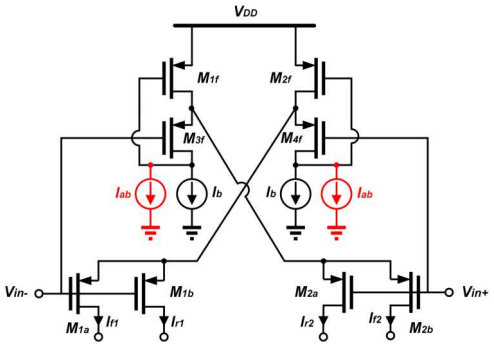

Fig. 2. Proposed class-AB input.

In this structure, $M_{1f\text{-}4f}$ forms two flipped voltage follower buffers, $M_{1a\text{-}1b}$,and $M_{2a\text{-}2b}$ form non-inverting and inverting input transistors, respectively and I_b and I_{ab} are bias and adaptive biasing current sinks, respectively. In steady-state, assuming the DC voltage of two inputs to be equal, we will have:

$$V_{gs_{1a}} = V_{gs_{1b}} = V_{gs_{4f}}, V_{gs_{2a}} = V_{gs_{2b}} = V_{gs_{3f}} \quad (3)$$

Where V_{gsi} show the gate-source voltage of M_i. So:

$$I_{f1} = I_{r1} = I_{M_{4f}} = I_b + I_{ab}$$
$$I_{f2} = I_{r2} = I_{M_{3f}} = I_b + I_{ab} \quad (4)$$

Where I_{f1}, I_{f2}, I_{r1}, I_{r2}, I_{M3f}, and I_{M4f} show the drain current of M_{1a}, M_{2a}, M_{1b}, M_{2b}, M_{3f} and M_{4f}, respectively and I_b, and I_{ab} stands for bias current sink, and adaptive bias current sink. In transient mode, the signal at the gate of each input transistor passes to the source of the opposite input transistors via the corresponding flipped voltage follower cell and determines and amplifies gate-source voltage (V_{gs}) of each input transistor. As a result, the transient current of input transistors is no longer limited by the bias current. This structure boosts the circuit's current according to the output voltage changes in the transient mode, which refers to the dynamic biasing technique in LDO regulators. This method of realization of dynamic biasing does not need any additional decoupling capacitor, resistance, or output voltage sensing circuit, thus improving the structure in terms of area and power. Furthermore, unlike the previous realizations of dynamic biasing [3], this method is not sensitive to the amount of output voltage changes and improves large-signal parameters, like slew rate, and small-signal parameters, like

gain, continuously. Two adaptive biasing current sinks have been added to the structure to change the bias current of the input stage with respect to output current to improve transient and frequency responses. When output current changes, an output sensing circuit senses the current changes and via adaptive biasing circuit, the bias current of internal blocks is set. We will come back to adaptive biasing at the end of this section. Fig. 7 depicts the circuit schematic of the proposed regulator where $M_{1a\text{-}1b}$, $M_{2a\text{-}2b}$, $M_{1\text{-}4c}$, and $M_{3\text{-}12}$ form the main core of the first stage of the error amplifier, which as mentioned before, is a recycling folded cascode (RFC). In RFC structure, M_3 and M_4, which in FC structure have the largest transconductance, and act as a simple current sink, are split to form the current mirrors M_{3c}, M_3 and M_{4c}, M_4 with a ratio of K: 1. This modification k times improves the conventional FC structure in terms of gain and slew rate.

As mentioned before, the rate of charge and discharge of parasitic capacitor at the pass transistor gate is the bottleneck of settling time in LDO regulators. It can be shown that for agile changes in the load current, the recovery time of the output voltage can be written as [4]:

$$t_{rec} \approx \frac{1}{BW_{cl}} + t_{slew} = \frac{1}{BW_{cl}} + C_{par}\frac{\Delta V_A}{I_{slew}} \tag{5}$$

Where BW_{cl} is the closed-loop bandwidth of the regulator and t_{slew} is the time delay due to the slewing of the error amplifier while driving the pass transistor. In (5), C_{par} is the total parasitic capacitance seen at the output of the error amplifier (mainly dominated by the gate capacitance of the pass transistor), ΔV_A and I_{slew} are the output voltage change and maximum slew current of the error amplifier. In this article, to address this issue, a class-AB stage has been proposed as output stage of the error amplifier to improve I_{slew} independently of bias current. Fig. 3 illustrates the proposed push-pull output stage, which consists of $M_{1\text{-}2}$ as output transistors, $M_{5\text{-}8}$, and $I_{b3\text{-}4}$ as bias transistors, and bias current sources, respectively. The input signal will be applied to this stage via nodes A or B showed in Fig. 3. First, we provide a DC analysis for this stage. Using KVL in the appropriate loops, we will have:

$$\begin{aligned} V_{GS3} + V_{GS1} &= V_{GS5} + V_{GS6} \\ V_{GS2} + V_{GS4} &= V_{GS7} + V_{GS8} \end{aligned} \tag{6}$$

Where V_{GSi} is the source-gate voltage of M_i. According to the quadratic model of the MOS device, the above equations can be rewritten as (I_{ab2} and I_{ab3} are neglected):

$$\begin{aligned} \sqrt{\frac{2I_o}{\mu_n C_{ox}(\frac{W}{L})_1}} &= \sqrt{\frac{2I_{b2}}{\mu_n C_{ox}(\frac{W}{L})_5}} + \sqrt{\frac{2I_{b2}}{\mu_n C_{ox}(\frac{W}{L})_6}} - \sqrt{\frac{2I_{b1}}{\mu_n C_{ox}(\frac{W}{L})_3}} \\ \sqrt{\frac{2I_o}{\mu_p C_{ox}(\frac{W}{L})_2}} &= \sqrt{\frac{2I_{b3}}{\mu_p C_{ox}(\frac{W}{L})_7}} + \sqrt{\frac{2I_{b3}}{\mu_p C_{ox}(\frac{W}{L})_8}} - \sqrt{\frac{2I_{b1}}{\mu_p C_{ox}(\frac{W}{L})_4}} \end{aligned} \tag{7}$$

Where $\mu_n C_{ox}$ and $\mu_p C_{ox}$ stand for technology parameters and $(W/L)_i$ shows the dimension of M_i. If for simplification, we assume that:

$$\begin{aligned} &(\frac{W}{L})_3 = (\frac{W}{L})_5 = (\frac{W}{L})_6, \quad (\frac{W}{L})_4 = (\frac{W}{L})_7 = (\frac{W}{L})_8 \\ &\frac{(\frac{W}{L})_1}{(\frac{W}{L})_3} = \frac{(\frac{W}{L})_2}{(\frac{W}{L})_4}, \qquad I_{b2} = I_{b3} \end{aligned} \tag{8}$$

Then the equation (7), can be simplify to:

$$I_o = \left[\frac{(\frac{W}{L})_1}{(\frac{W}{L})_3}(2\sqrt{I_{b2}} - \sqrt{I_{b1}})\right]^2 \tag{9}$$

Equation (9) shows that output current I_o is not PVT sensitive and can be determined by I_{b2}, I_{b1}, and dimensions of M_1 and M_3. According to (9), by increasing I_{b2}, we can have a larger DC output current in the output transistors (M_1, M_2). Using this feasibility, we can relocate the pole at the gate of the pass transistor and send it to higher frequencies by decreasing the small-signal impedance. For this reason, two adaptive current sources (I_{ab2} and I_{ab3}) have been added to this stage's bias circuit to change the I_o with respect to the output current of proposed regulator. We will explain this method in the following parts.

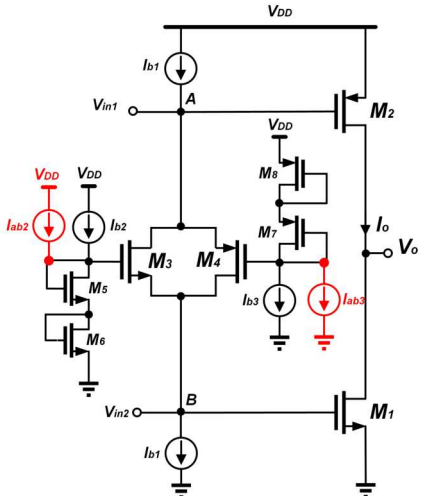

Fig. 3. Proposed class-AB output stage.

As mentioned before, node A or B is the input of this stage. Using the small-signal analysis, assuming $g_i R_o >> 1$, the input impedance at these nodes can be described by:

$$R_{in} = \frac{g_{m4}}{g_{m3} + g_{m4}} R \tag{10}$$

Where the R is equivalent small-signal resistance of I_{b1}. It can also be shown that, if an input current signal (i_{in}) is applied to the A or B, the small-signal voltage at these nodes, can be described by:

$$v_A = v_B = \frac{R}{2} i_{in} \tag{11}$$

Where v_a and v_b are small-signal voltages at A and B, respectively and i_{in} is the input current signal at A or B. From (10) and (11), it is evident that the input impedance

and small-signal voltage at *A* and *B* are equal, and we can use this structure as a push-pull stage. Another major advantage of this structure is that it can be implanted in the output of a folded-cascode stage, as shown in Fig. 7, making the design procedure easier and improving the circuit in terms of power. In the proposed scheme the bias current sources (I_{b1}) have been replaced with M_{10}, M_{12}, and M_4, M_6 from RFC.

B. Output current sensing and adaptive biasing circuit

As discussed before, in this work dynamic biasing technique has been employed to alleviate the power-speed tradeoff and provide a fast-transient for the system by only boosting the bias current during the transition period. Nevertheless, the dynamic biasing technique fails to provide good power supply rejection (PSR) in the active mode because of limited bandwidth. An adaptive biasing circuit has been designed and utilized to address this issue and improve transient and frequency responses. In some previous works to improve transient response, the adaptive biasing technique has been used exclusively [9]. To achieve this, the amount of bias current changes must be a large amount, which results in gain decreasing, and according to (1) and (2) the line and load regulation and low-frequency PSR starts to deterioration. In this work, thanks to dynamic biasing, we do not have to create significant changes in the bias current via adaptive biasing, resulting in small changes in DC gain. The main idea of utilizing adaptive biasing in this work is to enlarge the system's gain-bandwidth product and relocate the poles at the high impedance nodes to a higher frequency by decreasing the impedance and increasing transconductance of the stages. Fig. 4 depicts the circuit fulfillment of the adaptive biasing. Current sensing transistor M_{a1}, which is a replica of M_p with *N:1* ratio, senses the output current via the gate voltage of M_p and with respect to the drain current of M_p, changes the bias current of the current mirror transistors ($M_{a2\text{-}10}$). In this way, $M_{a7\text{-}a8}$ and $M_{a9\text{-}a10}$ change the bias current of the first and second stages of the error amplifier, respectively and form the adaptive current sources.

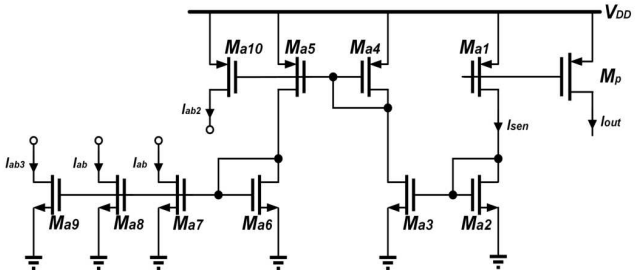

Fig. 4. Proposed output current sensing and adaptive biasing circuit.

C. Stability analysis

In this article, a novel compensation method has been designed and employed because of using a specific three inverting gain stages in the structure of the system. Fig.5 depicts the block diagram model of the proposed LDO regulator, where the proposed circuit has been modeled as a three-stage amplifier by considering the power transistor as the third stage. As shown in Fig.5, the structure consists of two feedback loops implementing voltage buffer compensation and cascode compensation in the outer loop and inner loop, respectively. In the block diagram model g_{m1}, g_{m2} and g_{m3} stand for transconductance of the gain stages, and R_1, R_2 , and R_3 show the output resistance of the first, second and third (output) stages, respectively. Also, C_1, C_2, and C_3 represent the parasitic capacitor of the first and second stages and summation of the parasitic capacitor at the output node and load capacitor, respectively. In the illustrated block diagram g_{c1}, C_{m1} and R_o show transconductance, compensation capacitor, and output resistance of voltage buffer feedback loop, respectively. Also, in the inner loop g_{c2}, $1/g_{c2}$, and C_{m2} represent the transconductance, input impedance, and compensation capacitor of the cascode compensation loop. The compensation strategy in this method is pole-splitting and generating left half-plane (LHP) zeros to improve the stability and gain-bandwidth product. As mentioned before, we applied the adaptive biasing technique to relocate the poles to the higher frequency by decreasing the impedance at critical nodes to enlarge gain-bandwidth production.

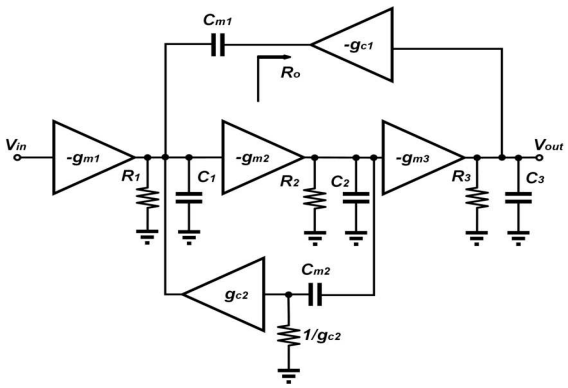

Fig. 5. Block diagram of the proposed LDO.

To provide an accurate analysis, a small signal model of the proposed system, has been illustrated in Fig. 6 . Assuming $g_iR_i>>1$ and $C_3>>C_{m2}$, C_{m1}, the open-loop transfer function of the system can be described as:

$$A(s) = A_{dc}\frac{1+b_1 s+b_2 s^2}{1+a_1 s+a_2 s^2+a_3 s^3+a_4 s^4+a_5 s^5} \tag{12}$$

Where A_{dc} (= - $g_{m1}g_{m2}g_{m3}R_1R_2R_3$) (13) is the dc gain of LDO and:

$$b_1 = \frac{C_{m1}R_o g_{c2}+C_{m2}}{g_{c2}}, \qquad b_2 = \frac{C_{m1}C_{m2}}{g_{c2}}$$

$$a_1 \approx C_{m1}R_1R_2R_3R_o g_{m2}g_{m3}g_{c1},$$

$$a_2 \approx C_{m1}C_{m2}R_1R_2R_3R_o g_{m2}g_{m3}g_{c1}g_{c2}^{-1},$$

$$a_3 \approx C_3C_{m1}C_{m2}R_1R_2R_3R_o g_{m2},$$

$$a_4 \approx C_1C_3C_{m_1}(C_2+C_{m2})R_1R_2R_3R_o,$$

$$a_5 \approx C_1C_2C_3C_{m1}C_{m2}R_1R_2R_3R_o g_{c2}^{-1} \tag{14}$$

Since a LDO regulator is expected to sustain its stability for full load current range, the system's transfer function is derived individually for three different operating regions; light load, medium load, and heavy load. The dominant pole for all loading conditions is equal and is estimated by:

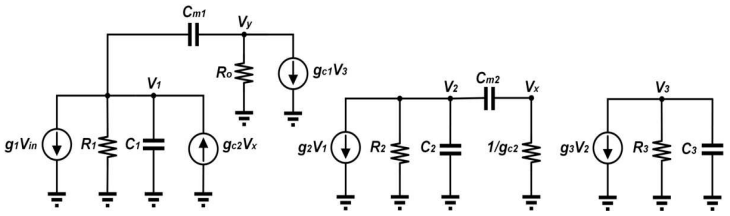

Fig. 6. Small-signal model of the proposed compensation topology.

$$\omega_{p1} = -\frac{1}{C_{m1}R_1R_2R_3R_o g_{m2}g_{m3}g_{c1}} \tag{15}$$

In the stability analysis, two non-dominant poles appear in the system and can be described as:

$$\omega_{p2} \approx -\frac{g_{m3}g_{c1}}{g_{c2}C_3},\ \omega_{p3} \approx -\frac{g_{m2}C_{m2}}{C_1(C_2+C_{m2})} \tag{16}$$

To guarantee stability, we have to comply with the following condition:

$$\omega_{p1} << 2\omega_{p2} << 4\omega_{p3} \tag{17}$$

As it can be seen from (16) and (17), there is a chance, by increasing the output current and by its nature g_{m3}, the non-dominant second pole (ω_{p2}), gets too close to the third pole (ω_{p3}) and causes instability of the whole system. To unravel this problem adaptive biasing technique has been deployed to relocate ω_{p3} to higher frequencies by increasing g_{m2}. Due to the movement of two non-dominant poles towards higher frequencies, it is possible to transfer the dominant pole towards higher frequencies and increase the system bandwidth, which the adaptive biasing technique has done in this work. Before providing transfer function for different load conditions, it is worth mentioning that, one of the zeros has been canceled by a pole, and another zero of the system can be approximately described by:

$$\omega_{z1} \approx -\frac{1}{C_{m1}R_o} \tag{18}$$

Also, the unity-gain frequency can be obtained by:

$$\omega_{GBW} \approx A_{dc}\omega_{-3dB} = \frac{g_{m1}}{C_{m1}R_o g_{c1}} \tag{19}$$

In the light load condition, the power MOSFET is in weak inversion and one non-dominant pole is near to unity-gain frequency and other non-dominant poles and zeros are far away from unity-gain frequency, so we can describe the transfer function as follows:

$$A(s) \approx A_{dc}\frac{1}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} \tag{20}$$

Where A_{dc}, ω_{p1}, and ω_{p2} are mentioned in (13), (15), and (16), respectively.

For full and medium load conditions, as the output current increases, the power transistor enters the saturation region. In this case, the non-canceled zero of the transfer function places between two non-dominant and dominant poles and improves the phase margin of the system. The transfer function of the system can be rewritten as:

$$A(s) \approx A_{dc}\frac{1+\frac{s}{\omega_{z1}}}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})(1+\frac{s}{\omega_{p3}})} \tag{21}$$

Where A_{dc}, ω_{p1}, ω_{p2}, ω_{p3}, and ω_{z1} are mentioned in (13), (15), (16), and (18), respectively.

IV. Simulation Results

The proposed on-chip LDO regulator is designed and simulated in TSMC 0.18 µm CMOS technology. According to the simulation results, the proposed regulator has an acceptable performance in load currents from 10 µA to 10 mA with an output voltage of 1.8 V. By using an adaptive biased super class-AB error amplifier, the open-loop gain of the regulator is increased up to 97 dB and 102 dB in full-load and no-load conditions, achieving an almost constant gain which is resulted in an outstanding line and load regulation. Using the dynamic biasing technique, despite low quiescent current (1.99 µA), the system recovers the output voltage in 1.35µs. TABLE I summarizes the simulated loop gain frequency response of the proposed regulator in different process corner cases and temperature variations for load currents of 10 µA and 10 mA. As it can be seen, the proposed LDO regulator is stable over PVT variations and different load conditions. The simulated load transient responses with an output capacitor of C_L=10 pF is shown in Fig. 9, where the load current is changing from 10 µA to 10 mA with the rise and fall times of 500 ns. Fig. 10 shows the performance of the method that has been introduced in this work to employ the adaptive and dynamic biasing technique. As it can be seen, the bias current of M_{3f} changes with respect to output voltage changes dynamically, and output current changes adaptively.

TABLE I. Simulated frequency response in different conditions.

I_{Load} = 10µA			
Process	FF@ -40° C	TT@ 27° C	SS@ 85° C
DC gain (dB)	102.18	102.13	102.08
ω_{GBW} *(KHz)*	125.38	123.36	125.22
PM (°)	65	63	60
I_{Load} = 10mA			
Process	FF @-40° C	TT @27° C	SS@85° C
DC gain (dB)	117.89	97.71	86.52
ω_{GBW} *(KHz)*	1215.2	970.8	887.8
PM (°)	60	52	44

Finally, TABLE II illustrates the performance comparison between the proposed LDO regulator and several previously reported LDO regulators. The figure-of-merit (FoM), used in previous works, compares different structures in terms of quiescent current, recovery time, and maximum output current.

$$FoM = T_R.\frac{I_Q}{I_{L\max}} \tag{22}$$

A lower value of this FoM implies a better transient performance. It should be mentioned that the circuit-level

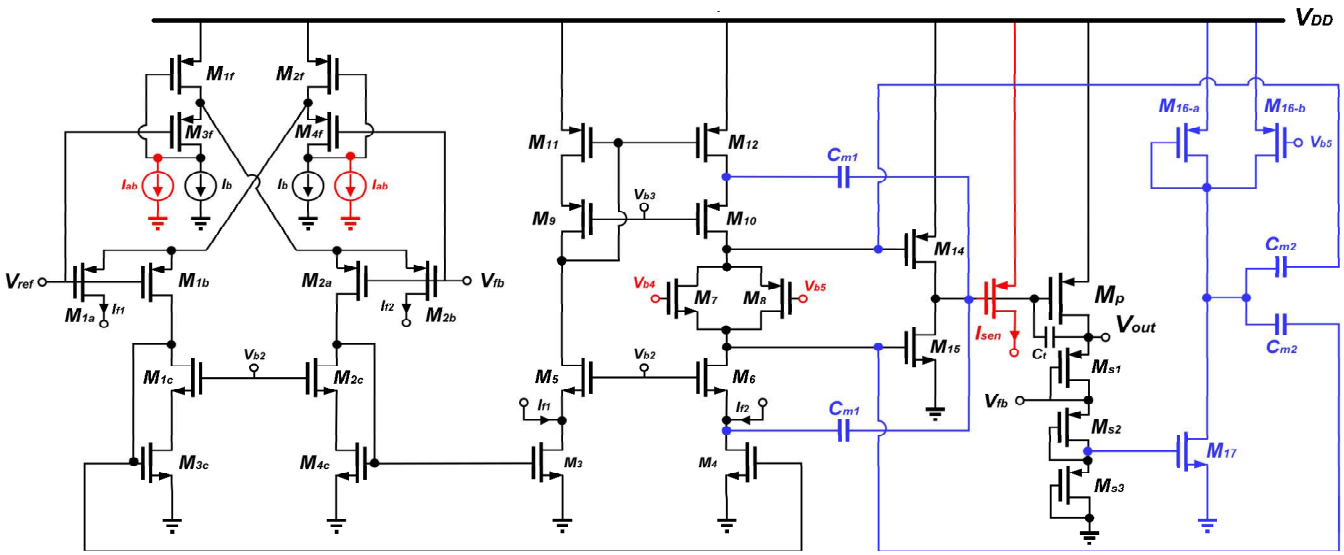

Fig. 7. Circuit realization of the proposed LDO regulator.

simulation results of the proposed LDO regulator are reported here, while some of the references listed in TABLE II are reporting the measured results, and this is not a fair comparison.

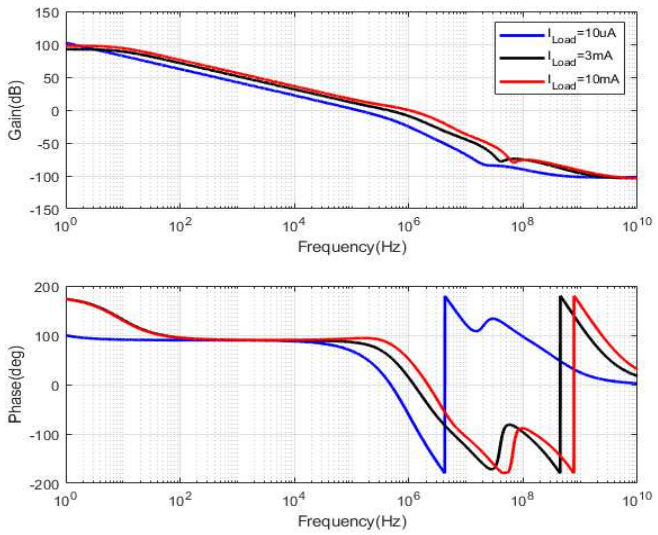

Fig. 8. Frequency response of the proposed LDO.

V. CONCLUSION

In this paper, a new high-gain and low-power LDO regulator has been proposed. A three-stage error amplifier is utilized, and the loop gain of the regulator is increased by using a class-AB input recycling folded-cascode amplifier in the first stage. To lower recovery time, an adaptive biased class-AB stage is used to charge and discharge the parasitic capacitor of the pass transistor independently of the bias current. Finally, because of the specific structure of the proposed system, a new compensation technique has been designed and utilized to ensure the stability of the regulator in various conditions and to enlarge the gain-bandwidth product of the system in full-load condition with an almost constant gain. Simulation results verify the usefulness of the proposed regulator, and hence, it can be used in implantable biomedical applications where ultra-low power consumption is necessary.

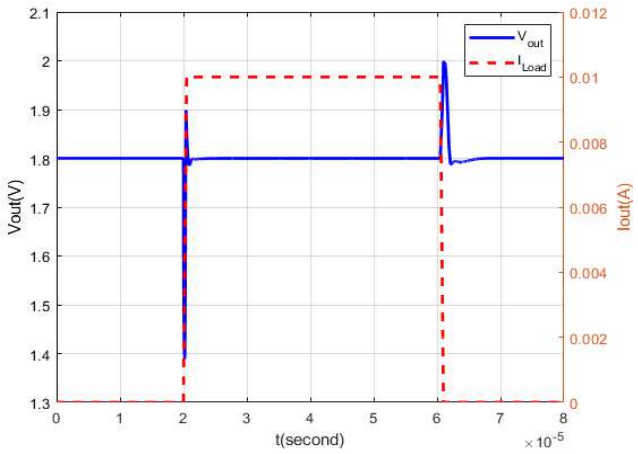

Fig. 9. Simulated transient response with C_L=10 pF @ V_{DD}=2 V for current pulse from 10 µA to 10 mA with 0.5 µs rise and fall time .

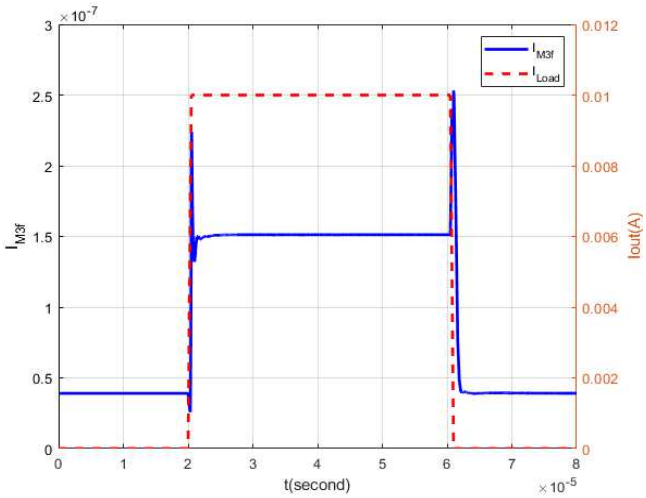

Fig. 10. Current of I_{M3f} in transient state.

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TABLE II.
PERFORMANCE SUMMARY AND COMPARSION WITH STATE-OF-THE-ART FULLY-ON-CHIP LDOS.

Reference	This work	TCASII'19 [2]	TCASI'14 [4]	ISSCC'17 [6]	ISSCC'17 [5]	AICSP'11 [8]	TPEL'20 [1]	AICSP'19 [3]
Technology (µm)	0.18	0.028	0.13	0.065	0.065	0.18	0.065	0.18
I_{Lmax} ***(mA)***	10	20	5	12	0.05	4	100	100
V_{DO} ***(mV)***	200	50	200	50	50-100	300	150	100
I_Q ***(µA)***	1.99	33	99.04	3.2	0.41	28	14	42
T_R ***(µs)***	1.35	0.22	0.16	5	20	1.6	3.2	2
PSR (dB) @ freq.	-66 @ 100Hz	-24 @ 1MHz	-57.11 @ 1MHz	N/A	-22.9 @ 1MHz	-37 @ 1MHz	-33 @ 1kHz	-46 @ 1kHz
LNR (mV/V)	3	17.5	N/A	N/A	N/A	0.24	12	2.3
LDR (µV/mA)	20	260	N/A	N/A	200000	175	90	1
FoM (ns)	0.26	0.36	3.16	1.33	164	11.2	0.448	0.84

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