# A 2.2GHz High-Swing Class-C VCO with Wide Tuning Range

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*Abstract*— **In this paper a novel bias scheme for Class-C oscillators is presented. As a proof of concept, an integrated voltage-controlled oscillator (VCO) with a 1.82–2.65 GHz tuning range is designed in a 0.18 µm CMOS technology. The VCO current consumption is 5.5 mA from a single 0.9 V power supply and achieves a low phase noise throughout the frequency range. The simulated phase noise at 1 MHz offset from the carrier frequency of 2.2 GHz is -126 dBc/Hz.**

## I. INTRODUCTION

Due to the thriving development of the wireless standards in the recent years, interest in utilization of transceivers capable to operate at different frequencies has been widely increased. Oscillators, as an essential building block of the communication systems, are not excepted from this rule. Operating at wide tuning range, associated with low phase noise and power consumption having a small chip area are the main requirements to design an oscillator. Ring oscillators may simply achieve the wide tuning range; however their applications are recognized to be limited because of their poor phase noise. Alternatively, switching techniques have been recently used to overcome this drawback in inductance-capacitance (LC) oscillators [1-8]. Furthermore, several circuit alternatives have been proposed to improve the performance of integrated VCOs.

Differential pair (Cross-Coupled) oscillators have been generally recognized superior over other topologies due to their ease of implementation, lower power consumption and differential operation. However in these oscillators, the noise generated by the active devices considerably degrades the phase noise. In [9], a tail current-shaping circuit technique is proposed with an inherent synchronization mechanism to improve the phase noise in a differential pair LC VCO, which requires only a capacitor parallel to the tail current source. To reduce the contribution of the tail current source in the phase noise, different filtering and noise cancellation techniques have been reported as well [10-12]. One can enumerate the main problems of the tail current filtration techniques as: consuming a larger chip area or using additional off-chip passive components. Noise cancellation techniques, on the other hand, are able to cancel only the contribution of flicker (1/f) noise, leaving the thermal noise unaffected. Among other topologies, Colpitts oscillator has better cyclostationary noise properties, potentially leading to lower phase noise [13, 14]. However, these single ended oscillators are rarely used because they are sensitive to the parameter variations and common-mode noise source and also consume lots of power for a reliable start-up. Herein, a class-C topology which is the optimal evolution over both differential pair and Colpitts oscillators has been employed. This topology can improve the phase noise performance and provide a fully differential output.

In class-C oscillator, a bias network is included; so that the core transistors operate in the active region and allow the voltage swing at the drains to grow to an adequate level, consequently optimize the phase noise performance [15]. However in this topology, the tail capacitor will limit the output swing and therefore the phase noise would not reach its minimum value. In this paper, a novel bias scheme for Class-C LC oscillators is presented to minimize the phase noise. Section II describes the novel bias architecture for class-C LC oscillators. Simulation results are given in Sect. III followed by the conclusion in Sect. IV.

## II. PROPOSED ARCHITECTURE

### A. Bias Scheme for Class-C VCO

In the RC biased class-C topology, shown in Fig 1(a), the output swing is not permitted to switch rail to rail due to the tail capacitor. Maximizing the output swing will remarkably degrade the phase noise in this configuration. To maximize the output swing, the current source and tail capacitor are omitted and a current mirror is used to bias the oscillator as shown in Fig 2. Diode connected transistors create a low-impedance biasing network at the cross-coupled transistor's gate ($M_3$ and $M_4$ mirror the current in $M_1$ and $M_2$). This design does not need any extra voltage to bias the gate of the switching transistors and allows avoiding the use of resistors which, for large impedance values needed, would consume large chip area. In order to remove the noise of the current source completely, it is not possible to use a small capacitor at the gate of the switching transistors. To have a good

978-1-61284-857-0/11/$26.00 

coupling of the output signal to the gate, the gate-source capacitance, $C_{gs}$, of the bias transistors ($M_3$, $M_4$) must be kept quite small. Therefore, the dimensions of the bias transistors are kept minimum in this design. Since no current-biasing tail transistor is used, $M1$ and $M2$ are allowed to switch rail-to-rail thus the output voltage swing is maximized, reducing the phase noise and also, $M1$ and $M2$ experience deep turn-off as their gates reach zero voltage. Deep turn-off is desired to eliminate all unused active devices when they are at off-state, so as to reduce the noise source of the circuit. Furthermore, using the proposed high-swing oscillator, allows us to use smaller power supplies. As shown in Fig 3, by increasing the current in both of the oscillators in Figs. 1(a) and 2, the output swing will be increase. In the presented topology, it is possible to get higher output swing; of course in higher power consumption. Therefore the phase noise in proposed topology is lower than RC-biased class-C introduced in [15]. Employing diode-connected transistors with this type of bias network will consume less area than employing inductors to perform the inductive coupling as shown in Fig 1(b).

### *B. Frequency Tuning*

In order to tune the oscillator over a wide frequency range, a large capacitance variation is required. A low-gain VCO is often desirable to minimize the AM–PM noise conversion due to noise on the control voltage. It is common to use a bank of switched MIM capacitors and a small varactor to cover a wide frequency range in a low-gain VCO. Therefore, a 4-bit binary weighted bank of switched capacitors has been used in this design for the coarse frequency tuning. For fine tuning, small nMOS varactors have been used. Fig. 4 shows the detailed schematic of switched capacitors bank. In this bank in order to reduce the ohmic losses when the switch is on, large size switches are used while resistors are used when the switch is off to reduce the parasitic junction capacitances of the main switches. $B_3B_2B_1B_0$ is a 4-bit control word of the capacitor bank and $V_{ctrl}$ is the varactor control voltage as it changes from 0 to 0.9 V for all coarse tuning bits. Because the middle of the varactor C-V characteristic occurs for a gate-source bias of about 0 V, each varactor is ac-coupled to the tank via a series MIM capacitor and its gate is biased at $V_{dd}/2$.

## III. Simulation Results

The circuit is simulated with a standard CMOS 0.18$\mu$m technology, oscillates at 1.82-2.65GHz. The tank inductor is realized as a 2.6 nH octagonal center tap on a 2 $\mu$m thick top metal layer, with Q= 12 at 2.5 GHz. Fig. 5 shows the Layout of the proposed high-swing class-C VCO. Fig. 6 presents the transient response of the signals at the drain and gate of the $M_1$ transistor. Since no current-biasing tail transistor is used, $M_1$ and $M_2$ are switched rail-to-rail. Thus the tank output voltage swing is maximized. In Fig. 7 the post layout simulated frequency range is shown. A 1.82–2.65 GHz tuning range and a very low VCO gain less than 67 MHz/V are achieved. Fig. 8 shows the phase noise versus the offset frequency.

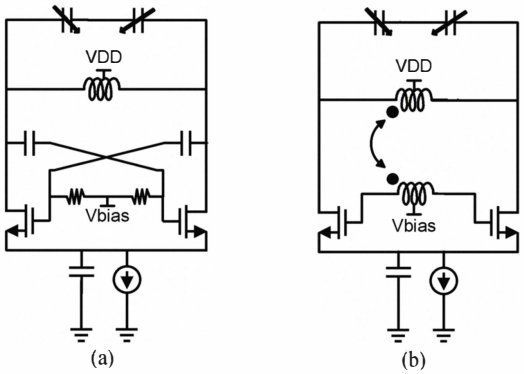


Figure 1. (a) RC-biased and (b) transformer-biased class-C oscillator presented in [15].

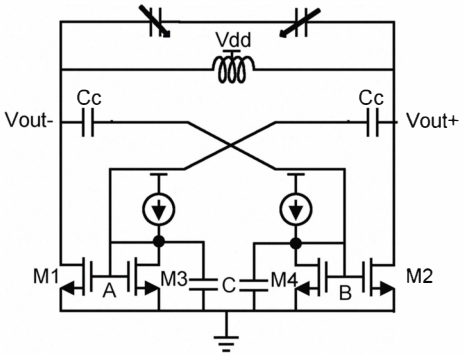


Figure 2. Proposed high-swing class-C oscillator.

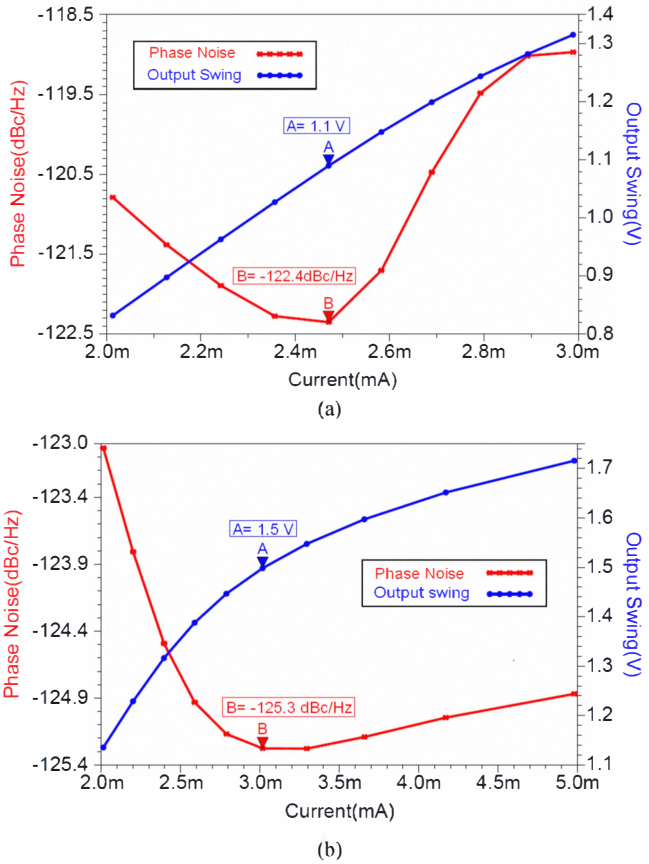


Figure 3. (a) RC-biased class-C and (b) proposed high-swing class-C.

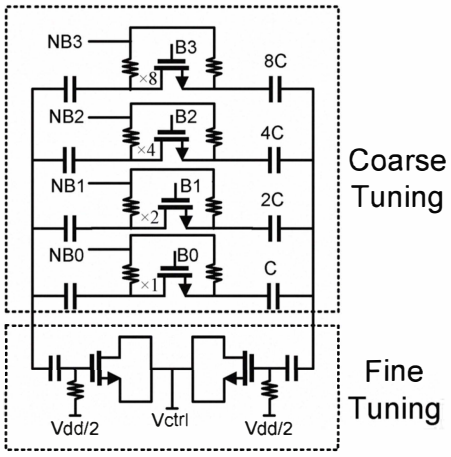


Figure 4. A 4-bit binary weighted switched capacitor bank.

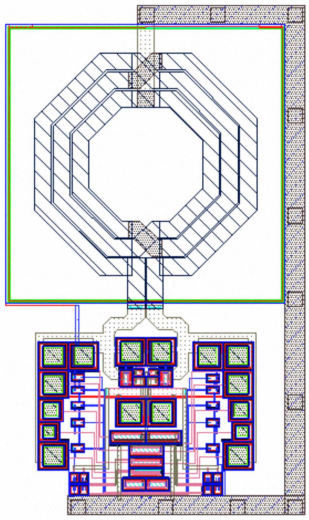

Figure 5. Layout of the proposed high-swing Class-C VCO

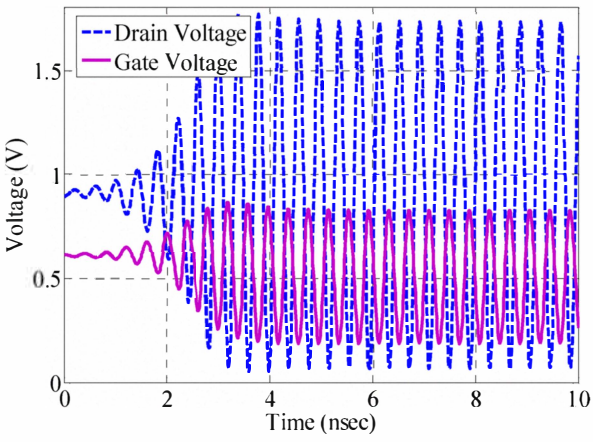


Figure 6. transient response of signals at gate and drain of M1.

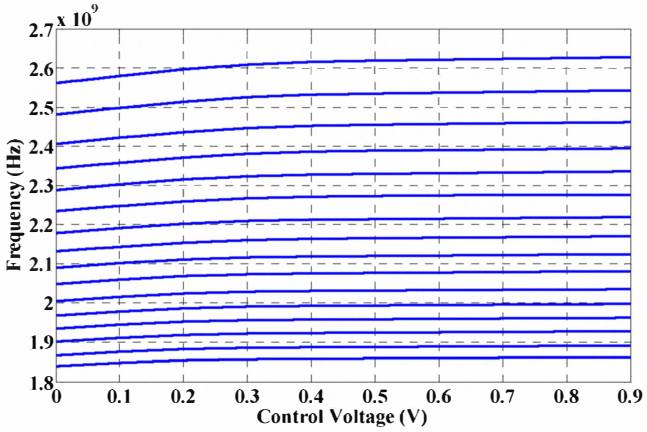


Figure 7. Simulated VCO tuning curves.

The simulated phase noise at 1 MHz offset frequency from a 2.2 GHz carrier frequency is -126dBc/Hz. To compare the performance of our oscillator to recently reported results, we define two figures of merit. First, the figure of merit taking the phase noise performance, frequency and power consumption into account is quoted here as [16]:

$$FOM = 10\log\left(\frac{kT}{P_{DC}}\left(\frac{\omega_o}{\Delta\omega}\right)^2\right) - L\{\Delta\omega\} \quad (1)$$

where, $k$ is the Boltzmann constant, $T$ is the absolute temperature, $\omega_0$ is the carrier frequency, and $L(\Delta\omega)$ is the phase noise at a $\Delta\omega$ offset from the carrier that is expressed in [17]. To take tuning range into account in the comparison of different oscillators, a second figure of merit called *power-frequency-tuning-normalized* (PFTN) as:

$$PFTN = 10\log\left(\frac{kT}{P_{DC}}\left(\frac{\omega_{\max}-\omega_{\min}}{\Delta\omega}\right)^2\right) - L\{\Delta\omega\} \quad (2)$$

was devised. Here, $\omega_{max}$ and $\omega_{min}$ are respectively the maximum and minimum oscillation frequencies. Fig. 9 shows the phase noise at 1 MHz offset frequency across the tuning range and varies less than 2 dB over the tuning range. The performance of the wideband CMOS VCO designed in this work has been summarized in Table I and compared with recent reports in Table II. The presented high-swing class-C VCO exhibits the FoM of -186 dBc/Hz and PFTN of -178 dBc/Hz, which are comparable with those of recent VCOs. It is worth mentioning that the VCOs presented in [8] and [9] also employ capacitor bank technique. However their FoMs are much lower than that of the VCO designed in this work. On the other hand, the topology presented in [15] has a higher FoM, but a quite smaller PFTN than that of the VCO proposed in this paper. Comparing the results summarized in Table II, one would come into this conclusion that there is a conspicuous tradeoff between the Phase noise and tuning range in wide tuning range VCOs. In the present work, for instance, reducing the tuning range to 10% will increase the FoM to -198 dBc/Hz.

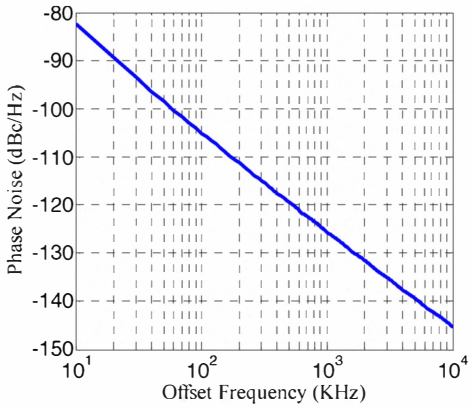


Figure 8. Phase Noise versus offset frequencies

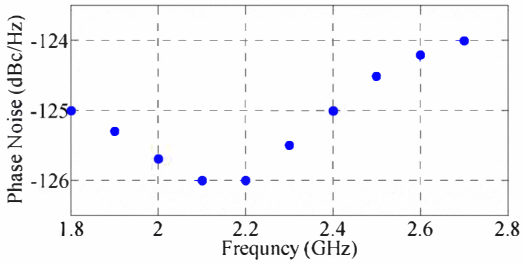


Figure 9. Phase noise at 1MHz offset in each sub-band.

TABLE I. PERFORMANCE OF THE DESIGNED CMOS VCO

| | |
|---|---|
| **Center Frequency** | 2.2GHz |
| **Tuning Rang** | 1.82-2.65GHz |
| **% Tuning Range** | 37% |
| **Phase Noise @Center Freq** | -126dBc/Hz@1MHz |
| **VCO gain(Sensitivity)** | ≤67MHz/V |
| **Power Consumption** | 5mW |
| **Technology** | 0.18µm CMOS |

TABLE II. COMPARISON WITH RECENTLY REPORTED CMOS VCOS

| Ref. No. | Tech. | Cent. Freq. (GHz) | TR (%) | PN@ 1MHz | P (mW) | PFTN (dB) | FoM (dB) |
|---|---|---|---|---|---|---|---|
| **1** | 90nm CMOS | 11.75 | 62 | -106 | 7.7 | 174.4 | 178.5 |
| **2** | 0.18µm CMOS | 2.4 | 20 | -117 | 0.365 | 174.5 | 189 |
| **4** | 0.18µm CMOS | 1.25 | 143 | -101<br>-118 | 6<br>28 | 161.2<br>171.4 | 155.1<br>165.4 |
| **5** | 0.13µm CMOS | 5.5 | 73 | -104 | 1<br>8 | 176.4<br>167.4 | 178.8<br>169.7 |
| **7** | 65nm CMOS | 4.8 | 67 | -115<br>-102 | 24<br>7.2 | 178.7<br>173.4 | 180<br>175 |
| **8** | 0.18µm CMOS | 1.8 | 73 | -126.5 | 10 | 181.6 | 179.2 |
| **9** | 90nm CMOS | 5.6 | 45 | -108.5 | 14 | 165 | 172.3 |
| **15** | 0.13µm CMOS | 4.75 | 10 | -120 | 1.4 | 172 | 192.5 |
| **This work** | 0.18µm CMOS | 2.2 | 37 | -126 | 5 | 178 | 186 |

## IV. CONCLUSION

Design of a high-swing Class-C LC VCO has been reported in a 0.18µm CMOS process. This VCO has a rail to rail output swing, with a wide (37%) tuning range and low- gain VCO. The phase noise at 1 MHz offset from the carrier frequencies of 2.2 GHz is -126dBc/Hz, and also the VCO power consumption is 5mW using a 0.9V power supply.

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