A Wideband Dual-Mode VCO with Analog and Digital Automatic Amplitude Control Circuitry

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Abstract: *In this paper, a dual mode class-C LC voltage controlled oscillator (VCO) has been designed in a 0.18 µm CMOS process. This system is capable to oscillate at two different frequencies, achieving a quite wide 64% tuning range. Depending on the oscillation frequency, the VCO current consumption is automatically adjusted from 4-5.5 mA using a 0.9 V power supply. The phase noise at 1 MHz offset from the carrier frequencies of 2 and 3 GHz are also -125 and -122 dBc/Hz, respectively. A design formula for the tuning range is proposed which considers the ratio of frequency overlap (OL) and all the parasitic effects from band-switching capacitor array and transistors. Furthermore, in order to stabilize the performance through the mentioned tuning range, both analog and digital automatic amplitude control techniques are presented. These amplitude control schemes consume a negligible power and area without degrading the phase noise.*

Keywords: Voltage Controlled Oscillator, Class-C, Wide Tuning Range, Phase Noise, Calibration.

1. Introduction

Due to the thriving development of the wireless standards in the recent years, interest in utilization of transceivers capable to operate at different frequencies has been widely increased. In this respect, research on the compact and power-efficient transceivers supporting multiple wireless standards seems indispensable. Oscillators, as an essential building block of the communication systems, are not excepted from this rule.

Several band switching techniques have been recently used to achieve the wide tuning range in LC oscillators. Switch capacitor banks and switch inductors [1-3] undergo resistive parasitics attributed to the switches which degrade the resonator quality factor and oscillator phase noise. Tunable active inductors have been proposed to achieve a wide tuning range in a small area [4]; however they do not result in low phase noise and power consumption. Furthermore, the design of transformer-based dual-mode VCOs to increase the tuning range has been reported in literature [5]. Utilization of magnetic tuning has also been proposed to increase the tuning range of the LC VCOs by switching extra inductors coupled to the primary ones [6] or by controlling the current in the secondary winding of a transformer [7].

Furthermore, several circuit alternatives have been proposed to improve the performance of integrated VCOs. Differential pair oscillators shown in Fig. 1(a) have been generally recognized superior over other topologies due to their ease of implementation, lower power consumption and differential operation. However in these oscillators, the noise generated by the active devices considerably degrades the phase noise. To reduce the contribution of the tail current source in the phase noise, different filtering and noise cancellation techniques have been reported as well [9-10]. Among other topologies, Colpitts oscillator shown in Fig. 1(b) has better cyclostationary noise properties, potentially leading to lower phase noise [11, 12]. However, these single ended oscillators are rarely used because they are sensitive to the parameter variations and common-mode noise source and also consume lots of power for a reliable start-up.

Herein, a class-C topology which is the optimal evolution over both differential pair and Colpitts oscillators has been employed. This topology, shown in Fig. 2, can improve the phase noise performance and provide a fully differential output. In class-C oscillator, a bias network is included; so that the core transistors operate in the active region and allow the voltage swing at the drains to grow to an adequate level, consequently optimize the phase noise performance [13].

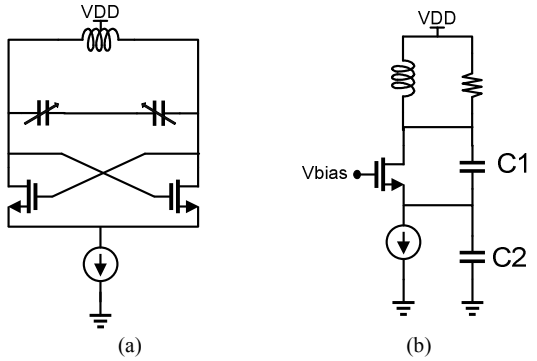

Fig. 1: (a) Standard differential pair VCO, (b) Colpitts VCO

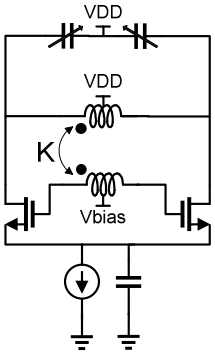

Fig. 2: Schematic of Transformer Biased class-C topology

In the current study, a dual-mode class-C VCO has been presented to overcome the mentioned drawbacks. Since the calibration is a key factor in setting the VCO current at an optimal level in all conditions [14], both analog and digital automatic amplitude control techniques are presented.

The paper is organized as follows. Section 2 describes wide tuning range VCO architecture. Section 3 describes the amplitude calibration circuitries. Simulation results are also shown in Section 4 followed by the conclusion in Section 5.

2. Wide Tuning range VCO Architecture

2.1 Active Core Design

Schematic of the dual-mode class-C VCO considered in this design is shown in Fig. 3. In order to cover a wide frequency range, the desired bandwidth can be broken into two sections and switched capacitor bank can be used to cover each of these sections. As shown in Fig. 3, the separate active circuitries are used to start the oscillations. Depending on the desired frequency range,

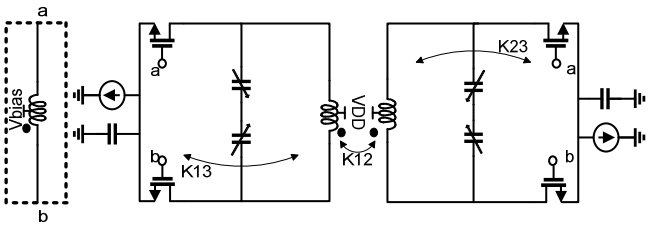

Fig. 3: Proposed Dual Mode class-C VCO

one of the active circuitries is on, while the other one is kept off.

2.2 Transformer Design

To reduce the resonator area, one can place the inductors one inside the other or stack them in different metal layers. Both these configurations lead to a fourth-order resonator with two different resonant peaks. If the coupling factor between the inductors is large, the impedance will have a higher peak magnitude at the lower resonant frequency when looking into each port of this resonator. In such a condition, it will be difficult to sustain the steady-state oscillation at the higher resonant frequency. On the other hand, in case of small coupling factor, the impedance will show a higher peak magnitude at the corresponding resonant frequency [15]. However it is no longer necessary to keep the coupling factors between inductors of resonators and bias inductors in small values. Here ω_1 and ω_2 are the resonant frequencies of the uncoupled tanks that can be expressed as:

$$\omega_1 = \frac{1}{\sqrt{L_1 C_1}} \text{ and } \omega_2 = \frac{1}{\sqrt{L_2 C_2}} \quad (1)$$

The resonant frequencies (ω_L and ω_H) of the fourth-order resonator are the roots of the following equation:

$$\omega^4(K_1^2+K_2^2+K_3^2-2K_1K_2K_3-1)+\omega^2(\omega_1^2(1-K_2^2)+\omega_2^2(1-K_3^2))-(\omega_1\omega_2)^2=0 \quad (2)$$

where ω_1, ω_2 are the resonant frequencies of the uncoupled inductors and K_i (i=1,2,3) are the coupling factors between the inductors. As can be seen in this equation, the resonant frequencies depend on the values of inductors, capacitors and coupling factors. Assuming $\omega_2>\omega_1$ it can be easily shown that: $\omega_H>\omega_2>\omega_1>\omega_L$. The necessary condition to guarantee that only one frequency starts and sustains at each port of the resonator is that the impedance has a larger magnitude at the corresponding resonant frequency as shown in Fig. 4.

Using coupled inductors technique, two different bands with center frequencies ω_L and ω_H ($\omega_L<\omega_H$) can be covered by setting L and C as:

$$\frac{1}{\sqrt{L_1 C_{max}}} \le \omega_L \le \frac{1}{\sqrt{L_1 C_{min}}}, \quad \frac{1}{\sqrt{L_2 C_{max}}} \le \omega_H \le \frac{1}{\sqrt{L_2 C_{min}}} \quad (3)$$

where, C_{min} and C_{max} are the minimum and maximum values of the capacitances in the coarse-tuning section. For overlapping bands, the following criterion should also to be satisfied:

$$\frac{1}{\sqrt{L_2 C_{max}}} \le \frac{1}{\sqrt{L_1 C_{min}}} \quad (4)$$

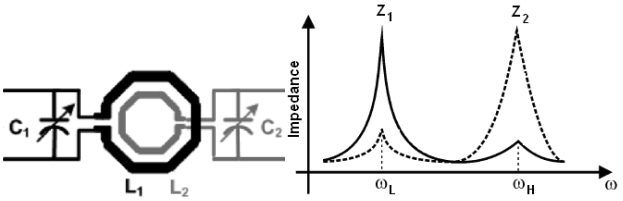

Fig. 4: Coupled tanks and the corresponding impedance responses with small coupling factor

In order to have a dual mode response, the coupling factor should be kept small. Therefore, the aim is to realize multiple inductors in a compact area with small coupling between them. The first possibility is to stack inductors in different metal layers. The Quality factor of the inductors implemented at the lower metal layers will be smaller due to the ohmic loss of the thinner lower metal layers and their proximity to the substrate. Moreover, overlaps between some or all of the turns of multiple stacked inductors will introduce parasitic capacitance that reduces the tuning range. The next possibility is to realize interwound inductors. This solution usually leads to larger coupling between inductors, is undesired in the proposed scheme. In this implementation, the three inductors are placed in a concentric configuration. Each inductor has two turns and realized as a differential spiral inductor with center tap, on a 2.3μm thick top metal layer. As inductors occupy substantial chip area, they can potentially be the source and receptor of detrimental noise coupling. Furthermore, the physical phenomena behind the substrate effects are complicated to characterize. Therefore, decoupling the inductor from the substrate can enhance the overall performance: increase Q and improve isolation [16]. Here a patterned ground shield inserted between on chip spiral inductors and substrate. The shield is realized in lower metal layer which is the closest metal layer to the silicon substrate. The horseshoe pattern consists of U-shaped metal rings placed beneath each turn. Note that there are no closed loops where magnetically induced currents may

flow. Thus, the addition of the shield metal does not affect the inductance. Fig. 5 shows the 3-D views of the coupled inductors and the lumped Π-model. The Coupling factors and quality factors which simulated by means of Agilent Momentum are shown in Fig.6. Physical dimensions of coupled inductors are shown in table I.

2.3 Switched Capacitors Design

In order to tune the oscillator over a wide frequency range within each mode, a large capacitance variation is still required. A low-gain VCO is often desirable to minimize the AM–PM noise conversion due to noise on the control voltage. It is common to use a bank of switched MIM capacitors and a small varactor to cover a wide frequency range in a low-gain VCO. Therefore, a 3-bit binary weighted bank of switched capacitors has been used in this design for the coarse frequency tuning within each mode.

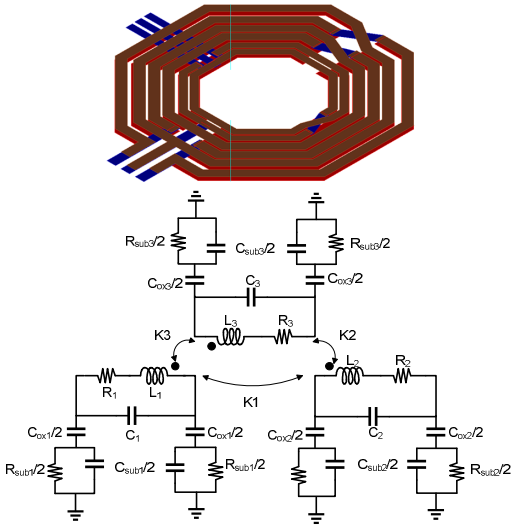

Fig. 5: the side view of triple-coupled inductors and Lumped Π-model used for the triple-coupled inductors

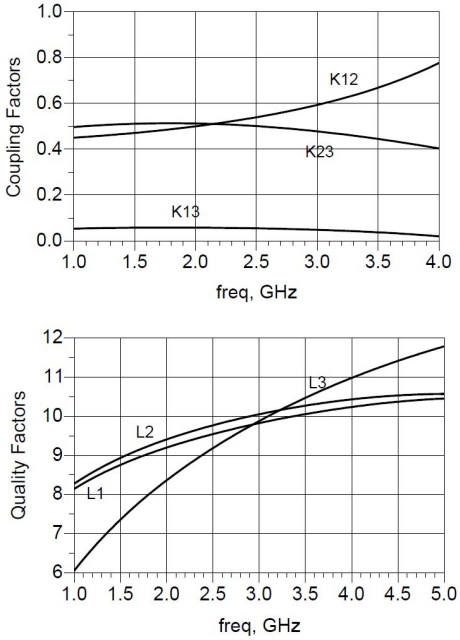

Fig. 6: Coupling and quality factor simulated by Agilent Momentum

TABLE I: DIMENTION OF THREE COUPLED INDUCTORS

	Physical dimensions	Metal Width	Space Between Turns
L1	493μm×493μm	15μm	7μm
L2	382μm×382μm	20μm	3μm
L3	280μm×280μm	20μm	3μm

For fine tuning, small nMOS varactors with minimum channel-length have been used for each mode. Fig.7 shows detailed schematic of Switched capacitors Bank. In this bank in order to reduce the ohmic losses when the switch is on, large size switches are used while small size switches are used when the switch is off [17].

2.4 Design Formula for the Tuning Range

Fig. 8 shows the binary weighted band switching LC tank, which consists of an inductor and capacitor array. The capacitance of the capacitor array comprises the varactor (C_{var}) for the fine tuning of the oscillation frequency, the band select switching capacitor (C_s) for the

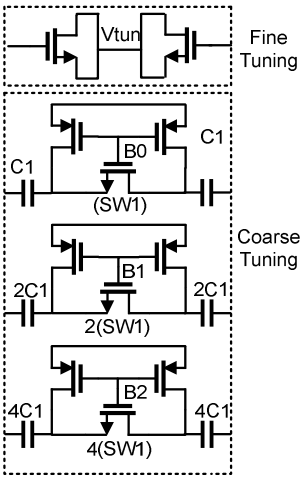

Fig. 7: Detailed schematic of Switched capacitors Bank

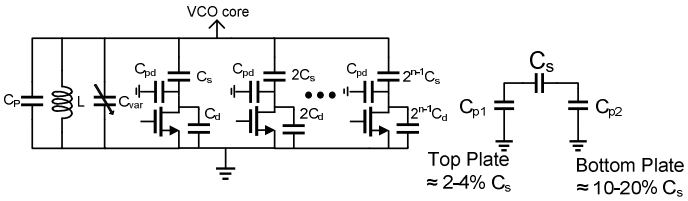

Fig. 8: binary weighted capacitor bank and its parasitics

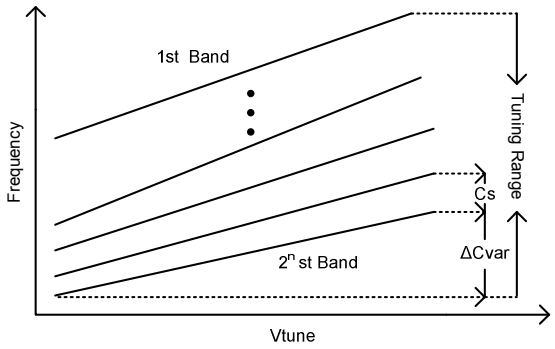

Fig. 9: The tuning characteristic of n-bits band switching

coarse tuning, the parasitic capacitor of the large MOS switch (C_d), the parasitic capacitor of the small MOS switch (C_{pd}) and the parasitic capacitor from VCO core

(C_p). Each capacitor has two parasitic capacitors as shown in Fig 8, Bottom pale and top plate capacitors. Fig. 9 shows the frequency tuning characteristic using a *n*-bit band switching capacitor. The (*OL*) is denoted as the ratio of frequency overlap between the adjacent bands. In order to provide more design insight, C_{pd} and top plate capacitance are omitted. When the switch turns on, the additional capacitances will reduce the original tuning ratio of the varactor. The explicit expressions of the oscillation frequency (f_{osci}) are given as:

$$1^{st}\ Band: f_{osc1} = \frac{1}{2\pi\sqrt{L(C_p + \Delta C_{\text{var}} + (2^n - 1)(C_s \,||\, (C_d + C_{p2})) + (0)(C_s))}}$$

$$2^{nd}\ Band: f_{osc2} = \frac{1}{2\pi\sqrt{L(C_p + \Delta C_{\text{var}} + (2^n - 2)(C_s \,||\, (C_d + C_{p2})) + (1)C_s)}} \quad (5)$$

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$$n^{th}\ Band: f_{oscn} = \frac{1}{2\pi\sqrt{L(C_p + \Delta C_{\text{var}} + (0)(C_s \,||\, (C_d + C_{p2})) + (2^n - 1)C_s)}}$$

Where $\Delta C_{var} = C_{max} \_ C_{min}$, C_{max} is the maximum capacitance of the varactor, C_{min} is the minimum capacitance of the varactor, (C_s||(C_d+C_{p2}) is the parallel capacitor when the band switch turns off and C_s when the band switch is turn on. The oscillation frequency of each sub-band is normalized by the first band to derive the tuning ratio (TR_i). TR_i is defined as the change of capacitance divided by total capacitance in the tank as given in Eqs.6. The overall tuning range (*TR*) is thus expressed as Eq.7.

$$TR_1 = \frac{2\pi\sqrt{L(C_p + \Delta C_{\text{var}} + (2^n - 1)(C_s \,||\, (C_d + C_{p2})) + (0)C_s)}}{2\pi\sqrt{L(C_p + \Delta C_{\text{var}} + (2^n - 1)(C_s \,||\, (C_d + C_{p2})) + (0)C_s)}}$$

$$TR_2 = \frac{2\pi\sqrt{L(C_p + \Delta C_{\text{var}} + (2^n - 1)(C_s \,||\, (C_d + C_{p2})) + (0)C_s)}}{2\pi\sqrt{L(C_p + \Delta C_{\text{var}} + (2^n - 2)(C_s \,||\, (C_d + C_{p2})) + (1)C_s)}} \quad (6)$$

.....

$$TR_n = \frac{2\pi\sqrt{L(C_p + \Delta C_{\text{var}} + (2^n - 1)(C_s \,||\, (C_d + C_{p2})) + (0)C_s)}}{2\pi\sqrt{L(C_p + \Delta C_{\text{var}} + (0)(C_s \,||\, (C_d + C_{p2})) + (2^n - 1)C_s)}}$$

$$TR = (1 - OL)\{(f_{OSC1} \times TR_1) + (f_{OSC2} \times TR_2) + \ldots + \frac{(f_{OSCn} \times TR_n)}{(1 - OL)}\} \quad (7)$$

3. Automatic Amplitude Calibration (AAC) Circuitry

In practice, the small signal transconductance (g_m) is set at a value which guarantees the start up with a reasonable margin under the worst condition, i.e. $g_m R_T(\omega) > 1$ [18].
The frequency dependence in $R_T(\omega) = Q_T.\omega.L$ indicates that this worst situation occurs at the lower end of the desired frequency range. Increasing g_m by this value adversely leads to higher noise contribution. On the other hand, as the frequency increases, the resultant growth in R_T reduces the required g_m value. Thus, in the wideband VCOs which use the transconductors fixed at a predetermined critical state, the g_m in the upper portion of the frequency range exceeds the required value that is a waste of power. Oscillation amplitude is an important design feature and has a significant influence on the neighbor system blocks. In wideband VCOs, large changes in R_T results in a transition from the current-limited to voltage-limited regimes by the increase in frequency [18].

In this paper the design of two different automatic amplitude control circuitry is presented. Automatic amplitude control is desired because without such a circuitry it would be impossible for the designer to set the VCO current at an optimal level over all conditions [14]. The purpose of this design is to create a VCO with wide tuning range, good phase noise and very robust performance over process and temperature variations.

3.1 Analog Automatic Amplitude Calibration Loop

An analog automatic amplitude calibration is used here to set the VCO current at an optimal level over a wide tuning range. Schematic of the proposed amplitude calibration loop composed of peak detector, comparator and current source is shown in Fig. 10. A CMOS peak detector tracks the output of the VCO, so that the measured signal can be used to tune the VCO to the correct amplitude. The peak detector would show a linear response to the resonant frequency variation. This behavior determines the operation of the comparator to recognize which frequency is attributed to a given amplitude. The total area of the inserted detector and comparator should partially contribute the VCO overall size and also their total power consumption should be a small fraction of the VCO total power. The peak detector senses the output swing voltage of the VCO in each mode and the differential pair compares this output with the reference voltage and filters it in a low pass filter for loop stabilization [14]. If the output level of the VCO is larger or smaller than the reference voltage, the current biasing will decrease or increase, respectively.
The main drawback of this solution is the low pass shaped noise in parallel to the VCO tail current. This noise is introduced by AAC loop and can potentially affect the output phase through AM-PM conversion due to varactors. But it is worth highlighting that the AAC loop does not contribute to the wide band noise. In fact the differential pair and current mirror are limited in band, and a noise at 4GHz cannot propagate to the tail generator.

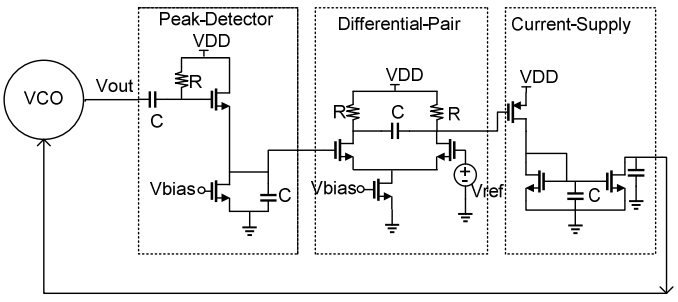


Fig. 10: Automatic Analog Amplitude calibration loop

3.2 Digital Automatic Amplitude Control Circuitry

Another way to control the amplitude is by digital controlled current source. This method has the advantage of being active only when the frequency changes. Furthermore the open loop nature of this control method eliminates any concern of instability. Fig.11 shows the digital controlled current source. A combination of these control bits controls the active core current consumption

too, to optimize the phase noise throughout the frequency range.

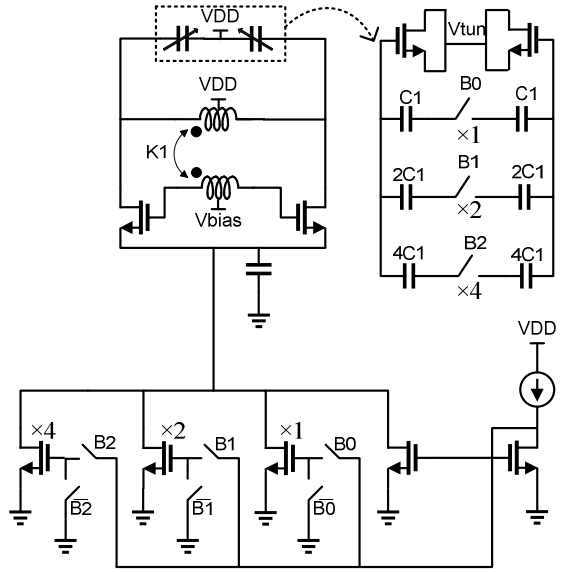


Fig. 11: Digital Amplitude Control Circuitry

4. Simulation Results

The capacitance variation is obtained by combining a 3-bit binary-weighted capacitor array and a MOS varactor. The VCO is simulated in a 0.18µm CMOS technology Fig. 12 shows the phase noise versus the offset frequency at 2 and 3 GHz. In Fig. 13 the simulated VCO frequency range is shown.$B_2B_1B_0$ is a 3-bit control word of the capacitor bank. V_{tune} is the varactor control voltage as i changes from 0 to 0.9 V for all coarse tuning bits and fo the two modes. Modes 1 and 2 are the lower and highe frequency modes of operation which cover 1.7 to 2.5 anc 2.45 to 3.3 GHz frequency intervals, respectively witl about 50 MHz overlap between these modes. The performance of the wideband CMOS VCO designed ir this work has been summarized in Table 1 and compare with recent reports in Table 2. To compare the performance of our oscillator to recently reported results we define two figures of merit. First, the figure of meri taking the phase noise performance and power consumption into account is quoted here as [19]:

$$FOM = 10\log\left(\frac{kT}{P_{DC}}\left(\frac{\omega_o}{\Delta\omega}\right)^2\right) - L\{\Delta\omega\} \quad (8)$$

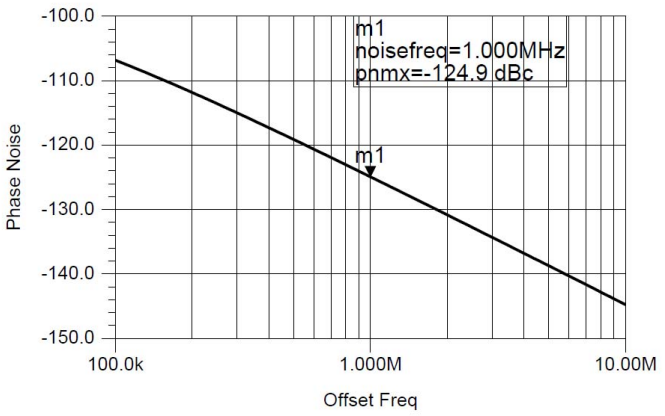
where, k is the Boltzmann constant, T is the absolute temperature, ω_o is the carrier frequency, and $L(\Delta\omega)$ is the phase noise at a $\Delta\omega$ offset from the carrier that is expressed in [20]. To take tuning range into account in the comparison of different oscillators, a second figure of merit called *power-frequency-tuning-normalized* (PFTN)

$$PFTN = 10\log\left(\frac{kT}{P_{DC}}\left(\frac{\omega_{\max}-\omega_{\min}}{\Delta\omega}\right)^2\right) - L\{\Delta\omega\} \quad (9)$$

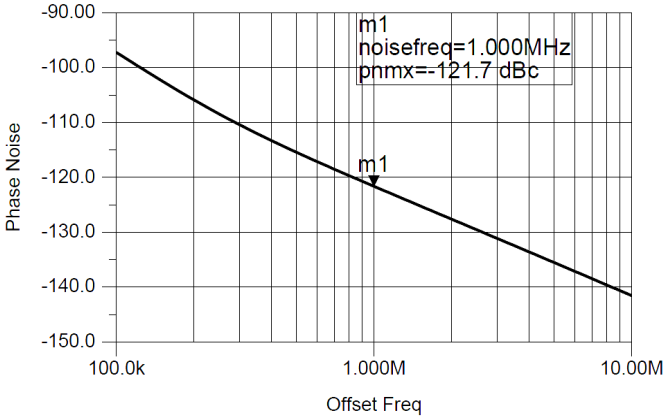
was devised. where ω_{max} and ω_{min} are respectively the maximum and minimum oscillation frequencies. Fig. 14 shows the phase noise performance across the VCO frequency range for calibrated and uncalibrated scenarios. In the uncalibrated case, the bias current is set just high enough to satisfy start-up requirements at the low-end of the tuning range and remains constant. At the upper-end of the tuning range, this results in a tank amplitude that is too large and considerably degrades phase noise, as discussed in Section 3. In the calibrated case, the bias current is effectively scaled down with frequency to maintain the tank amplitude approximately constant, helping to sustain the phase noise performance over the upper-end of the tuning range. The combination of lower phase noise and lower power consumption for the calibrated scenario yield a significantly improved FOM in the upper half of the frequency range.

5. CONCLUSION

Design of a dual mode LC VCO has been reported in a 0.18 µm CMOS process. This system is capable to operate at two different frequencies with a wide (64%) tuning range. The phase noise at 1 MHz offset from the carrier frequencies of 2 and 3 GHz are respectively -125 and -122 dBc/Hz, and also the VCO power consumption is 3.5-5 mW using a 0.9 V power supply. Performance of this VCO is stabilized through the entire tuning range by the means of both analog and digital automatic amplitude calibration circuitries which consumes negligible power and area.



(a)



(b)

Fig. 12: Phase noise versus the offset frequency (a) 2 and (b) 3 GHz

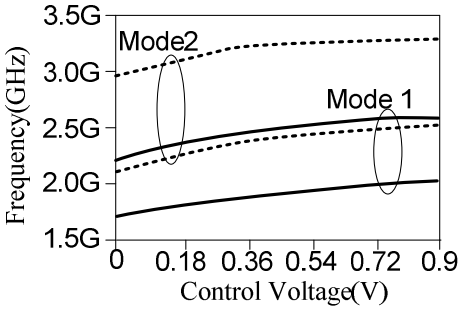


Fig. 13: Simulated VCO frequency range

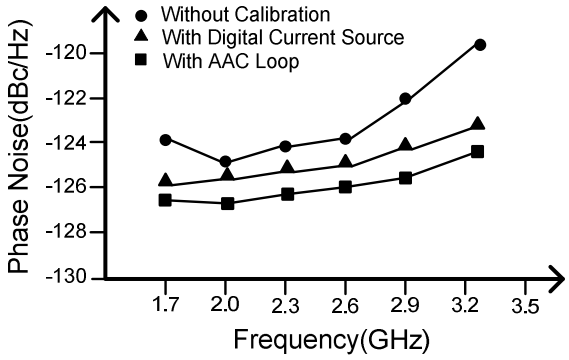


Fig. 14: Phase noise @1MHz for calibrated and uncalibrated cases

TABLE II: PERFORMANCE OF THE DESIGNED CMOS VCO

	Mode 1	Mode 2
Frequency TR (GHz)	1.7-2.5	2.45-3.3
PN@1MHz (dBc/Hz)	-125	-122
Power Consum (mW)	5	3.5
Technology (µm)	0.18	0.18
Supply (V)	0.9	0.9

TABLE III: COMPARISON WITH RECENTLY REPORTED CMOS VCOS

Ref. No.	Tech.	Cent. Freq. (GHz)	TR (%)	PN @1MHz	Power (mW)	PFTN (dB)
1	90nm CMOS	11.75	62	-106	7.7	0.57
2	0.18µm CMOS	2.41	20	-117	0.365	-0.41
4	0.18µm CMOS	1.75	143	-102	6 28	-11.6 -18.3
5	0.13µm CMOS	4.6	69	-104	1 8	1.29 -7.73
7	65nm CMOS	5.25	78	-115 -102	24	-13.4 -0.4
16	0.13µm CMOS	2.28 4.6	128	-117	4.3 9.1	10.4 7.16
17	0.18µm CMOS	1.8	73	-126	10	10.3 4.5
This work	0.18µm CMOS	2 3	64	-125 -122	5 3.5	11.5 9.4

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