

A 10-bit 250MS/s Pipelined ADC With a Merged S/H & 1st Stage Using an Optimal Opamp Sharing Technique

Mohammad Reza Ashraf and Mohammad Yavari

Integrated Circuits Design Laboratory
Department of Electrical Engineering
Amirkabir University of Technology
Tehran, Iran

E-mails: m.r.ashraf@aut.ac.ir, myavari@aut.ac.ir

Abstract—This paper presents a very high-speed low-power 10-bit pipelined ADC in a 90nm CMOS technology. A modified opamp-sharing technique is proposed which enables merging the S/H and first stage with optimum power saving. The new technique saves power by changing the bias currents of the input and output stages of the amplifier. Stage scaling and low power dynamic comparators are also utilized to reduce power consumption more effectively. Using this approach, a 10-bit 250MSample/s pipelined ADC has been designed in a 90nm CMOS technology. According to HSPICE simulation results, the ADC achieves a 54.5dB SNDR with a nyquist-rate, $1V_{p-p,diff}$ input signal while consuming only 29mW with a 1V supply voltage.

I. INTRODUCTION

Rapid growth in digital systems makes analog-to-digital converters (ADCs) the basic building block of every handheld digital device. In these devices, the power consumption is one of the most important issues. Pipeline ADCs are the best choice to use in low power high speed, medium-high resolution applications. These ADCs consist of several similar stages. Every stage converts a part of input signal into digital format and sends the residue signal to the next stage. Multiply-By-Two (MBT) gain stages are widely used as the basic building blocks of every stage. The accurate gain of two is achieved by using an opamp in a feedback loop. Opamps are the most power-hungry blocks of pipeline stages. Several methods have been proposed to reduce the power consumption of these ADCs [1-3]. Opamp sharing technique reduces the power consumption by sharing one opamp between two successive stages. The switched-opamp technique reduces the power consumption by turning the opamp off during the amplification phase. Double sampling technique reduces the power consumption by expanding the available time for settling of the opamp. However, these techniques also suffer from some drawbacks. Opamp sharing and double sampling techniques suffer from an effect called the "memory effect" which is caused because there is no time to reset the input and

output nodes of the opamp. So, the input capacitor of the opamp will not reset and the charge on this capacitor will affect the output voltage of the stage. Also, for switched opamp technique, because the opamp should be turned off during the amplification phase and then turned on for the sampling phase, the settling time of the opamp will increase since it takes some time for the opamp to wake up.

In this paper, a comparison between opamp sharing and double sampling techniques is done. It is shown that the opamp sharing technique is more effective than the double sampling technique in power consumption. However, the opamp sharing technique, itself is not optimum since one opamp is used for two successive stages. So, because of stage scaling, the opamp is not suitable for one of the stages. Also, as the feedback factor is not the same for the S/H and first stage, merging the S/H and first stage cannot be done efficiently. A modified opamp sharing technique is proposed here which enables merging the S/H and first stage of a pipelined ADC.

To verify the effectiveness of the proposed technique, a 10-bit 250MS/s pipelined ADC has been designed and simulated. To achieve low-power and high performance, the stage scaling, gain-boosted two-stage class A amplifiers, and dynamic comparators have also been employed. Simulation results in a 90nm CMOS process with 1V supply voltage show 54.5dB SNDR while consuming only 29mW power.

This paper is organized as follows. Section II reviews the opamp sharing and double sampling techniques and compares these two methods with each other. Section III explains the modified opamp sharing technique. Simulation results are shown in section IV. Section V concludes the paper.

II. REVIEW

In this section, the concepts of opamp sharing and double sampling techniques are reviewed. Then, a comparison between these two techniques is made.

A. Opamp Sharing

The conventional 1.5 bit MDAC is shown in Fig. 1. Φ_1 and Φ_2 are two non-overlapping clock phases as shown in the figure. In phase Φ_1 , the input signal is sampled on both capacitors, C_1 and C_2 . After that, in phase Φ_2 , C_1 is flipped around the opamp and C_2 is connected to the DAC voltage. It is seen that the opamp is not used during sampling phase (Φ_1). In this phase, the opamp's input and output nodes are connected to ground and the opamp will reset. The basic idea behind the opamp sharing technique is that since the opamp is not needed during the sampling phase, it can only be active during the half clock period. That is, as shown in Fig. 2, the opamp can be used for stage N when Φ_1 is high, other wise it can be used for stage N+1.

B. Double Sampling

Double sampling technique takes advantage of the fact that the opamp is not active during sampling phase. The single-ended double sampling circuit of a 1.5 bit MDAC is shown in Fig. 3. As is evident from the figure, existence of two parallel paths with inverse timing makes it possible to take advantage of the opamp in both of two phases. However, this technique suffers from some obstacles. The main problem is the mismatches between the two paths. The problem is more vital about the mismatches between the capacitors since it introduces different gains for the two paths. In addition, this technique adds another series of switches and capacitors which occupies more silicon area.

C. Comparison of Opamp Sharing and Double Sampling Techniques

Opamp sharing and double sampling techniques both

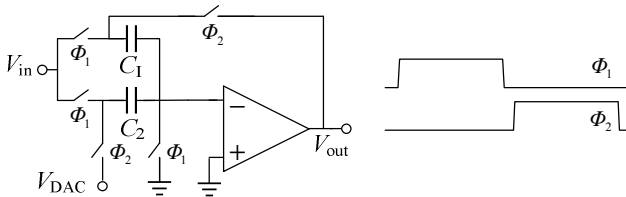


Figure 1: Conventional 1.5-bit MDAC.

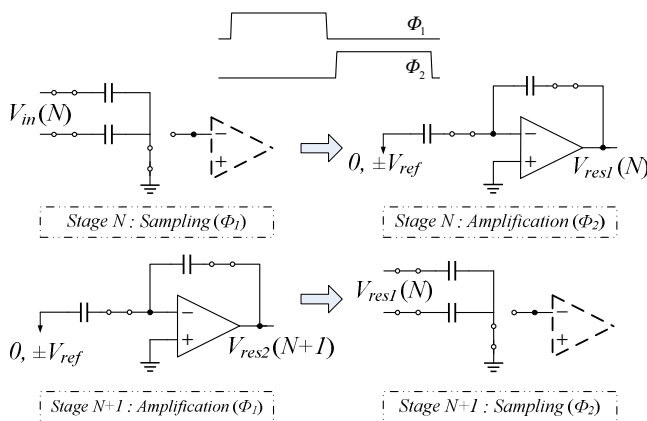


Figure 2: Opamp sharing technique.

reduce the power consumption of a pipelined ADC. However, it is worth comparing the power consumption of these two techniques to evaluate their performances. Consider two consecutive pipeline stages as shown in Fig. 4. Suppose the capacitor scaling is applied to the second stage with a scaling factor of δ . Here, two situations can occur. First, suppose the double sampling technique is applied to both of these stages. In this condition, we have two stages with two separate opamps which their settling times are doubled. Second, suppose the opamp sharing technique is applied to both of these stages. In this case, only one opamp is used for the two stages. A question is raised here that which technique consumes less power. To answer this question it is supposed that a two stage opamp is used for these stages which its second stage current is α times of its first stage current. In this way, the capacitor scaling will not change the input stage current of the opamp and it has a direct relation to the current of the second stage of the opamp. Also the feedback factor of each stage of the pipeline ADC has a direct impact on the current of the input stage of the amplifier. Equations (1) and (2) show the power consumption of the double sampling and opamp sharing techniques with respect to the conventional MDAC structure. As is seen from these equations, the opamp sharing technique saves more power in comparison with the double sampling technique.

$$\frac{P_{op-sh}}{P_{conv}} = \frac{P_{S1,conv}}{P_{S1,conv} + P_{S2,conv}} = \frac{1 + \alpha}{2 + (1 + \delta)\alpha} \quad (1)$$

$$\frac{P_{DS}}{P_{conv}} = \frac{P_{S1,DS} + P_{S2,DS}}{P_{S1,conv} + P_{S2,conv}} = \frac{1 + (1 + \delta)\alpha}{2 + (1 + \delta)\alpha} \quad (2)$$

Figure 5 shows the power consumption of double sampling and opamp sharing techniques with respect to the ratio of the currents of stages (α) with a fixed scaling factor (δ). As shown in the figure, the opamp sharing technique

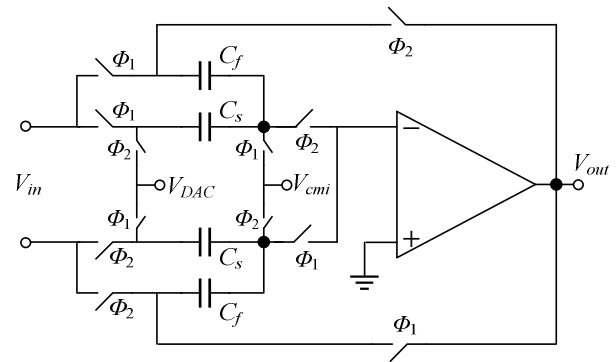


Figure 3: Double sampling technique.

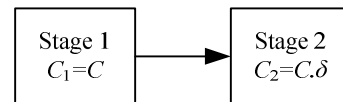


Figure 4: Two successive pipelined stages with scaling factor of δ .

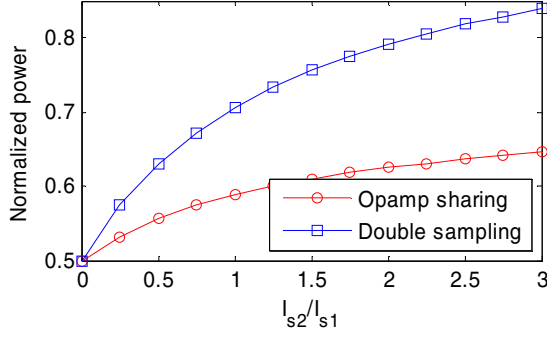


Figure 5: Power consumption of Opamp sharing and double sampling techniques with respect to α .

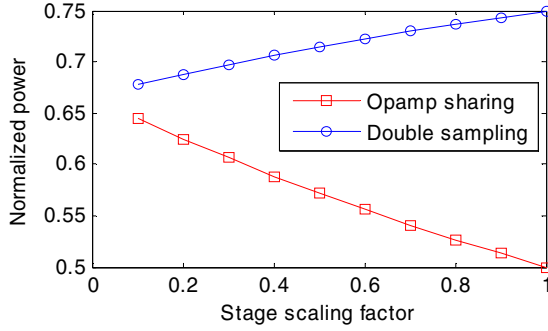


Figure 6: Power consumption of Opamp sharing and double sampling techniques with respect to δ .

saves more power than the double sampling technique. Also, Fig. 6 shows the power consumption of the two techniques with respect to δ with a fixed α . It is clear that the double sampling technique consumes more power than the opamp sharing technique.

III. PROPOSED STRUCTURE

As shown in the previous section, the opamp sharing technique can save more power in comparison with the double sampling technique. In this way, it is better to use the opamp sharing technique for all of the pipeline stages. Fig. 7(a) & (b) shows the schematic of the pipeline stages. However, since the feedback factors of the S/H and first stage are different from each other, the opamp sharing technique cannot be done efficiently for these stages. To solve this problem, a modified opamp sharing technique is used. The modified opamp sharing technique changes the bias current of the input stage of the amplifier, so that the transconductance of the input differential pair changes to meet the requirements for the S/H and first stage. In addition, since the stage scaling affects the bias currents of the output stage of an amplifier, the bias currents of the output stage of the amplifier changes to optimize the power consumption of the amplifier. The proposed circuit is shown in Fig. 8(a) & (b). As is seen, in phase Φ_1 , transistor M_{1b} determines the bias currents, while in phase Φ_2 , transistor M_{1a} sets the bias currents of the input and output stages of the amplifier. Using this technique, a pipelined ADC with a merged S/H and first stage can be designed with optimum power consumption. In addition, the stage scaling can be done more effectively.

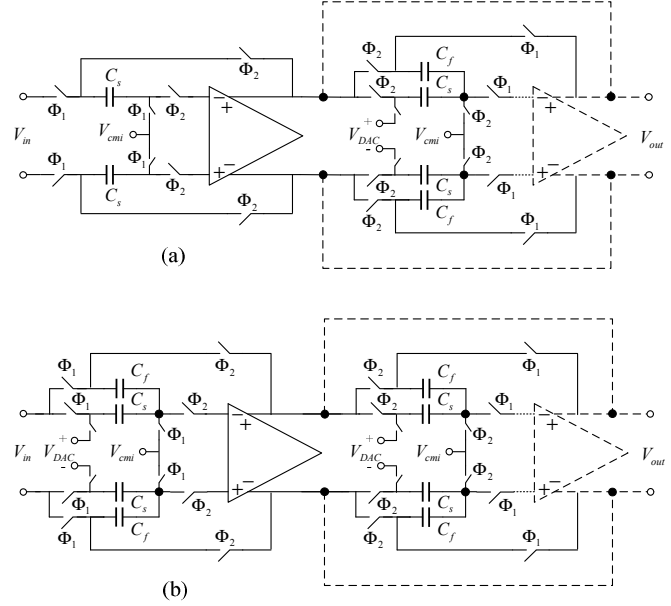


Figure 7: (a) Opamp sharing structure used for the S/H stage and the 1st stage of the pipeline structure (b) Opamp sharing structure used for the stages 2 through 7 of the pipeline structure.

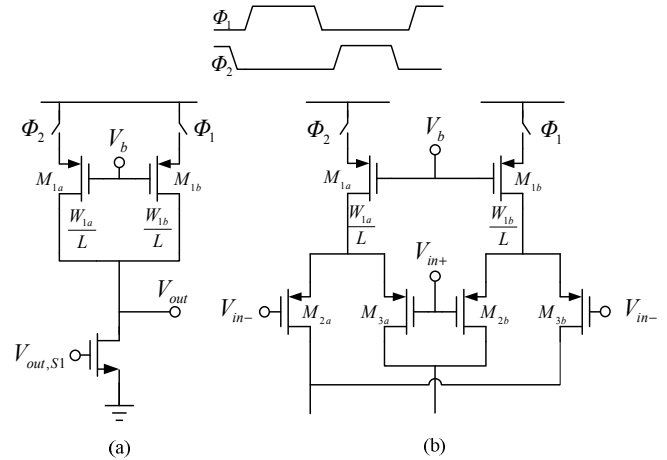


Figure 8: (a) Proposed structure to change the bias current of the output stage of the amplifier (b) Proposed structure to change the bias current of the input differential pair.

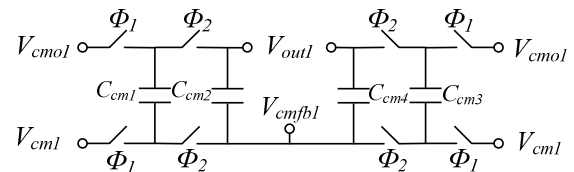


Figure 9: CMFB circuit used to adjust the DC voltage level of the "high-impedance" output node of the amplifier.

IV. SIMULATION RESULTS

To evaluate the effectiveness of the proposed structure, a 10-bit 250MS/s pipelined ADC has been designed in a 90nm CMOS technology with 1V supply voltage. The overall structure consists of an S/H stage following eight 1.5-bit MDAC stages and a 2-bit Flash ADC at the end. The S/H and first stage were merged together using the modified opamp sharing technique. Also, stages 2 through 7 use the opamp sharing technique to optimize the power consumption. Stage 8 remains alone. The stage scaling has been done effectively to reduce the power consumption more efficiently.

A low-voltage low-power two-stage class A hybrid-cascode opamp based on an OTA introduced in [4] is used for the pipeline stages. As the gain of this amplifier is not sufficient for the first 4 stages of the pipelined ADC, gain boosting technique is used to provide the needed gain. Also, in stage 4, the channel length of the output transistors of input and output stages of the amplifier is chosen more than minimal so that its gain would be sufficient. As with the opamp sharing technique, the opamp is active in both two phases, there is no time to reset the opamp's input and output nodes. So, the problem of "memory effect" will be happen. Due to the finite gain of the opamp, a charge is injected in the input parasitic capacitance which never resets. Therefore, the output voltage will be a recursive function of the present and the previous samples. To overcome this problem, two methods have been used. First, the opamps gain is set to be 6dB higher than the required gain for each stage. In this way, the injected charge will be negligible. Moreover, a technique called "FSPI" as introduced in [5] is used to minimize the memory effect of opamp sharing structure. By using these two techniques, the "memory effect" will be reduced to one third. As the output node of the amplifier is a "high-impedance" node, the DC level of the output voltage can not easily be adjusted. For this reason, there should be an auxiliary circuit to continuously adjust the voltage level of this node. A discrete-time CMFB circuit as shown in Fig. 9 is used.

As 1.5-bit conventional MDAC is used, $\pm V_{ref}/4$ offset error can be tolerated by the comparators, where V_{ref} is the single-ended reference voltage. Therefore, a low power dynamic class AB comparator and a switched-capacitor scheme of capacitive dynamic divider are designed to use in the ADC to achieve low power consumption.

The ADC is simulated with HSPICE using BSIM4v4.3.0 model of a 90nm CMOS process. The full scale input signal voltage is $1V_{p-p,diff}$ while the supply voltage is 1V. Reference voltages are chosen 0.25V and 0.75V to meet the requirements of a 1.5-bit conventional MDAC structure. This is as a result of that comparators could withstand $\pm V_{ref}/4$ offset error. Simulation results show that the ADC consumes 29mW power while its SNDR is 55dB and 54.5dB at 34.1796875MHz and at 124.755859375MHz (Nyquist rate) input signal frequencies, respectively. The power spectral density (PSD) of the output of the ADC is shown in Fig. 10. Also, the variations of the SNDR of the output of ADC with the input signal frequency is shown in Fig. 11. In both Figs. (10) and (11), the effect of the circuit noise has not been included. As is evident, the designed ADC is not much sensitive to the input signal frequency.

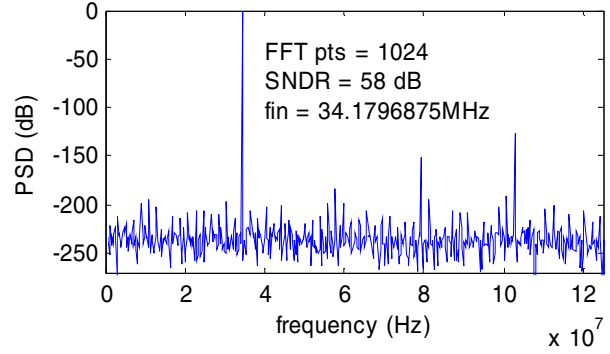


Figure 10: Power Spectral Density of the designed ADC

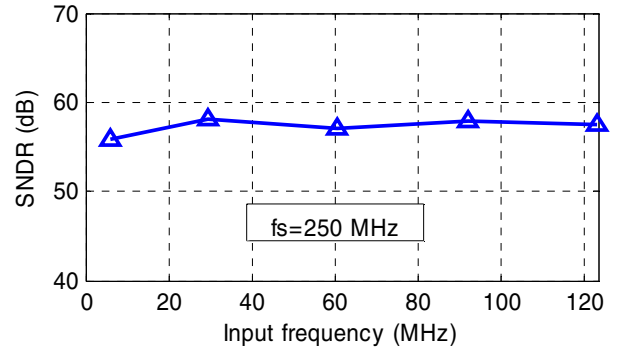


Figure 11: variations of SNDR versus input signal frequency

TABLE I. COMPARISON WITH SOME REPORTED ADCS.

Reference	Tech. (nm)	V_{DD} (V)	F_s (MHz)	SNDR (dB)	Power (mW)	FoM (pJ.V/step)
[6]	90	1.2	500	52.8	55	0.31
[7]	180	1.8	50	58.2	9.9	0.30
[8]	180	1.8	50	64	18.4	0.28
[9]	65	1.2	800	44.2	30	0.28
[10] ^a	90	1	200	58.5	30.9	0.22
This work ^a	90	1	250	54.5	29	0.27

a. Simulation results with a Nyquist rate input signal frequency are reported

Table I summarizes the simulation results in comparison with some recently reported pipelined ADCs. The comparison is based on a figure of merit defined as:

$$FOM = \frac{P}{2^{ENOB} \times f_s} \quad (3)$$

In this table, the circuit noise is also taken into account. As is seen from Table 1, the proposed ADC achieves a reasonable FOM among the reported ADCs. This implies that the proposed opamp sharing technique is an efficient way to reduce the power consumption of a pipelined ADC.

V. CONCLUSION

In this paper, a comparison between the opamp sharing and double sampling techniques was performed. The results show that using the opamp sharing technique along all of the pipelined stages is a more effective way to reduce the power consumption than utilizing the double sampling technique. With this assumption, a low power 10-bit 250MS/s pipelined ADC is designed. Using a modified opamp sharing technique, the S/H and first stages are merged together. The modified opamp sharing changes the transconductance of the input differential pair so that the amplifier will be efficient for both the S/H and first stage. Also, the remaining stages use the opamp sharing technique to optimize the power consumption. HSPICE simulation results of the designed ADC in a 90nm CMOS technology shows an SNDR of 54.5dB while consuming only 29mW with a 1V supply voltage.

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