# A High Speed 1.5-Bit Mismatch-Insensitive Multiplying Digital-to-Analog Converter

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*Abstract*—A new method to reduce the mismatch between the capacitors of a 1.5 bit multiplying digital-to-analog converter (MDAC) structure is presented. The new structure employs two capacitors in series and operates in three phases. Compared to the conventional MDAC structure, the mismatch between the capacitors has a much smaller influence not only on the accuracy of the input signal but also on DAC voltage. Moreover, despite the addition of a phase, the speed of the proposed MDAC is higher than that of a conventional one. Circuit-level analysis and simulation results of the proposed architecture and the conventional structure are presented using a 90nm CMOS technology.

*Index Terms—* Pipelined analog-to-digital conversion, digital-to-analog conversion, switched-capacitor circuits.

## 1. INTRODUCTION

Pipelined analog-to-digital converters (ADCs) are the best choice to use in high speed and medium to high resolution applications. These ADCs consist of several similar stages. Every stage converts a part of the input signal into digital format and sends the residue signal to the next stage. Multiply-by-two (MBT) gain stages are widely used as the basic building block of every stage in 1.5 bit/stage structures. In these configurations, the gain error is mainly caused by the mismatch between the sampling and holding capacitors. Various methods have been proposed to alleviate this problem. Some of them only study the gain error of the input signal [1-6]. Actually these methods are just useful in a MBT structure and if they are to be used in a MDAC structure, the DAC voltage is not transferred accurately. For example, in the method proposed in [3], if $C_1$ and $C_2$ have a mismatch such that $C_2 = C_1(1+\varepsilon)$, then the output voltage will be:

$$V_{out} = 2V_{in} - \frac{C_2}{C_1}V_{DAC} = 2V_{in} - (1+\varepsilon)V_{DAC} \qquad (1)$$

As is seen, the mismatch between the capacitors in the DAC path will directly transfer to the output voltage. In [7] a new structure has been proposed to reduce the effect of mismatch in both input signal and reference signal paths. Despite the accuracy of this technique, the speed of this method has been decreased in comparison to the conventional MDAC. The feedback factor of this structure is less than that of the conventional one. Also, the

capacitive load of this structure has been increased in comparison to the conventional MDAC. In addition, this structure needs a four-input OTA structure that somewhat increases the power consumption of the circuit.

In this paper, a new high speed 1.5-bit mismatch-insensitive MDAC is presented. The proposed technique reduces the effect of mismatch between the capacitors on the output voltage by employing a new technique which uses the series capacitors and avoids using the conventional structure which employs the charge conservation rule. This technique, not only corrects the gain error of the input voltage, but also the DAC voltage. Despite the addition of a phase, the speed of the proposed MDAC is faster than that of a conventional one.

The paper is organized as follows. In Sect. 2, the conventional structure is reviewed. The proposed technique is described in Sect. 3. The effects of circuit non-idealities are studied in Sect. 4. Simulation results are presented in Sect. 5 and Sect. 6 concludes the paper.

## 2. CONVENTIONAL STRUCTURE

Figure 1 shows the conventional structure of a 1.5-bit MDAC. $\Phi_1$ and $\Phi_2$ are two non-overlapping clock phases as shown in the figure. In phase $\Phi_1$, the input signal is sampled on both capacitors, $C_1$ and $C_2$. After that, in phase $\Phi_2$, $C_1$ is flipped around the opamp and $C_2$ is connected to the DAC voltage. In this case, the output voltage will be twice the input voltage minus the DAC voltage. Now, consider a mismatch between these capacitors such as $C_2 = C_1(1+\varepsilon)$, then the output voltage will be:

$$V_{out} = (2+\varepsilon)V_{in} - (1+\varepsilon)V_{DAC} \qquad (2)$$

As is seen, the mismatch between the capacitors affects both the input and DAC voltages and will directly transferred to the output voltage.
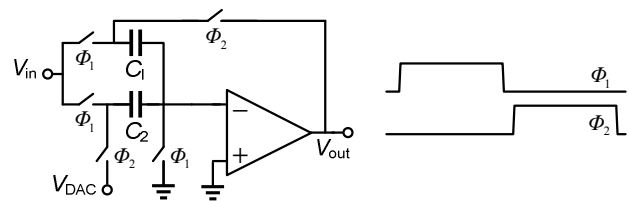


**Figure 1:** Conventional 1.5-bit MDAC.
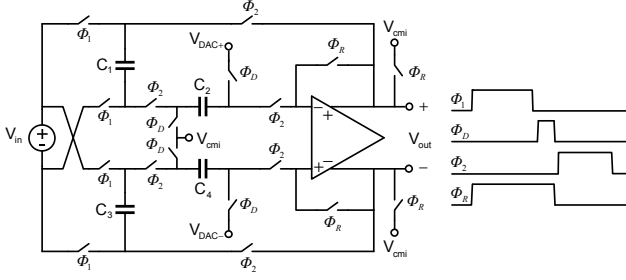
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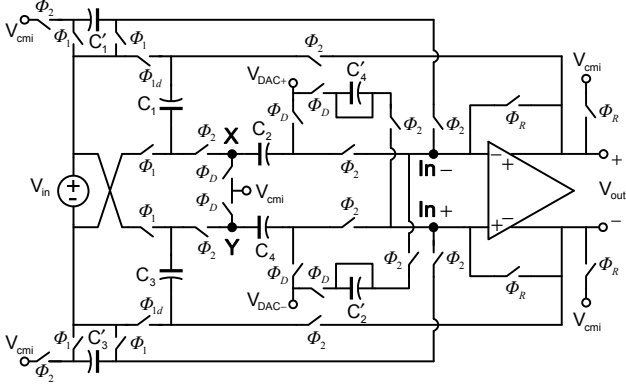**Figure 2:** Proposed 1.5-bit mismatch-insensitive MDAC



**Figure 3:** Proposed 1.5-bit mismatch-insensitive MDAC with parasitic compensation capacitors.

## 3. PROPOSED STRUCTURE

Figure 2 shows a conceptual realization of the proposed mismatch-insensitive MDAC. The MDAC is configured for a 1.5 bit/stage pipelined ADCs. During phase $\Phi_1$, the input signal, $V_{in}$, is sampled on both plates of the input capacitors $C_1$ and $C_3$ rather than sampling onto one plate of the capacitors with the other tied to a reference. Then in phase $\Phi_D$, capacitors $C_2$ and $C_4$ are charged to the DAC voltage. After that, during $\Phi_2$, $C_1(C_3)$ and $C_2(C_4)$ are connected in series with each other in a feedback loop. In this case, the output voltage will be the sum of voltages on the capacitors and it does not depend on the size of the capacitors. So in the ideal case, the mismatch between any of the capacitors will not affect the output voltage and it equals to twice of the input voltage subtracted to the DAC voltage.

## 4. EFFECTS OF CIRCUIT NON-IDEALITIES

Although in the ideal case of the proposed structure, it seems that the effect of the mismatch is completely removed, but some circuit non-idealities degrade its performance. Among these non-idealities, parasitic capacitors and charge injection are the main drawbacks.

Parasitic capacitors arise from the top plate and bottom plate of the MIM capacitors and the parasitic effects of the switches. In the conventional structure, however, these parasitic capacitors do not affect the performance of the circuit. But, the proposed structure is highly sensitive to the top plate and bottom plate parasitic capacitors (TPPC & BPPC). These parasitic capacitors will affect the transfer function of the circuit and cause the differential output voltage to become as:

$$V_{out} = (1 + \frac{C_t}{2C})V_{in} - (1 + 2\frac{C_t + C_b}{C} + 2\frac{C_t C_b}{C^2})V_{DAC} \quad (3)$$

where $C_{1,2,3,4} = C$, and $C_t$ and $C_b$ is the TPPC and BPPC of the capacitors, $C_1$ to $C_4$, respectively.

To compensate this non-ideality, as shown in Fig. 3, four capacitors ($C'_1$, $C'_2$, $C'_3$, $C'_4$) are used. Figure 4 shows the parasitic capacitances associated with the main capacitors and also the compensation capacitors in different phases. During $\Phi_1$, the TPPC of the $C'_1$, $C'_{1t}$, holds the same but the opposite amount of charge corresponds to the TPPC of the $C_1$, $C_{1t}$. Again during $\Phi_D$, the BPPC of the $C'_2$, $C'_{2b}$, holds the same and the opposite amount of charge corresponds to the BPPC of the $C_2$, $C_{2b}$. So during $\Phi_2$, the charges of these capacitors cancel each other. The charge conservation equations at nodes **X**, **Y**, **In-** and **In+** are given in equations (4) to (7), respectively:

$$\begin{aligned}\mathbf{X}: &C_1(V_X - V_{out+}) + C_2 V_X + (C_{1t} + C_{2t})V_X \\ &= -C_1 V_{in} - C_2 V_{DAC} - C_{1t}V_{in}/2\end{aligned} \quad (4)$$

$$\begin{aligned}\mathbf{Y}: &C_3(V_Y - V_{out-}) + C_4 V_Y + (C_{3t} + C_{4t})V_Y \\ &= C_3 V_{in} + C_4 V_{DAC} + C_{3t}V_{in}/2\end{aligned} \quad (5)$$

$$\begin{aligned}\mathbf{In-}: &-C_2 V_X \\ &= C'_{1t}V_{in}/2 - (C'_{2t} + C'_{2b} - C_{2b} - C_2)V_{DAC}\end{aligned} \quad (6)$$

$$\begin{aligned}\mathbf{In+}: &-C_4 V_Y \\ &= C'_{3t}V_{in}/2 + (C'_{4t} + C'_{4b} - C_{4b} - C_4)V_{DAC}\end{aligned} \quad (7)$$

where $C_{1,2,3,4} = C'_{2,4} = C$, $C'_{1,3} = C/2$, $C_{1t,2t,3t,4t} = C'_{2t,4t} = C_t$, $C'_{1t,3t} = C_t/2$. Equations (4) through (7) show that the differential output voltage with the compensation is as follows:

$$\begin{aligned}V_{out} \cong &2\left[1 + \frac{\varepsilon C_t}{4C} - \frac{1}{2}(\frac{C_t}{C})^2\right]V_{in} \\ &- \left[1 + 2\alpha\varepsilon + \frac{\varepsilon C_t}{C} - 2(\frac{C_t}{C})^2\right]V_{DAC}\end{aligned} \quad (8)$$
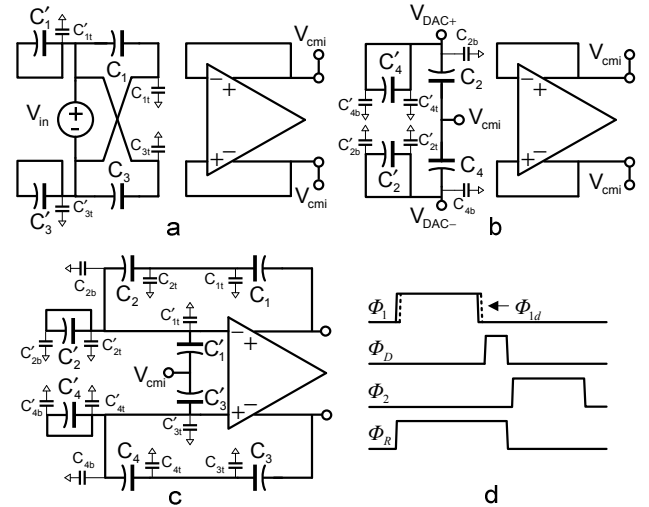


**Figure 4:** Structure of the proposed 1.5-bit mismatch-insensitive MDAC in different phases: (a) phase $\Phi_1$, (b) phase $\Phi_D$, (c) phase $\Phi_2$, and (d) timing diagram of phases.
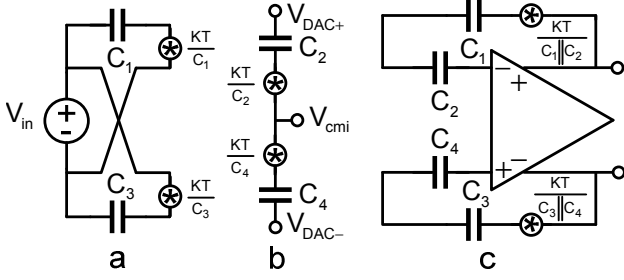
**Figure 5:** Noise voltage sources in each phase.

where $\alpha$ is the BPPC factor and $\varepsilon$ is the percentage of mismatch between $C_1$ and $C_2$; i.e. $C_2 = C_1(1+\varepsilon)$. Compared to the proposed architecture without compensation, the first order term in (3) disappears and only the second order term remains in (8). So, the proposed circuit with the compensation is less sensitive to the parasitic capacitors.

Charge injection is due to mobile channel charge in the switches. Since in our topology the input capacitors are sampled on both plates, the bottom plate sampling is not beneficial. To alleviate this effect, the bottom plates of the sampling capacitors are connected to a switch that is triggered with a delayed version of $\Phi_1$, $\Phi_{1d}$. Also a dummy switch is connected to the top plate of the sampling capacitors to cancel the charge of these switches.

### 4.1 Speed considerations

The expressions for the capacitive load of the conventional MDAC and the proposed structure are given in equations (9) and (10), respectively:

$$\left( C_1 \big\| \left( C_2 + C_p \right) \right) \approx \frac{C}{2} \qquad (9)$$

$$C_1 \big\| C_2 \big\| C_1' \approx \frac{C}{4} \qquad (10)$$

where $C_p$ is the total parasitic capacitance at the input of the opamp. From these equations, it is seen that the capacitive load of the proposed structure is smaller than the conventional MDAC. In addition, the feedback factor for the proposed scheme is:

$$FF = \frac{C/2}{C/2 + C_p} \qquad (11)$$

which is nearly the same as the conventional structure. So with the same power consumption, the proposed scheme is faster than the conventional structure. Hence, despite the addition of a phase ($\Phi_D$), the overall speed of the proposed MDAC gets faster than that of a conventional one.

### 4.2 Comparison of *kT/C* noise performance

The *kT/C* noise power is calculated with the assumption that the opamp is ideal and has infinite bandwidth. Figure 5 shows the noise voltage sources in each phase. In phase $\Phi_1$, $kT/C_1$ is stored on capacitor $C_1$. Then, in phase $\Phi_D$, $kT/C_2$ is stored on capacitor $C_2$. Finally, in phase $\Phi_2$,

$kT/(C_1\|C_3)$ is stored on capacitors $C_1$ and $C_3$ and added to the previous amount of noises that were stored on them. The expression for the differential input referred *kT/C* noise for the proposed scheme is hence given by:

$$V_{n,in}^2 = V_{n,out}^2 \big/ A_v^2$$

$$= \left( \frac{kT}{C_1} + \frac{kT}{C_2} + \frac{kT}{C_3} + \frac{kT}{C_4} + \frac{kT}{C_1\|C_2} + \frac{kT}{C_3\|C_4} \right) / 2^2 \qquad (12)$$

$$= \frac{2kT}{C}$$

which is nearly the same as the input referred *kT/C* noise for the conventional 1.5bit MDAC.

## 5. SIMULATION RESULTS

HSPICE circuit-level Monte-Carlo simulations were performed on the conventional and the proposed MDAC by using a 90nm CMOS technology to compare and evaluate the proposed scheme's performance. The opamp and switches were ideal in order to see just the effects of the capacitor mismatches on the performance of the proposed structure. To get better and realistic results, a model of opamp which indicates its limited $G_m$ and output resistance was used. Also, to see the effects of parasitic capacitors, a model of parasitic capacitors was made with the assumption that $C_t$ and $C_b$ are 1% and 5% of the main capacitor, respectively. 1% relative mismatch was made between the capacitors $C_1$ ($C_3$) and $C_2$ ($C_4$). The differential input voltage and DAC voltage were chosen to 0.2V and 0.6V so that the output voltage would settle to 1.0V. As is seen from Fig. 6, the conventional structure shows an error in the output voltage up to 0.5 percent, while it is 0.05 percent for the proposed one, which is 10 times smaller.

Figure 7 shows the transient step response of the proposed technique. From this figure, it is obvious that the mismatch between the capacitors has a much smaller impact on the output voltage of the proposed structure in comparison with the conventional one.

To see the effects of charge injection of the sampling switches, the input sampling switches were realized by bootstrapped switches. The bottom plates of the sampling capacitors are connected to a switch that is triggered with a delayed version of $\Phi_1$, $\Phi_{1d}$. Also, a dummy switch is connected to the top plates of sampling capacitors to cancel the channel charge of the sampling switches. Figure 8 shows the output PSD for a single tone input signal. The sampling frequency was 250 MHz and the input signal frequency was 15.380859375 MHz. From the figure, the output signal to noise plus distortion ratio (SNDR) is approximately 77 dB. So the proposed structure does not suffer much from the effects of charge injection of the sampling switches.

To evaluate the speed of the proposed structure and compare the results with the conventional one, a folded cascode opamp was used. As is evident from Fig. 9, the settling behavior of the proposed structure is better than the conventional MDAC as theoretically expected.

Table 1 gives a summary of the information about the performances of the conventional and the proposed MDAC structures.

## 6. CONCLUSIONS

A new mismatch-insensitive 1.5 bit MDAC was proposed which is less sensitive to the mismatch between the capacitors in both input signal and feedback DAC paths. Simulation results show that the proposed scheme provides better accuracy as well as faster settling speed in comparison to the conventional MDAC.
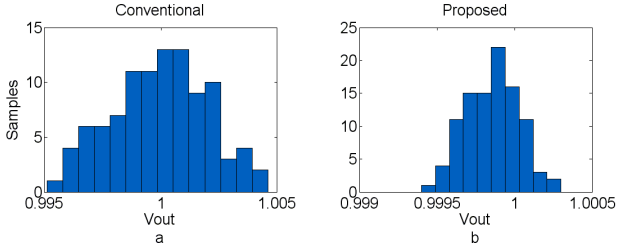


**Figure 6:** Evaluation of the proposed structure using 100 Monte-Carlo simulations with a 1% relative-mismatch for the capacitors. (a) The histogram of the output of the conventional MDAC and (b) the histogram of the output of the proposed MDAC.
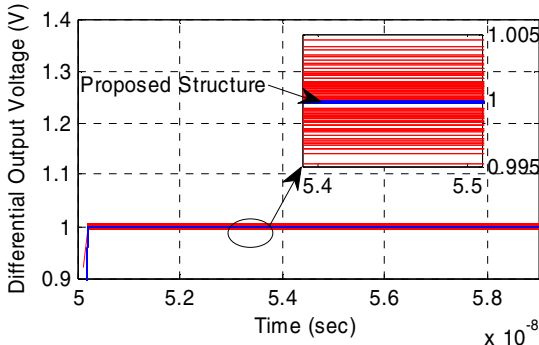


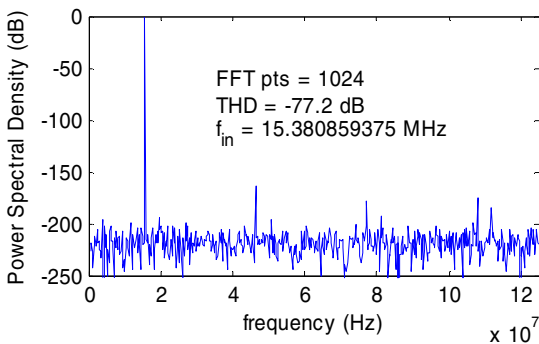**Figure 7:** Transient step response of both topologies.



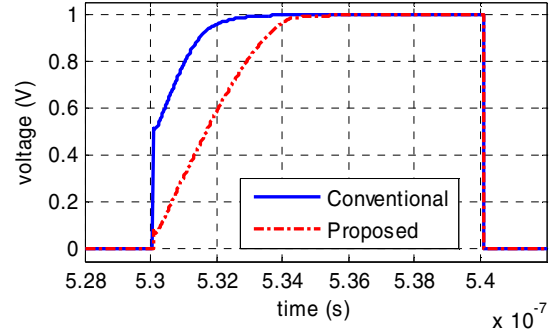**Figure 8:** The output PSD for a single tone input signal of the proposed MDAC.



**Figure 9:** Settling behavior of the conventional and the proposed MDAC.

**Table 1:** Performance results of both topologies

| Parameter | Conventional MDAC | Proposed MDAC |
|---|---|---|
| No. of required phases | 2 | 3 |
| Output mismatch (3σ) | 0.5% | 0. 05% |
| Feedback factor | 1 | 1 |
| Load | $C/2$ | $C/4$ |
| $kT/C$ noise | $2 \times kT/C$ | $2 \times kT/C$ |

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