A High Input Impedance Fully-Differential Chopper Amplifier for Closed-Loop Neural Recording

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***Abstract*—This paper presents a chopper capacitively-coupled instrumentation amplifier (CCIA) with low power and low area consumption and high input impedance for closed-loop neural recording in the presence of in-band stimulation artifacts. A novel high linear pseudo resistor is used in DC servo loop (DSL) making the small high-pass cut-off frequency with small capacitor, and hence, reduced area occupation. With reducing the high-pass cut-off frequency, the positive feedback loop can also operate at low frequency. The proposed work has been simulated with Cadence using a 180 nm CMOS process. This chopper amplifier can tolerate 20 mV_p differential input and 520 mV_p common-mode artifacts while recording the small neural signal.**

***Keywords*— Chopper amplifiers, closed-loop neural recording, front-end, stimulation artifacts, DC servo loop, positive feedback loop.**

I. INTRODUCTION

Neural recording is an effective way for diagnosis and therapy of the various diseases like Parkinson's disease, epilepsy, narcolepsy, and depression [1]. In closed-loop neural systems, neural signals are required to be recorded while the neurons are stimulated simultaneously. The stimulation artifacts contain both the common-mode and differential-mode components which can saturate the conventional neural recording amplifier [2]. One of the main challenges in the design of the neural amplifiers is existence of large stimulation artifacts. Due to the large in-band differential-mode artifact, the mid-band gain is usually limited to less than 30 dB to avoid the saturation of the chopper amplifier [2].

The neural signals are classified as local field potentials (LFPs) and action potentials (APs) that are recorded by electrodes [2, 3]. The frequency range of LFPs is about 1 Hz to 200 Hz, and for APs, it is about 200 Hz to 5 kHz [2]. The maximum amplitude of the LFPs is about 1 mV and the maximum amplitude of the APs is about 100 µV [2, 4].

The analog front-end (AFE) amplifier is one of the most significant blocks in the closed-loop seizure control systems since the peak amplitude of the interested signals are small and they are affected by the flicker noise. To reduce the flicker noise, large input transistors can be used while this technique cannot decrease the noise enough [5, 6]. To mitigate the low frequency flicker noise of the amplifier, the chopping is an impressive way [2, 7]. In this technique, the input signal is firstly modulated by the input modulator and then it is amplified. Finally, at the output of the amplifier, the input signal is demodulated to the primary frequency and the flicker noise is modulated to high frequency. Therefore, the flicker noise is attenuated by a low-pass filter succeeding at the output of the amplifier [7, 8]. In addition to LFPs and APs, a large offset is appeared at the electrode with magnitudes of sub mV to a few volts. A DC servo loop (DSL) is usually employed in neural amplifiers to avoid the saturation of the amplifier output due to large input offset. To realize a sub-Hz high-pass corner in DSL, pseudo resistors are utilized instead of the passive resistors [7, 9]. These resistors need small area.

In [2], a DSL with an RC integrator is used with 20 pF total integrator capacitor. In [4], a DSL based on the Gm-C integrator with 80 pF total integrator capacitor has been used. In these works, large capacitors have been used to achieve low high-pass corner frequency while in neural recording amplifiers; the area consumption is one of the important factors. In [2], a current-reused differential pair is used in the first stage while the input common-mode range of this circuit is less than the required common-mode range. In [10], an extra circuit is used to alleviate this issue and to tolerate 650mV_{pp} common-mode artifacts at the cost of the increased power consumption and area.

In this paper, a closed-loop neural recording amplifier is presented by using several techniques such as the chopping, DC servo loop, positive feedback loop (PFL), and ripple reduction. A modified folded-cascode amplifier with an inherent common-mode feedback (CMFB) circuit is utilized in the first-stage to accommodate the large input common-mode range. In the second-stage, a fully-differential common-source amplifier with a simple CMFB circuit is utilized to achieve large swing. Moreover, a new pseudo resistor with large resistance and high linearity is employed.

The rest of the paper is organized as follows. Section II describes the structure and design challenges of the proposed neural recording chopper amplifier. Section III presents the simulation results, and Section IV concludes the paper.

II. PROPOSED NEURAL RECORDING AMPLIFIER

A. Overall Structure

The proposed neural recording chopper amplifier is shown in Fig. 1. It comprises of a two-stage Miller compensated amplifier (G_{m1} and G_{m2}), a positive feedback loop, a DSL based on the RC integrator, a capacitive feedback loop, ripple reduction capacitors (C_{DC}) and chopping switches. The Chopper is included four CMOS switches. The chopping frequency is selected 25 kHz that is in proportion to the bandwidth of the chopper capacitively-coupled instrumentation amplifier (CCIA) and the bandwidth of the G_{m1} [8].

The input chopper could be placed before or after $C_{in1,2}$ [9]. The second case reduces the common-mode rejection ratio (CMRR) due to the mismatch of the input capacitors. Thus in

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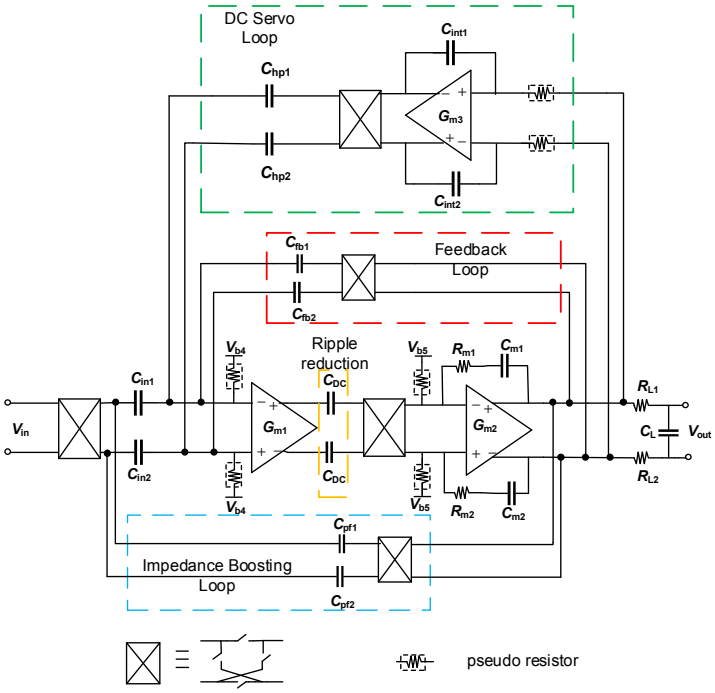

Fig. 1. Structure of the simulated closed-loop neural amplifier.

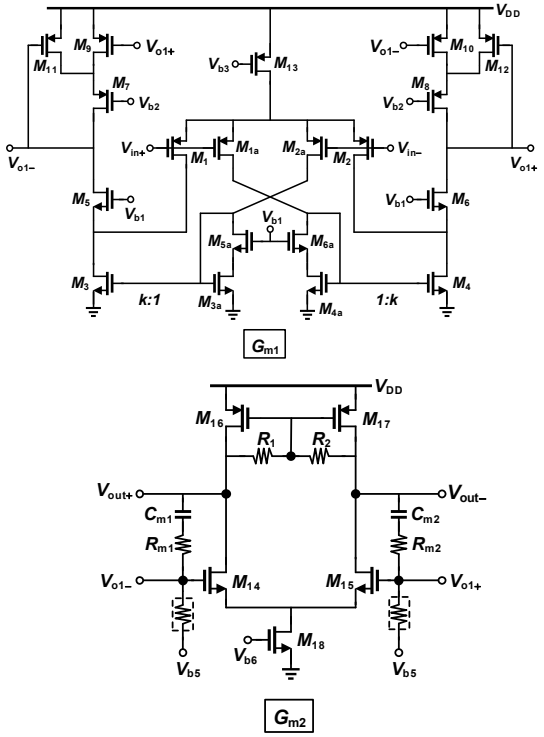

Fig. 2. Schematic of the proposed two-stage OTA.

this structure, the input chopper is placed before $C_{in1,2}$. The capacitive feedback loop consists of $C_{in1,2}$ and $C_{fb1,2}$, defines the pass-band gain of the chopper amplifier which is given by $G_0 = C_{in1,2}/C_{fb1,2}$. In the capacitive feedback, the gain is set accurately by the ratio of capacitors. In this proposed design, $C_{in1,2}$ and $C_{fb1,2}$ are set to 1 pF and 50 fF, respectively.

The low-pass corner frequency of the total close-loop structure is given by:

$$f_H \approx \frac{1}{2\pi}\frac{C_{fb}}{C_{fb}+C_{in1,2}} \times A_0 \times \frac{1}{g_{m14}R_{o1}R_{o2}C_{m1,2}} \quad (1)$$

where A_0 is the open-loop gain which is given by $(1+k)g_{m1}g_{m14}R_{o1}R_{o2}$, the current mirror factor k is 13/12 in the first-stage amplifier as shown in Fig. 2, R_{o1} and R_{o2} are the output resistances of the G_{m1} and G_{m2}, respectively. By substituting A_0 into (1), the closed-loop low-pass corner frequency is obtained as:

$$f_H \approx \frac{1}{2\pi}\frac{C_{fb1,2}}{C_{in1,2}+C_{fb1,2}}(1+k)\frac{g_{m1}}{C_{m1,2}} \quad (2)$$

B. Two-Stage Amplifier

The structure of the two-stage Miller compensated OTA is shown in Fig. 2. A pair of capacitors C_{DC} is used between the amplifier stages to remove the DC offset. Also C_{DC} capacitors reduce the ripple at the output since with these capacitors, the offset current generated by G_{m1} which is the primary cause of output ripple, is blocked [11]. The pseudo resistors connected to the input of the G_{m1} and G_{m2} stages are used to create a stable DC bias for the input pairs. The swing of the second-stage mainly determines the linearity of the circuit.

Due to the chopper structure, the flicker noise of the OTA is highly attenuated and hence the thermal noise is the main remained noise source [12]. The input transistors of G_{m1} and G_{m2} are biased in the subthreshold region for low noise and low power design, because in this region, the g_m of the transistors is larger than the strong inversion region. G_{m1} and G_{m2} consume 825 nA and 130 nA, respectively.

Since the common-mode artifacts have the same bandwidth as the differential signals of interest, the opamp have to tolerate these large common-mode artifacts. Due to the folded-cascode structure of G_{m1} stage, it can tolerate large common-mode artifacts. The cross-coupled transistors comprising of M_7-M_{12} transistors defines the output common-mode voltage of the modified folded-cascode amplifier without needing an explicit CMFB circuit [13]. In the second-stage, resistors R_1 and R_2 are used to define the output common-mode voltage. The Miller compensation with a nulling resistor is used to provide a dominant pole in the proposed two-stage amplifier and hence the closed-loop stability. Two wide-swing cascode current mirrors are utilized to bias the two-stage amplifier shown in Fig. 2.

C. DC Servo Loop

The DSL is a negative feedback loop that is used to attenuate to low frequency signals such as electrodes offset at the output of the amplifier. As shown in Fig. 1, it is realized by an RC integrator, chopper switches, and capacitors $C_{hp1,2}$. The value of the $C_{hp1,2}$ capacitors is obtained as [4, 7]:

$$V_{EDO} \le \frac{V_{DD}C_{hp1,2}}{C_{in1,2}} \quad (3)$$

where V_{EDO} is the maximum offset voltage that is cancelled by the DSL. In this work, the maximum V_{EDO} of ±50 mV is cancelled with $C_{hp1,2}$ = 50fF. The high-pass corner, f_{hp}, of the DSL is is given by [7]:

$$f_{hp} = \frac{C_{hp1,2}}{C_{fb1,2}} f_{ugb} \quad (4)$$

where f_{ugb} is the unity-gain frequency of the integrator in the DSL. A simple two-stage Miller compensated amplifier is also used as G_{m3} with total 400 nA current consumption including the CMFB circuit.

In this paper, a new linear pseudo resistor with large value is utilized to achieve low unity-gain frequency in the integrator with small $C_{int1,2}$ capacitors. This decreases the required die area. The value of $C_{int1,2}$ capacitors is chosen as 820 fF. The structure of proposed pseudo resistor is shown in Fig. 3. This pseudo resistor has higher linearity in comparison with the pseudo resistors presented in [14] since the transistors of this pseudo resistor operate in the cut-off region and in the bias circuit, PMOS transistors are used in order to achieve less sensitivity to the process variations. For an input tone of 20 mV_p, the simulated total harmonic distortion (THD) of this pseudo resistor is about -54.2 dB while the THD of pseudo resistor presented in [14] with a value of 40 MΩ is about -35.8 dB with the same input. The value of this pseudo resistor is about 1 TΩ. The simulated THD of the duty cycled resistor (DCR) presented in [2] is about -53.1 dB and its resistance is 4 GΩ. Besides, the DCR suffers from the aliasing issue because it employs the sampling technique and also a very fast clock must be used for biasing. In these simulations, an RC low-pass filter with a 1 pF series capacitor and pseudo resistor is used to calculate the THD of pseudo resistors with considering five harmonics.

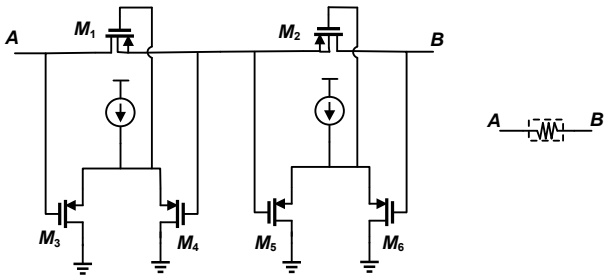

Fig. 3. The proposed pseudo resistor.

D. Positive Feedback Loop

The main problem of the chopper topology is reducing the differential input impedance. The equivalent switched-capacitor resistance is given by:

$$Z_{in} = \frac{1}{2 f_{ch} C_{in1,2}} \quad (5)$$

with f_{ch} = 25 kHz and $C_{in1,2}$ = 1pF, the input DC impedance will be limited to 37 MΩ. A PFL is used to increase the input impedance [4, 7, 9]. In this work, a PFL is also utilized to boost the input impedance up to 958 MΩ at 15 Hz that is enough for neural recording.

The PFL is driven by the output and the DSL attenuates the DC signal at the output by creating a high pass corner. So the PFL is rendered inoperative at DC. With the proposed high density pseudo resistor, the high-pass frequency is decreased to 0.1 Hz, and hence the PFL can operate at low frequency as well.

III. Simulation Results

The proposed chopper amplifier has been simulated in Cadence using TSMC 0.18 µm CMOS process. The simulation results in different process corner cases and power supply variations are summarized in Table 1. In all simulations, V_{DD} is 1.6 V in FS and SS corners and it is 2 V in SF and FF corners. For typical corner, V_{DD} is 1.8 V. As shown in Fig. 4, the simulated mid-band gain in typical corner case is 26.06 dB with a –3 dB bandwidth of 0.1 Hz–5 kHz. The simulated closed-loop amplifier consumes about 2.02 µA from a 1.8 V power supply.

The total input-referred noise of the chopper amplifier is 0.58 μV_{rms} for a bandwidth from 1 Hz to 200 Hz (LFP) and it is 2.54 μV_{rms} for 200 Hz–5 kHz (AP) bandwidth. The simulated input-referred noise power spectral density (PSD) is shown in Fig. 5 in different process corner cases and body temperature.

In this work, the electrode offset can be tolerated up to 50mV with smaller capacitors $C_{int1,2}$ which are used in the active RC integrator compared to [2, 9]. The simulated input impedance of the chopper amplifier is shown in Fig. 6 in process variations at 37°C.

Table 1. Effect of the process variations on the AFE characteristics at 37°C.

Process Corner	TT	SF	FS	FF	SS
Mid-band Gain (dB)	26.06	26.06	26.07	26.07	25.9
Bandwidth (Hz)	0.1-5k	0.12-6 k	0.2-4.1 k	0.12-6.3 k	0.1-3.6 k
Total current (µA)	2.02	2.09	1.9	2.03	2.05
Input referred noise (μV_{rms})	LFP:0.58 AP: 2.54	LFP: 0.62 AP: 2.75	LFP:0.57 AP: 2.47	LFP:0.6 AP: 2.68	LFP:0.59 AP: 2.61
Input impedance @ 15Hz	958 MΩ	1.8 GΩ	1.3 GΩ	568 MΩ	920 MΩ
NEF	LFP: 2.32 AP:2.07	LFP:2.53 AP: 2.28	LFP: 2.21 AP: 1.96	LFP: 2.41 AP: 2.19	LFP: 2.38 AP: 2.15
THD (dB) (40 mV_{pp})	-73.22	-73.88	-67.86	-67.83	-57.93

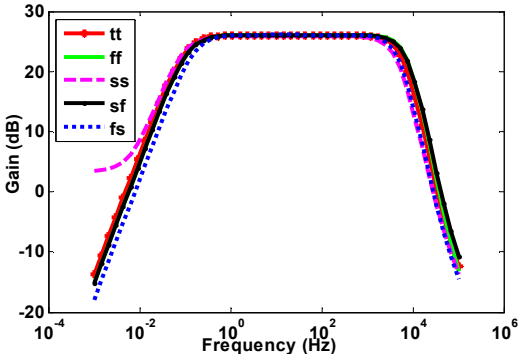

Fig. 4. Simulated frequency response of the proposed neural amplifier at 37°C.

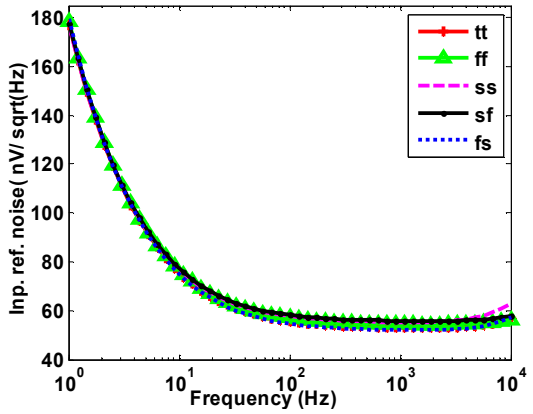

Fig. 5. Total input-referred noise in process variations and 37°C.

The simulated THD is about −73.22 dB as shown in Fig. 7 where an input tone with 40 mV_{pp} at 1 kHz is applied. A two-tone test with a large common-mode input of 520 mV_p at 750 Hz is applied to the simulated amplifier. The differential input tones are 20 mV_p at 750 Hz indicating the differential stimulation artifact and 1 mV_p at 1 kHz representing the desired neural signal. The achieved simulation result is depicted in Fig. 8. As it is seen, the intermodulation terms are small and the simulated amplifier can tolerate large differential and common-mode artifacts while amplifying the desired small neural signal. The simulated step response of the proposed amplifier is shown in Fig. 9. As it is seen, there is not any overshoot indicating the proper stability of the closed-loop amplifier. The ripples in the step response belong to the chopping mechanism and they are attenuated by the low-pass filter succeeding the neural amplifier.

The proposed neural amplifier is compared with the current state-of-the-art works in Table 2. The following noise efficiency factor (NEF) is used in this comparison [15]:

$$\mathrm{NEF} = V_{ni,rms}\sqrt{\frac{2I_{tot}}{4\pi V_T kTBW}} \tag{6}$$

where $V_{ni,rms}$ is the input-referred rms noise voltage, BW is the amplifier bandwidth, I_{tot} is the total supply current, and V_T is the thermal voltage. A lower NEF means that lower noise is

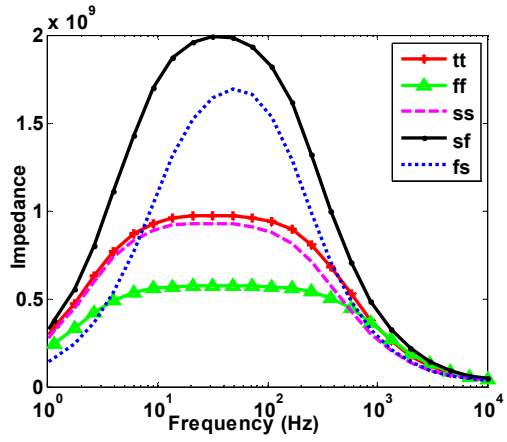

Fig. 6. Simulated input impedance of the chopper amplifier at 37°C.

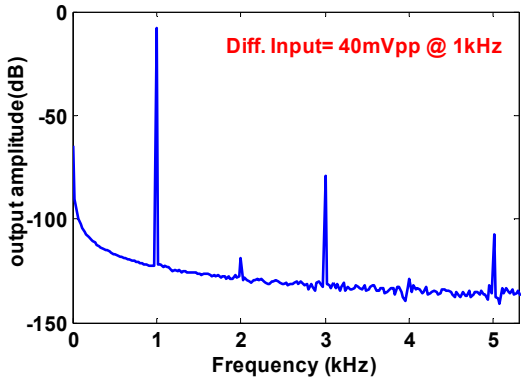

Fig. 7. Total harmonic distortion of the chopper amplifier for a 40 mV_{pp} input at 1 kHz.

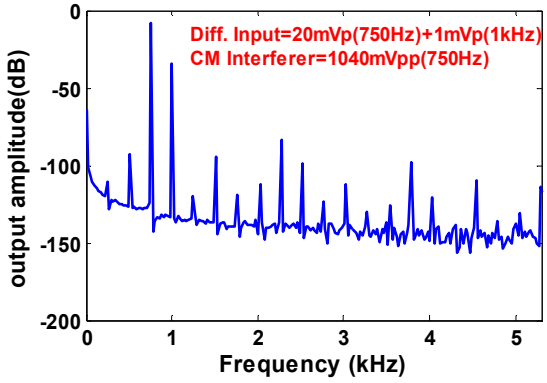

Fig. 8. Two-tone test with a large common-mode input.

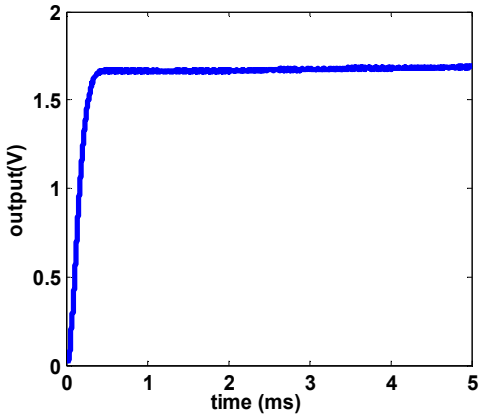

Fig. 9. Step response of the simulated closed-loop neural amplifier.

achieved after being normalized to the analogous current consumption. The other figure of merit is the power efficiency factor (PEF) which is defined as [15]:

$$PEF = V_{DD}.NEF^2 \tag{7}$$

According to Table 2, the achieved performance of the proposed neural amplifier is comparable with the best reported designs in current literature.

Table 2. Simulation performance summary and comparison with the current state-of-the-art.

Parameters	[6] JETCAS'11	[16] TCAS'15	[2] JSCC'17	[10] JSCC'17	[17] ISCAS'19	[4] JSCC'19	This work
Topology	CCIA	Chop. Amp.	Chop. Amp.	Chop. Amp.	Chop. Amp.	Chop. Amp.	Chop. Amp.
Process (nm)	180	180	40	40	180	180	180
Supply voltage (V)	1.8	1.25	1.2	1.2	1	1.8	1.8
Total current (μA)	11.5	1.7	1.66	2.33	1.89	1.8	2.02
Signals	LFP + AP	LFP + AP	LFP + AP	LFP + AP	ECoG	LFP + AP	LFP + AP
Mid-band gain (dB)	52.5-57.7	32	26	25.7	40	40	26.06
Bandwidth(Hz)	4-10 k	0.5 - 10 k	0.2 – 5 k	0.12 – 5 k	0.4 -500	0.3 – 5.4 k	0.1 – 5k
Input referred noise (μV_{rms})	2.6	5.7	LFP: 2 AP: 7	LFP :1.8 AP: 5.3	0.75 (1-200)	LFP: 0.65 AP: 2.14	LFP: 0.58 AP: 2.54
NEF	3.38	2.9	LFP: 7 AP: 4.9	LFP: 7.4 AP: 4.4	2.77	LFP: 2.37 AP: 1.56	LFP: 2.32 AP: 2.07
PEF	20.56	10.51	LFP: 58.8 AP : 28.81	LFP: 65.71 AP : 23.23	7.7	LFP: 10.11 AP : 4.38	LFP: 9.68 AP : 7.71
Impedance	N/A	N/A	300 MΩ	1.6 GΩ	100 MΩ	440 MΩ @50Hz	958MΩ @15Hz
Tolerance to Large-signal CM	No	No	No	650 mVpp	No	No	1040 mVpp
Electrode Offset Removal	RC Filter	RC Integrator DSL	RC Integrator DSL	RC Integrator DSL	Gm-C DSL	Gm-C DSL	RC Integrator DSL
Total Integrator Capacitor	N/A	30 pF	20 pF	24 pF	N/A	80 pF	1.64 pF
DR (dB)	N/A	N/A	LFP: 78 AP: 69	LFP: 81 AP: 74	N/A	N/A	LFP: 87.63 AP: 74.89
THD (dB)	-46.24 (1 mV_{pp})	N/A	-74 (40 mV_{pp})	-76 (80 mV_{pp})	-46.02 (1 mV_{pp})	-61 (5 mV_{pp})	-73.22 (40 mV_{pp})
Sim./Meas.	Sim.	Meas.	Meas.	Meas.	Sim.	Meas.	Sim.

IV. Conclusion

This paper presents a closed-loop neural amplifier to record the LFP and AP signals in the presence of large differential and common-mode stimulation artifacts. A linear pseudo resistor is utilized in DSL making the realization of the cut-off frequency of the high-pass filter with a small capacitor and also low frequency operation of the PFL. A two-stage Miller compensated amplifier with inherent CMFB circuits is used to realize the required G_m stages. A modified folded-cascode amplifier is used to accommodate the large input common-mode variations.

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