A Very Wideband Low Noise Amplifier for Cognitive Radios

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Abstract— In this paper, a new full on-chip CMOS low-noise amplifier (LNA) topology for the range of 50 MHz to 10 GHz is introduced that has very low power consumption. It exploits the combination of a common-gate (CG) stage for wideband input matching and a common-source (CS) stage for canceling the noise and distortion of CG stage. Moreover the CS stage used both nMOS and pMOS transistors to improve the IIP2. Simulated in a 90 nm RF CMOS technology, the proposed LNA achieves a noise figure of 2.3 dB to 2.8 dB and input return loss (S_{11}) less than -10 dB over whole the bandwidth while consumes only 6 mW from a 1 V power supply. The average of the power gain (S_{21}) is 12 dB. The achieved IIP3 and IIP2 are about -5 dBm and 20 dBm, respectively.

I. Introduction

Nowadays the idea of "cognitive radios" (CR) has interested scientific because the usage of the cellular and wireless local area network (WLNA) bands has increased. CRs can utilize any unoccupied channel in a wide frequency range, from several of megahertz up to 10GHz but conventional wireless transceivers can be applied in especial bands [1]. Recent effort on CR design has focused on the TV bands below 1 GHz [2], but, CRs will be applied for a much wider spectrum in near future. Because of a large bandwidth, this structure can be applied for wireless personal area networks (WPANs), providing seamless connectivity between consumer electronics devices for transmission of video, audio, and other high-bandwidth data (range of frequency is 3 to 10 GHz) [3]. Also it can be used for TV application (range of frequency is 50 to 900 MHz). The broadband behavior of receiver is determined by the front-end low-noise amplifier.

The design of broadband low noise amplifiers is controlled by tradeoff between input matching, noise figure, gain, bandwidth, linearity, and voltage headroom. There are many possible techniques to design a wide-band low noise amplifier, including common gate amplifiers [4, 5], distributed amplifiers, and negative feedback amplifiers [6]. The choice of topology begins with the input matching requirement. Here, we compare two common wideband matching techniques: a common-source (CS) stage with resistive shunt feedback and a common-gate stage [7]. These two structures are shown in Fig. 1. For having wideband input matching in CS stage, we have to use the resistive feedback which causes to reduce NF and gain. In addition, it consumes high power. But, CG stage can implement broadband impedance matching without many extra components. Moreover, the CG LNA has better linearity, low power consumption, and better input-output isolation [8] although it suffers from the poor noise performance because the g_m of this structure should be 20 mA/V for having the input matching condition. A popular method for reduction the noise figure (NF) is the noise cancelation structure which eliminates the channel thermal noise of the CG structure by using a common source (CS) transistor [7].

In this paper, a low power LNA is designed by using the CG structure and the noise cancellation technique which also removes partially the circuit's nonlinear distortion. In addition, for input matching below 1 GHz, a new technique is introduced. Section II describes the concept of the proposed wideband LNA and the analysis of gain, noise, and input matching are given. Section III describes the simulation results. Finally, the conclusion is presented in Sect. IV.

II. Circuit Analysis and Design

The proposed LNA is shown in Fig. 2. In this structure, M_1 is used as the CG structure for implementing the broadband input matching. In addition, the CS stage, M_2, is applied for canceling the channel noise of M_1. To reuse the current of M_2 and improve the IIP2, M_3 is selected as a pMOS transistor. The gate-source parasitic capacitor of M_1 is damped by L_g in order to improve the input return loss (S_{11}). L_s is used to cancel the degrading effect of the parasitic capacitances of transistors M_1 and M_2. The gate inductor L_1 and drain inductors L_{D1}, L_2 and L_3 are added for inductive shunt-peaking and series-peaking, respectively. The resistor R_A is applied to extend the bandwidth in low frequencies and decrease the flicker noise of M_1. In the output node, R_L is paralleled in order to decrease the variation of output impedance and hence to achieve a smooth gain. Finally, we used negative feedback, R_F, for preventing the variation of output voltage because the output node is a high impedance node. The value of R_F is selected large in order to ignore its effect in the analysis. In this paper, we ignored L_g, and L_1 in calculations for simplifying. Part A describes the input matching and bandwidth extension. Noise and gain analysis are explained in parts B and C, respectively. Eventually, part D describes the non-linearity behavior briefly.

A. Input Matching and Bandwidth Extension

To achieve the input matching in 10GHz bandwidth, especially in low frequencies, we have to increase the size of L_s up to 200 nH, because, if the size of L_s decreases the series resistance of L_s, R_{Ls}, due to limited quality factor of L_s, will be decreased (approximately up to 5Ω). So, this resistance is

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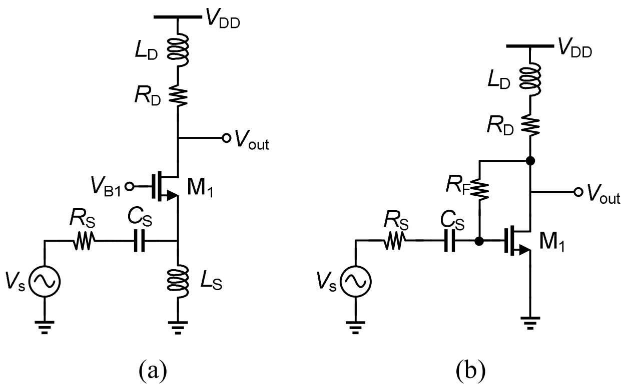

Figure 1: Common wideband input matching techniques (a) common gate, and (b) CS with resistive shunt feedback

paralleled with Z_{i1}. As shown in Fig. 2, $Z_{i1} \approx 1/(g_{m1}+g_{mb1})$. So, in $(R_{Ls}+sL_s)\,\|\,1/(g_{m1}+g_{mb1})$, the sL_s term can be ignored in low frequencies resulting in a degraded input matching condition below 1.5 GHz. For solving this problem, we put a series resistor, R_A, with L_s, hence, the equivalent impedance is equal to $(R_{Ls}+R_A+sL_s)\,\|\,1/(g_{m1}+g_{mb1})$. In low frequencies $R_A >> (R_{Ls}+sL_s)$, $1/(g_{m1}+g_{mb1})$. Accordingly, the input impedance approximately equals $1/(g_{m1}+g_{mb1})$ in this paper. In the following to take into account the body effect of M_1 and also to simplify the relations, g_{m1} stands for $g_{m1}+g_{mb1}$. The input impedance with resistor R_A is calculated as:

$$
\begin{aligned}
Z_{in} &= \left(R_A + sL_s\right)\left\|\frac{1}{sC_X}\right\|\frac{1}{g_{m1}} \\
&= \frac{R_A + sL_s}{C_X L_s s^2 + \left(R_A C_X + g_{m1} L_s\right)s + \left(g_{m1} R_A + 1\right)}
\end{aligned}
\tag{1}
$$

Thus, the poles of Z_{in} are obtained approximately as:

$$
\omega_{p1} \approx \frac{R_A g_{m1} + 1}{R_A C_X + g_{m1} L_s} \approx \frac{R_A}{L_s}, \qquad g_{m1} L_s \gg R_A C_X \tag{2}
$$

$$
\omega_{p2} \approx \frac{R_A C_X + g_{m1} L_s}{C_X L_s} \tag{3}
$$

where C_X denotes the parasitic capacitance in node X and equals to $C_X = C_{gs1} + C_{gs2}$ where C_{gs1} is also damped by L_g.

The series resistor, R_A, causes the dominant pole, ω_{p1}, to move to the upper frequencies, so, the bandwidth in low frequencies is increased. Also, the value of zero is increased. On the other hand, since this zero is located between the two poles, this causes to have a smooth gain. But, increasing the value of R_A decreases the gain, so, we need to compensate for that in the next stage.

B. Gain Analysis

The equivalent impedance was seen from drain of transistor M_1 toward the ground is called Z_Y and calculated as $(R_{D1}+sL_{D1})\,\|\,[r_{ds1}+(R_s\,\|\,(R_A+sL_s)(1+g_{m1}r_{ds1}))]\,\|\,1/sC_Y\,\|\,R_F/(1+A_v)$ where R_s is the source resistance and R_A is the series resistance with L_s. R_{D1} and L_{D1} are the load impedance of M_1 and C_Y is the all of parasitic capacitance in node Y. The resistance R_F is large enough and also the voltage gain of M_3 is low, approximately 3, so, the effect of R_F is ignored. Z_{out} is defined

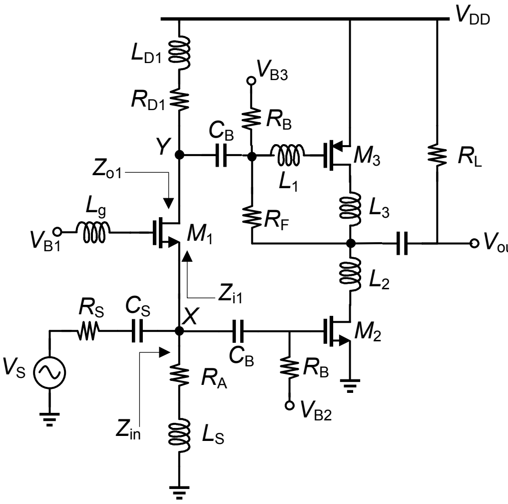

Figure 2: Proposed LNA with added resistor in source of CG-stage.

as the output impedance which is calculated as $(r_{ds2}+sL_2)\,\|\,(r_{ds3}+sL_3)\,\|\,R_L\,\|\,1/sC_{out}$ where $L_{2,3}$ are the drain inductances of both transistors M_2 and M_3, and C_{out} is the parasitic capacitance in output node. According to these assumptions, the voltage gain of this circuit is calculated as:

$$
A_v = \left|\frac{Z_{in}}{Z_{in} + R_s}\right|\left(g_{m1} g_{m3} \left|Z_Y\right| + g_{m2}\right)\left|Z_{out}\right| \tag{4}
$$

$$
Z_{out} = \frac{L^2 s^2 + ALs + B}{C_{out} L^2 s^3 + ALC_{out} s^2 + \left(BC_{out} + 2L\right)s + A} \tag{5}
$$

where $A = r_{ds2} + r_{ds3}$, $B = r_{ds2} r_{ds3}$ and $L = L_3 = L_2$.

By decreasing technology size, for increasing f_t, r_{ds} is reduced owing to the length channel reduction. Also, because of parasites, the variation of r_{ds} in high frequencies is increased. According to (5), Z_{out} has a high value in low frequencies but it falls down in high frequencies. So the variation of gain is increased. For solving this problem, we used the inductive shunt-peaking and series-peaking. The shunt inductive peaking causes a resonance at output of each stage when the gain starts to roll off at higher frequencies, because, the parasites of the output nodes of the each stage are damped by these inductors [9]. Drain inductors in output node, $L_{2,3}$, cause the S_{11} to be deteriorated. So we put an inductor, L_g, in gate of CG stage for damping the parasites of M_1 in order to improve the input matching. Moreover, R_L is paralleled in output node which its value is near to the value of Z_{out} at low frequencies, so it affects more in low frequencies and decreases the variation of the output impedance. As a result, there is less variation in the LNA gain, although, the gain is decreased at low frequencies.

C. Noise Analysis

The purpose of noise cancelation is to decouple the input matching with the NF by canceling the output noise from the matching device [10]. The current noise of input transistor flows into node X but out of node Y that creates two voltages with opposite phases. These two voltages are converted to current by M_2 and M_3 [7]. But, the input signal in these two nodes has the same phases. Thus the input signal is boosted at the output. These two voltages are calculated as $V_x = Z_{in} I_{n,M1}$ and $V_Y = -Z_Y I_{n,M1}$, thus, the output current of noise is equaled to:

$$\begin{aligned} & I_{n,out} = g_{m2}V_x - g_{m3}V_Y = 0 \\ & \Rightarrow g_{m2}V_x = g_{m3}V_Y \Rightarrow g_{m2}Z_{in} = g_{m3}Z_Y \end{aligned} \quad (6)$$

To reuse the current of M_2, M_3 is selected as a pMOS transistor, but using pMOS reduces the bandwidth at high frequencies because of its large parasites. So, we selected low size for it and also we used an inductor, L_1, in gate of pMOS transistor for damping the parasites of pMOS and improving the bandwidth at high frequency. In addition, R_A decreases the flicker noise of M_1.

By using noise cancellation technique, the most important sources of noise are: 1) thermal noise of R_{D1} and R_A, 2) channel noise of M_2, 3) channel noise of M_3. They are calculated as (7-10), respectively. We have also supposed that $R_s = 1/g_{m1}$ in order to simplify the relations.

$$\begin{aligned} NF_{R_{D1}} &= \frac{4kTR_{D1}\left(g_{m3}Z_{out}\right)^2\left(Z_{o1}/\left(Z_{o1}+R_{D1}\right)\right)^2}{4kTR_s A_v^{\,2}} \\ &\cong \frac{R_{D1}R_s}{\left|Z_{o1}+R_{D1}\right|^2} \end{aligned} \quad (7)$$

According to Fig. 2, $Z_{o1} = [r_{ds1}+(R_s \| (R_A+sL_s)\ (1+g_{m1}r_{ds1})]$.

$$NF_{R_A} = \frac{4kTR_A\left(2A_v\right)^2\left(Z_{i1}\|R_s/\left(\left[Z_{i1}\|R_s\right]+R_A\right)\right)^2}{4kTR_s A_v^{\,2}} \cong \frac{R_s}{R_A} \quad (8)$$

According Fig. 2, Z_{i1} is calculated as $(Z_Y + r_{ds1})/(1 + g_{m1}r_{ds1})$, for simplifying. We suppose that $Z_{i1} = 1/g_{m1}$.

$$\begin{aligned} NF_{M2} &= \frac{4kTg_{m2}Z_{out}^{\,2}}{4kTR_s A_v^{\,2}}\frac{\gamma}{\alpha} \\ &= \frac{g_{m2}}{R_s\left(Z_Y g_{m1}g_{m3}+g_{m2}\right)^2}\frac{\gamma}{\alpha} \cong \frac{1}{R_s g_{m2}}\frac{\gamma}{\alpha} \end{aligned} \quad (9)$$

$$\begin{aligned} NF_{M3} &= \frac{4kTg_{m3}Z_{out^2}}{4kTR_s A_v^{\,2}}\frac{\gamma}{\alpha} \\ &= \frac{g_{m3}}{R_s\left(Z_Y g_{m1}g_{m3}+g_{m2}\right)^2}\frac{\gamma}{\alpha} \cong \frac{R_s}{\left|Z_Y\right|^2 g_{m3}}\frac{\gamma}{\alpha} \end{aligned} \quad (10)$$

Finally, the total NF of the proposed LNA is given by:

$$NF = \frac{R_{D1}R_s}{\left|Z_{o1}+R_{D1}\right|^2} + \frac{1}{R_s g_{m2}}\frac{\gamma}{\alpha} + \frac{R_s}{\left|Z_Y\right|^2 g_{m3}}\frac{\gamma}{\alpha} + \frac{R_s}{R_A} \quad (11)$$

According to (11), for decreasing the thermal noise of R_{D1} and R_A, their value should be increased, but, this is limited by voltages that drop on R_{D1} and R_A. In addition, the channel noise of M_2 and M_1 can be decreased by increasing g_{m2} and g_{m3}, respectively.

D. *Non Linearity*

The non-linearity of CS transistor is worse than the CG transistor. In this case, we used the pMOS-nMOS structure in the output stage to improve the values of IIP2 and IIP3. In this method, the input pMOS and nMOS transistors are biased in a way that each transistor expunges the IIP2 of other one [5]. It means that the IIP2 summation of these two transistors counteract each other effects in range of voltage bias.

III. Simulation Results

The proposed LNA shown in Fig. 2 is designed in a 90-nm RF-CMOS technology using Spectre RF. By carefully selection of the transistors size, bias current and picking inductor values, it was possible to operate this amplifier with power dissipation of only 6 mW from a 1V supply voltage while it achieves reasonably high and flat small signal gain and very low noise figure in whole of requisite bandwidth.

As Fig. 3 illustrates, the input return loss is less than -10 dB in the whole of bandwidth. Figure 4 shows the -3dB bandwidth power gain that varies between 10.6-13.4 dB in 50 MHz up to 10 GHz. The NF of this LNA is shown in Fig. 5 where the NF varies from 2.3 dB to 2.8 dB in the 10 GHz bandwidth. The proposed LNA is compared with the same LNA without using R_A and the results are also shown in the figures. In this circuit, the output impedance is approximately 50Ω, so, it does not need a buffer in the output node. The designed values of proposed LNA are shown in Table I. The simulation results in different corner cases and temperature variations are summarized in Table II.

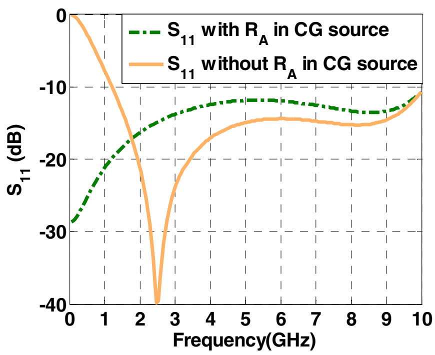

Figure 3 : Simulated input return loss.

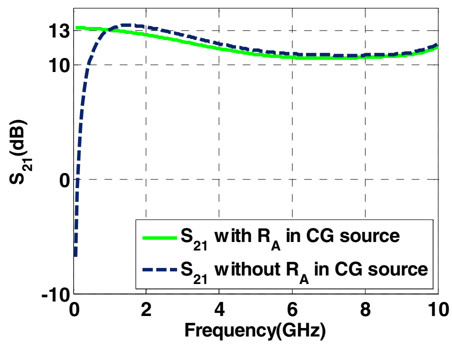

Figure 4: Simulated power gain.

TABLE I. DESIGNED VALUES OF THE LNA.

Transistor size	**(W/L)$_1$** (25×5)µm/90nm		**(W/L)$_2$** (23×5)µm/90nm		**(W/L)$_3$** (10×5)µm/90nm	
Inductor size	L_S 8 nH	L_{D1} 5 nH	L_g 1.7 nH	L_1 2 nH	L_2 3 nH	L_3 1 nH
Resistor size	R_A 300 Ω	R_{D1} 400 Ω	R_F 10 kΩ	R_L 200 Ω		

TABLE II. SIMULATED RESULTS IN CORNER CASES.

Corner case	NF (dB)	S_{11} (dB)	S_{21} (dB)	IIP3 (dBm)	Power (mW)
FF @ -40°C	1.6-2.8	< -10	15.2-12.6	-9	6.9
TT @ 27°C	2.3-2.8	< -11	13.4-10.6	-5	6
SS@ 85°C	3.2-3.6	< -13	11.4-8.4	0	5.2

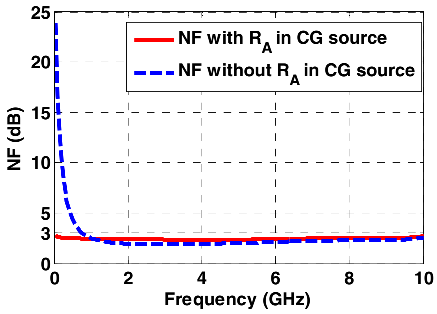

Figure 5: Simulated NF.

To compare the proposed LNA with previous topologies, we used the following figure of merit (FoM) defined in [5], and the results are summarized in Table III.

$$FoM = \frac{Gain_{av}[abs] \times BW[GHz]}{(F_{av} - 1) \times P_{dc}[mW]} \quad (12)$$

where $Gain_{av}$ is the average power gain, F_{av} is the average noise factor over the frequency range and P_{dc} is the power consumption. According to Table III, the proposed LNA achieves a very low noise figure and has very low power consumption. Moreover, by using a series resistor, R_A, the bandwidth is extended, especially in low frequencies.

IV. CONCLUSIONS

In this paper, a 50 MHz-10 GHz wideband LNA for spectral sensing in cognitive radios has been proposed in a 90 nm standard RF-CMOS technology. A new method for extending the bandwidth, especially in low frequencies, is applied which acquits the problem of inductor size in the source of CG stage. In addition, we can nearly achieve 50Ω output impedance by paralleling a resistor with the output node. The simulation results show a flat NF of 2.3-2.8 dB over the whole bandwidth, a peak gain of 13.4 dB with -3 dB bandwidth from 50 MHz to 10 GHz. Furthermore, its S_{11} is less than -10 dB in 10 GHz bandwidth and the IIP3 is about -5 dBm. Finally, it consumes 6 mW from a 1 V power supply.

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TABLE III. COMPARATION OF LNA PERFORMANCE.

Ref.	-3dB BW GHz	NF (dB)	S_{11} (dB)	S_{21} (dB)	IIP3 (dBm)	Power (mW)	FoM	Technology
[1]	0.05-10	2.9-5.9	-10	18-20	-11.2/-7	22	20.5	65 nm
[3]	0.5-14	3.4-5.4	-11	11.5	+10	52	2.15	0.18 µm
[7]	1.2-11.9	4.5-5.1	-11	9.7	-6.2	20	2.487	0.18 µm
[11]*	4.7-11.7	2.88-3	-11.9	12.4	-3	13.5	9.31	0.13 µm
[12]*	3-10.6	5	-10	6	9	N.A.	N.A.	0.18 µm
[13]	0.2-5.2	2.9-3.5	-12	13-16	0	14	9.16	65 nm
This work*	0.05-10	2.3-2.8	-11	13.4-10.6	-5#	6	32.93	90 nm

*Simulation results
#Two-tone RF signals at frequencies of 6 and 6.02 GHz were applied.