A Very Wideband Low Noise Amplifier for Cognitive Radios

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Abstract—In this paper, a new full on-chip CMOS low-noise amplifier (LNA) topology for the range of 50 MHz to 10 GHz is introduced that has very low power consumption. It exploits the combination of a common-gate (CG) stage for wideband input matching and a common-source (CS) stage for canceling the noise and distortion of CG stage. Moreover, the CS stage used both nMOS and pMOS transistors to improve the IIP2. Simulated in a 90 nm RF CMOS technology, the proposed LNA achieves a noise figure of 2.3 dB to 2.8 dB and input return loss (S11) less than -10 dB over the whole bandwidth while consumes only 6 mW from a 1 V power supply. The average of the power gain (S21) is 12 dB. The achieved IIP3 and IIP2 are about -5 dBm and 20 dBm, respectively.

I. INTRODUCTION

Nowadays the idea of “cognitive radios” (CR) has interested scientific because the usage of the cellular and wireless local area network (WLNA) bands has increased. CRs can utilize any unoccupied channel in a wide frequency range, from several of megahertz up to 10GHz but conventional wireless transceivers can be applied in especial bands [1]. Recent effort on CR design has focused on the TV bands below 1 GHz [2], but, CRs will be applied for a much wider spectrum in near future. Because of a large bandwidth, this structure can be applied for wireless personal area networks (WPANs), providing seamless connectivity between consumer electronics devices for transmission of video, audio, and other high-bandwidth data (range of frequency is 3 to 10 GHz) [3]. Also it can be used for TV application (range of frequency is 50 to 900 MHz). The broadband behavior of receiver is determined by the front-end low-noise amplifier.

The design of broadband low noise amplifiers is controlled by tradeoff between input matching, noise figure, gain, bandwidth, linearity, and voltage headroom. There are many possible techniques to design a wide-band low noise amplifier, including common gate amplifiers [4, 5], distributed amplifiers, and negative feedback amplifiers [6]. The choice of topology begins with the input matching requirement. Here, we compare two common wideband matching techniques: a common-source (CS) stage with resistive shunt feedback and a common-gate stage [7]. These two structures are shown in Fig. 1. For having wideband input matching in CS stage, we have to use the resistive feedback which causes to reduce NF and gain. In addition, it consumes high power. But, CG stage can implement broadband impedance matching without many extra components. Moreover, the CG LNA has better linearity, low power consumption, and better input-output isolation [8] although it suffers from the poor noise performance because the $g_{m}$ of this structure should be 20 mA/V for having the input matching condition. A popular method for reduction the noise figure (NF) is the noise cancelation structure which eliminates the channel thermal noise of the CG structure by using a common source (CS) transistor [7].

In this paper, a low power LNA is designed by using the CG structure and the noise cancellation technique which also removes partially the circuit’s nonlinear distortion. In addition, for input matching below 1 GHz, a new technique is introduced. Section II describes the concept of the proposed wideband LNA and the analysis of gain, noise, and input matching are given. Section III describes the simulation results. Finally, the conclusion is presented in Sect. IV.

II. CIRCUIT ANALYSIS AND DESIGN

The proposed LNA is shown in Fig. 2. In this structure, $M_1$ is used as the CG structure for implementing the broadband input matching. In addition, the CS stage, $M_2$, is applied for canceling the channel noise of $M_1$. To reuse the current of $M_2$ and improve the IIP2, $M_3$ is selected as a pMOS transistor. The gate-source parasitic capacitor of $M_1$ is damped by $L_g$ in order to improve the input return loss ($S_{11}$). $L_s$ is used to cancel the degrading effect of the parasitic capacitances of transistors $M_1$ and $M_2$. The gate inductor $L_1$ and drain inductors $L_{D1}$, $L_2$ and $L_3$ are added for inductive shunt-peaking and series-peaking, respectively. The resistor $R_f$ is applied to extend the bandwidth in low frequencies and decrease the flicker noise of $M_1$. In the output node, $R_f$ is paralleled in order to decrease the variation of output impedance and hence to achieve a smooth gain. Finally, we used negative feedback, $R_f$, for preventing the variation of output voltage because the output node is a high impedance node. The value of $R_f$ is selected large in order to ignore its effect in the analysis. In this paper, we ignored $L_{D1}$ and $L_1$ in calculations for simplifying. Part A describes the input matching and bandwidth extension. Noise and gain analysis are explained in parts B and C, respectively. Eventually, part D describes the non-linearity behavior briefly.

A. Input Matching and Bandwidth Extension

To achieve the input matching in 10GHz bandwidth, especially in low frequencies, we have to increase the size of $L_s$ up to 200 nH, because, if the size of $L_s$ decreases the series resistance of $L_s$, due to limited quality factor of $L_s$, will be decreased (approximately up to 5Ω). So, this resistance is...
paralleled with \( Z_1 \). As shown in Fig. 2, \( Z_1 \approx 1/(g_{m1}+g_{m2}) \). So, in \((R_{Ls}+sL_s)\), the \( sL_s \) term can be ignored in low frequencies resulting in a degraded input matching condition below 1.5 GHz. For solving this problem, we put a series resistor, \( R_A \), with \( L_s \); hence, the equivalent impedance is equal to \((R_{Ls}+R_A+sL_s)\). In low frequencies \( R_d \gg (R_{Ls}+sL_s), \approx 1/(g_{m1}+g_{m2}) \). Accordingly, the input impedance approximately equals \( 1/(g_{m1}+g_{m2}) \) in this paper. In the following to take into account the body effect of \( M_1 \) and also to simplify the relations, \( g_{m1} \) stands for \( g_{m1}+g_{m2} \). The input impedance with resistor \( R_A \) is calculated as:

\[
Z_{in} = (R_d + sL_s) \left[ \frac{1}{sC_X} \right] \frac{1}{g_{m1}} = \frac{R_d + sL_s}{C_X L_s^2 + (R_d C_X + g_{m1} L_s) s + (g_{m1} R_d + 1)}
\]

Thus, the poles of \( Z_{in} \) are obtained approximately as:

\[
\omega_{p1} = \frac{R_d C_X + g_{m1} L_s}{R_d L_s}, \quad g_{m1} L_s \gg R_d C_X
\]

\[
\omega_{p2} = \frac{R_d C_X + g_{m1} L_s}{C_X L_s}
\]

where \( C_X \) denotes the parasitic capacitance in node \( X \) and equals to \( C_X = C_{m1} + C_{m2} \) where \( C_{m1} \) is also damped by \( L_s \).

The series resistor, \( R_A \), causes the dominant pole, \( \omega_{p1} \), to move to the upper frequencies, so, the bandwidth in low frequencies is increased. Also, the value of zero is increased. On the other hand, since this zero is located between the two poles, this causes to have a smooth gain. But, increasing the value of \( R_A \) decreases the gain, so, we need to compensate for that in the next stage.

B. Gain Analysis

The equivalent impedance was seen from drain of transistor \( M_1 \) toward the ground is called \( Z_Y \) and calculated as \((R_{D1}+sL_{D1})\) \( Z_{in} \). To convert \((R_{D1}+sL_{D1})\) \( Z_{in} \) to 1/s\( C_Y \) \( Z_{in} \) to \( sC_Y \), \( R_{D1} \) is the source resistance and \( R_d \) is the series resistance with \( L_s \). \( R_{D1} \) and \( L_{D1} \) are the load impedance of \( M_1 \) and \( C_Y \) is the all of parasitic capacitance in node \( Y \). The resistance \( R_{D1} \) is large enough and also the voltage gain of \( M_1 \) is low, approximately 3, so, the effect of \( R_d \) is ignored. \( Z_{out} \) is defined as the output impedance which is calculated as \((r_{ds}+sL_{D1})\) \( Z_{out} \).

\[
A_v = \frac{Z_{in}}{Z_{out}} \left( \frac{g_{m1} g_{m3} [Z_Y + g_{m2}]}{g_{m1} + g_{m2}} \right)
\]

\[
Z_{out} = \frac{L^2 s^2 + A L s + B}{C_{out} L^2 s^3 + A L s + B}
\]

where \( A = r_{ds} + r_{ds}, B = r_{ds} r_{ds} \) and \( L = L_{D1} = L_{D2} \).

By decreasing technology size, for increasing \( f_t \), \( r_{ds} \) is reduced owing to the length channel reduction. Also, because of parasites, the variation of \( r_{ds} \) in high frequencies is increased. According to (5), \( Z_{out} \) has a high value in low frequencies but it falls down in high frequencies. So the variation of gain is increased. For solving this problem, we used the inductive shunt-peaking and series-peaking. The shunt inductive peaking causes a resonance at output of each stage when the gain starts to roll off at higher frequencies, because, the parasites of the output nodes of each stage are damped by these inductors [9]. Drain inductors in output node, \( L_{D1}, \) cause the \( S_{11} \) to be deteriorated. So we put an inductor, \( L \), in gate of CG stage for damping the parasites of \( M_1 \) in order to improve the input matching. Moreover, \( R_d \) is paralleled in output node which its value is near to the value of \( Z_{out} \) at low frequencies, so it affects more in low frequencies and decreases the variation of the output impedance. As a result, there is less variation in the LNA gain, although, the gain is decreased at low frequencies.

C. Noise Analysis

The purpose of noise cancelation is to decouple the input matching with the NF by canceling the output noise from the matching device [10]. The current noise of input transistor flows into node \( X \) but out of node \( Y \) that creates two voltages with opposite phases. These two voltages are converted to current by \( M_2 \) and \( M_3 \). But, the input signal in these two nodes has the same phases. Thus the input signal is boosted at the output node which its value is near to the value of \( Z_{out} \) for damping the parasites of \( M_1 \) in order to improve the input matching. Moreover, \( R_d \) is paralleled in output node which its value is near to the value of \( Z_{out} \) at low frequencies.
According to Fig. 2, for simplifying. We suppose that important sources of noise are: 1) thermal noise of $M_2$, 2) channel noise of $M_2$, 3) channel noise of $M_3$. They are calculated as (7-10), respectively. We have also supposed that $R_s = 1/g_{m1}$ in order to simplify the relations.

$$NF_{R_{D1}} = \frac{4kT}{R_{D1}} \left( \frac{g_{m3} V_{out}^2}{4kTR_{D1}} \right)^2$$

$$\cong \frac{R_{D1} R_s}{|Z_{in} + R_{D1}|^2}$$

According to Fig. 2, $Z_{in} = [r_{d1} + (R_s (r_{sd} L_s)) (1 + g_{m1} r_{d1})].$

$$NF_{R_s} = \frac{4kT R_{D1} (2A_v)^4}{\left( \frac{Z_{in}}{R_s} \right)}$$

According to Fig. 2, $Z_{11}$ is calculated as $(Z_{11} + r_{d1})(1 + g_{m1} r_{d1})$, for simplifying. We suppose that $Z_{11} = 1/g_{m1}$.

$$NF_{M2} = \frac{4kT g_{m2} Z_{out}^2}{4kTR_{D1} A_v^2}$$

$$\cong \frac{g_{m2}}{R_s \left( Z_{11} g_{m3} + g_{m2} \right)^2} \alpha \equiv \frac{1}{R_s} \frac{g_{m2}}{\alpha}$$

$$NF_{M3} = \frac{4kT g_{m3} Z_{out}^2}{4kTR_{D1} A_v^2}$$

$$\cong \frac{g_{m3}}{R_s \left( Z_{11} g_{m3} + g_{m2} \right)^2} \alpha \equiv \frac{R_s}{g_{m3}}$$

Finally, the total NF of the proposed LNA is given by:

$$NF = \frac{R_{D1} R_s}{|Z_{in} + R_{D1}|^2} + \frac{1}{R_s g_{m2}} \alpha + \frac{R_s}{Z_{11}} + \frac{R_s}{g_{m3}} \alpha$$

According to (11), for decreasing the thermal noise of $R_{D1}$ and $R_s$, their value should be increased, but, this is limited by voltages that drop on $R_{D1}$ and $R_s$. In addition, the channel noise of $M_2$ and $M_1$ can be decreased by increasing $g_{m1}$ and $g_{m3}$, respectively.

D. Non Linearity

The non-linearity of CS transistor is worse than the CG transistor. In this case, we used the pMOS-nMOS structure in the output stage to improve the values of IIP2 and IIP3. In this method, the input pMOS and nMOS transistors are biased in a way that each transistor expunges the IIP2 of other one [5]. It means that the IIP2 summation of these two transistors counteract each other effects in range of voltage bias.
Two-tone RF signals at frequencies of 6 and 6.02 GHz were applied. Simulation results and the results are summarized in Table III.

In this paper, a 50 MHz-10 GHz wideband LNA for spectral sensing in cognitive radios has been proposed in a 90 nm CMOS technology. A new method for extending the bandwidth, especially in low frequencies, is applied which acquires the problem of inductor size in the source of CG stage. In addition, we can nearly achieve 50Ω output impedance by paralleling a resistor with the output node. The simulation results show a flat NF of 2.3-2.8 dB over the whole bandwidth, a peak gain of 13.4 dB with -3 dB bandwidth from 50 MHz to 10 GHz. Furthermore, its $S_11$ is less than -10 dB in 10 GHz bandwidth and the IIP3 is about -5 dBm. Finally, it consumes 6 mW from a 1 V power supply.

### IV. CONCLUSIONS

In this paper, a 50 MHz-10 GHz wideband LNA for spectral sensing in cognitive radios has been proposed in a 90 nm CMOS technology. A new method for extending the bandwidth, especially in low frequencies, is applied which acquires the problem of inductor size in the source of CG stage. In addition, we can nearly achieve 50Ω output impedance by paralleling a resistor with the output node. The simulation results show a flat NF of 2.3-2.8 dB over the whole bandwidth, a peak gain of 13.4 dB with -3 dB bandwidth from 50 MHz to 10 GHz. Furthermore, its $S_11$ is less than -10 dB in 10 GHz bandwidth and the IIP3 is about -5 dBm. Finally, it consumes 6 mW from a 1 V power supply.

### TABLE I. DESIGNED VALUES OF THE LNA.

<table>
<thead>
<tr>
<th>Transistor size</th>
<th>(W/L)$_1$</th>
<th>(W/L)$_2$</th>
<th>(W/L)$_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>90 nm 10×5 µm</td>
<td>3.2-3.6</td>
<td>-13</td>
<td>11.4-8.4</td>
</tr>
<tr>
<td>65 nm 10×5 µm</td>
<td>2.3-2.8</td>
<td>-11</td>
<td>13.4-10.6</td>
</tr>
<tr>
<td>65 nm 300×5 µm</td>
<td>1.6-2.8</td>
<td>-10</td>
<td>15.2-12.6</td>
</tr>
</tbody>
</table>

### TABLE II. SIMULATED RESULTS IN CORNER CASES.

<table>
<thead>
<tr>
<th>Corner case</th>
<th>NF (dB)</th>
<th>$S_{11}$ (dB)</th>
<th>$S_{21}$ (dB)</th>
<th>NF3 (dBm)</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF @ -40°C</td>
<td>-10.2</td>
<td>15.2-12.8</td>
<td>-9</td>
<td>6.9</td>
<td></td>
</tr>
<tr>
<td>TT @ 27°C</td>
<td>-11.0</td>
<td>13.4-10.6</td>
<td>-5</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>SS @ 85°C</td>
<td>-12.4</td>
<td>11.4-8.4</td>
<td>-1</td>
<td>5.2</td>
<td></td>
</tr>
</tbody>
</table>

To compare the proposed LNA with previous topologies, we used the following figure of merit (FoM) defined in [5], and the results are summarized in Table III.

$$FoM = \frac{Gain_{av}[dBm] \times BW [GHz]}{(F_{av} - 1) \times P_{dc} [mW]}$$

(12)

where $Gain_{av}$ is the average power gain, $F_{av}$ is the average noise factor over the frequency range and $P_{dc}$ is the power consumption. According to Table III, the proposed LNA achieves a very low noise figure and has very low power consumption. Moreover, by using a series resistor, $R_s$, the bandwidth is extended, especially in low frequencies.

### IV. CONCLUSIONS

In this paper, a 50 MHz-10 GHz wideband LNA for spectral sensing in cognitive radios has been proposed in a 90 nm standard RF-CMOS technology. A new method for extending the bandwidth, especially in low frequencies, is applied which acquires the problem of inductor size in the source of CG stage. In addition, we can nearly achieve 50Ω output impedance by paralleling a resistor with the output node. The simulation results show a flat NF of 2.3-2.8 dB over the whole bandwidth, a peak gain of 13.4 dB with -3 dB bandwidth from 50 MHz to 10 GHz. Furthermore, its $S_11$ is less than -10 dB in 10 GHz bandwidth and the IIP3 is about -5 dBm. Finally, it consumes 6 mW from a 1 V power supply.

### TABLE III. COMPARISON OF LNA PERFORMANCE.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>-3dB BW (GHz)</th>
<th>NF (dB)</th>
<th>$S_{11}$ (dB)</th>
<th>$S_{21}$ (dB)</th>
<th>NF3 (dBm)</th>
<th>Power (mW)</th>
<th>FoM</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>0.05-10</td>
<td>2.9-5.9</td>
<td>-10</td>
<td>18-20</td>
<td>11.2-7</td>
<td>2</td>
<td>20.5</td>
<td>65 nm</td>
</tr>
<tr>
<td>[3]</td>
<td>0.5-14</td>
<td>3.4-5.4</td>
<td>-11</td>
<td>11.5</td>
<td>-10</td>
<td>+10</td>
<td>2.15</td>
<td>0.18 µm</td>
</tr>
<tr>
<td>[7]</td>
<td>1.2-11.9</td>
<td>4.5-5.1</td>
<td>-11</td>
<td>9.7</td>
<td>-6.2</td>
<td>20</td>
<td>2.487</td>
<td>0.18 µm</td>
</tr>
<tr>
<td>[11]*</td>
<td>4.7-11.7</td>
<td>2.88-3.3</td>
<td>-11.9</td>
<td>12.4</td>
<td>-3</td>
<td>13.5</td>
<td>9.31</td>
<td>0.13 µm</td>
</tr>
<tr>
<td>[12]*</td>
<td>3-10.6</td>
<td>5</td>
<td>-10</td>
<td>6</td>
<td>9</td>
<td>N.A.</td>
<td>N.A.</td>
<td>0.18 µm</td>
</tr>
<tr>
<td>[13]</td>
<td>0.2-5.2</td>
<td>2.9-3.5</td>
<td>-12</td>
<td>13-16</td>
<td>0</td>
<td>14</td>
<td>9.16</td>
<td>65 nm</td>
</tr>
<tr>
<td>This work</td>
<td>0.05-10</td>
<td>2.3-2.8</td>
<td>-11</td>
<td>13.4-10.6</td>
<td>-5</td>
<td>6</td>
<td>12.93</td>
<td>90 nm</td>
</tr>
</tbody>
</table>

*Simulation results
#Two-tone RF signals at frequencies of 6 and 6.02 GHz were applied.

REFERENCES


