A Comprehensive Analysis of the Noise Power of Three-Stage OTAs in Switched-Capacitor Circuits

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***Abstract*— In this paper, a comprehensive analysis of the noise power of three-stage amplifiers is presented. It is found that the noise power of each stage at the output of the amplifiers, depending on the type of compensation structure, could have different conditions. In some of the three-stage amplifiers, because of the compensation structure, the noise power contribution of the first stage is dominant, and in others the noise power contribution of the second stage. To demonstrate the validity and the correctness of this analysis, the reversed nested Miller compensation (RNMC) and the damping factor control frequency compensation (DFCFC) amplifiers are designed in a 90 nm CMOS technology using HSPICE and circuit-level simulation results are provided, which show, for the RNMC and DFCFC amplifiers, the first stage and second stage noise contribution is dominant, respectively.**

***Keywords*— CMOS three-stage operational amplifiers, reversed nested Miller compensation, damping factor control frequency compensation, switched-capacitor circuits, circuit noise power.**

I. Introduction

The operational transconductance amplifier (OTA) is a vital and basic building block in analog-to-digital (A/D) converter circuits. Fast and high DC gain OTAs are needed to realize fast and high accuracy switched-capacitor (SC) circuits in A/D converters [1]. On the other hand, with the CMOS technology scaling, the inherent DC gain ($g_m r_o$) of the transistors and the power supply voltage are decreased and the design of high DC gain and large output swing amplifiers becomes more challenging. Hence, to achieve simultaneously high DC gain and large output swing in nano-meter CMOS technologies, the multi-stage amplifiers like three-stage OTAs, has been used [2]. On the other hand, owing to the increase in the poles and zeros frequency of the three-stage amplifier, the closed-loop stability becomes very critical. Several methods have been presented in the frequency compensation of three-stage OTAs including nested Miller compensation (NMC) and reversed nested Miller compensation (RNMC) schemes [3].

To improve the frequency response of the three-stage amplifiers, several variants of the basic NMC and RNMC schemes have been proposed such as feed-forward transconductance stages [3, 4], damping factor control frequency compensation (DFCFC) [5], active feedback stages [6-8], ac boosting amplifiers [9] and other several methods which are presented in literature. The majority of these methods are mainly proposed for low-speed applications that have a large output load capacitance where the required gain bandwidth is small. In high-speed switched-capacitor circuits, the load capacitance is small and the output must be settled within a desired time with a specific settling accuracy.

Noise power is one of the important parameters in OTAs and one of the limiting factors in high accuracy A/D converters. As a result, the signal-to-noise ratio (SNR) is one of the most important parameters in these applications. The OTAs that are used in high accuracy A/D converters must meet the required SNR. Hence, the analysis and calculating of the noise power is necessary. The noise analysis of the first-order circuits is straightforward. However, in three-stage OTAs, the noise transfer functions (NTFs) of the amplifier stages are at least third order, and as a result, the noise power relations are complicated. In [10], the NTFs of the stages of a three-stage NMC amplifier are calculated but a comprehensive analysis is not presented for these NTFs. In [11], a comprehensive noise analysis has been done on the three-stage NMC amplifier and it has been shown that in the NMC amplifier, not only the first stage noise power contribution at the output of the amplifier is not higher than the second stage noise power contribution, but also the noise power contribution of the second stage is more dominant and have the maximum noise power contribution at the amplifier output.

Similar to the noise power contribution of each stage at the NMC amplifier output in [11], in this paper, the noise power contribution of each stage at the output of the other three-stage amplifiers are considered and a comprehensive analysis is given. It was found that the noise power of each stage at the output of the amplifiers, depending on the type of the compensation structure, could have different conditions. For example, in [11], the noise power contribution of the second-stage is dominant since there is a low-frequency LHP zero in its second-stage NTF and it raises the magnitude of this NTF and causes a peaking at high frequencies. In this paper, a comprehensive analysis of the noise power of the three-stage amplifiers with the RNMC and DFCFC structures is performed and it is shown in the RNMC and DFCFC amplifiers, the first and the second stage noise contribution is dominant, respectively.

II. Small-Signal Modelling of The RNMC and DFCFC Amplifiers

In the NMC amplifier, the compensation capacitors are connected to the amplifier output, and hence, the output capacitor becomes large and the bandwidth is decreased. To overcome this problem, the RNMC compensation structure has been proposed. On the other hand, the C_{m2} capacitor in the NMC and RNMC amplifiers lowers the natural frequency of the non-dominant complex poles. Therefore, to push the non-dominant poles into high frequencies and extend the gain-bandwidth, more power must be consumed.

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To solve this problem, the DFCFC structure has been proposed. The block diagram of the three stages RNMC and DFCFC OTAs are shown in Fig. 1. By assuming high dc gain in amplifier stages and compensation and load capacitors are much greater than all parasitic capacitances of the circuit, i.e. $g_{mi}r_{oi} >> 1$ and C_L, C_{m1}, $C_{m2} >> C_{1,2}$, the closed-loop signal transfer function of the RNMC and DFCFC amplifiers are given by:

$$H(s)_{RNMC} = \frac{A_{dc}}{1+\beta A_{dc}} \frac{1 - s\frac{C_{m_2}}{g_{m_2}} - s^2\frac{C_{m_1}C_{m_2}}{g_{m_2}g_{m_3}}}{D(s)_{,RNMC}} \quad (1)$$

$$H(s)_{DFCFC} = \frac{A_{dc}}{1+\beta A_{dc}} \frac{1 - \frac{C_{m1}g_{m4}}{g_{m2}g_{m3}}s - \frac{C_{m1}C_2}{g_{m2}g_{m3}}s^2}{D(s)_{,DFCFC}} \quad (2)$$

where β is the feedback factor, $A_{dc}=g_{m1}r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}$ is the dc gain of the both RNMC and DFCFC OTAs and $D(s)_{RNMC}$ and $D(s)_{DFCFC}$ are given by:

$$D(s)_{,RNMC} = 1 + s\left(\frac{C_{m_1}}{\beta g_{m_1}} - \frac{C_{m_2}}{g_{m_2}}\right) + s^2\left(\frac{C_{m_1}\left(g_{m_2}C_L - g_{m_3}C_{m_1}\right)}{\beta g_{m_1}g_{m_2}g_{m_3}}\right) + s^3\frac{C_{m_1}C_{m_2}C_L}{\beta g_{m_1}g_{m_2}g_{m_3}}$$

$$D(s)_{,DFCFC} = 1 + \left(\frac{C_{m1}}{\beta g_{m1}} - \frac{C_{m1}g_{m4}}{g_{m2}g_{m3}}\right)s + \frac{C_LC_{m1}g_{m4}}{\beta g_{m1}g_{m2}g_{m3}}s^2 + \frac{C_{m1}C_2C_L}{\beta g_{m1}g_{m2}g_{m3}}s^3$$

There are two zeros in RNMC and DFCFC transfer functions and it can be easily shown that the gain-bandwidth improvement is given by:

$$\frac{\omega_{GBW,DFCFC}}{\omega_{GBW,NMC}} = \sqrt{\frac{C_{m2,NMC}}{C_2}} \quad (3)$$

According to (3), it is clear that for equal power consumption, the gain-bandwidth of the DFCFC amplifier is much larger than the gain-bandwidth of the NMC and RNMC OTAs, which indicates that the DFCFC amplifier is more suitable for switched-capacitor circuits.

A typical fully-differential circuit implementation of the RNMC and DFCFC OTAs is shown in Fig. 2 where the stages of both OTAs are realized by three differential pairs with active loads. The DFC block in DFCFC amplifier is also realized by a differential pair with an active load.

III. Noise Analysis

The channel thermal noise is the most significant noise source in MOS transistors. This noise source can be modelled by a current source between the drain and source terminals for the MOS transistors that operating in the saturation region [12]. The small-signal noise model of the three-stage RNMC and DFCFC amplifiers are shown in Fig. 3 where the noise of each stage is modelled by a current source and the amplifiers are utilized in the negative feedback with the feedback factor of β. To calculate the noise power at the output, firstly, the NTF of each stage to the output must be obtained, and then by integrating it, the noise power at the output is calculated. The noise power spectral density (PSD) of the first stage amplifiers is given by:

$$\overline{I^2_{n1,RNMC}} = \overline{I^2_{n1,DFCFC}} = 4kT\gamma(g_{m1} + g_{m3,4}) \quad (4)$$

where k, T, and γ represent the Boltzmann's constant, absolute temperature, and excess noise coefficient of MOS transistors, respectively, and $g_{m3,4}$ is the transconductance of M_3 and M_4 transistors shown in Fig. 2. The NTF of the first stage amplifiers are given by:

$$H_{n1}(s)_{,RNMC} = \frac{V_{n,out}}{I_{n1}} = \frac{1}{\beta g_{m_1}} \frac{1 - s\frac{C_{m_2}}{g_{m_2}} - s^2\frac{C_{m_1}C_{m_2}}{g_{m_2}g_{m_3}}}{D(s)_{,RNMC}} \quad (5)$$

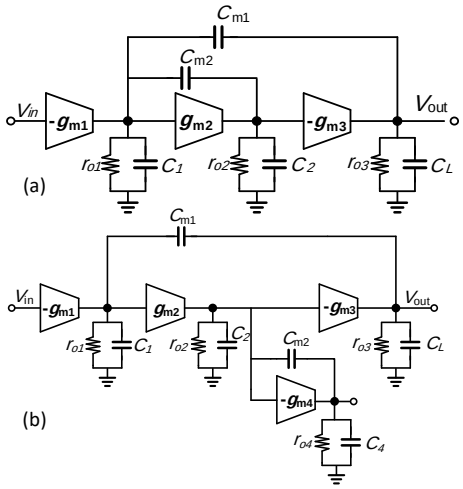

Fig. 1. Block diagram of the (a) RNMC and (b) DFCFC amplifiers.

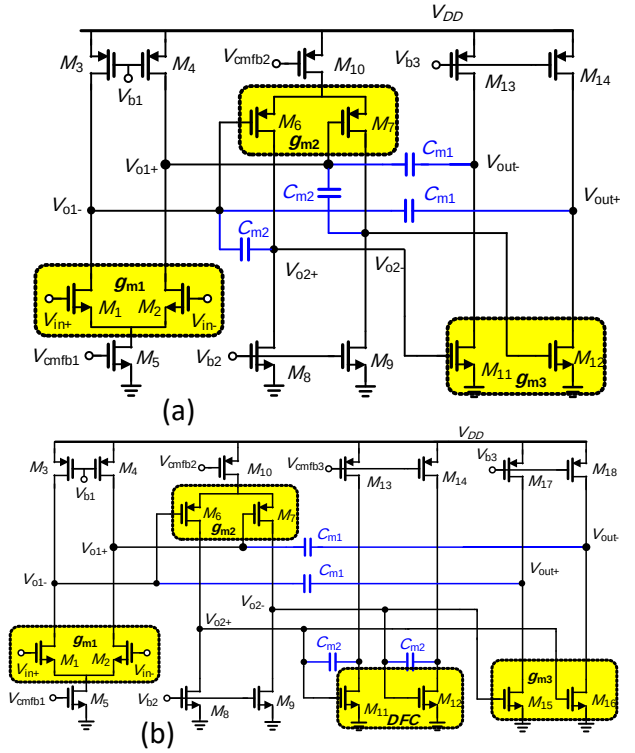

Fig. 2. A typical fully-differential circuit implementation of three-stage (a) RNMC and (b) DFCFC OTAs (bias and CMFB circuits are not shown for simplicity).

$$H_{n1}(s)_{,DFCFC}=\frac{V_{n,out}}{I_{n1}}=\frac{1}{\beta g_{m_1}}\frac{1-s\dfrac{C_{m_1}g_{m4}}{g_{m_2}g_{m3}}-s^2\dfrac{C_{m_1}C_2}{g_{m_2}g_{m_3}}}{D(s)_{,DFCFC}} \quad (6)$$

Now by integrating the product of the noise PSD with the squared NTF magnitude, the noise contribution of both first stage amplifiers at the output is obtained as follows [13]:

$$SN_{out,1}=2\left[\overline{I^2_{n1}}\int_0^{\infty}\left|H_{n1}(f)\right|^2 df\right] \quad (7)$$

The factor of 2 is due to the fully-differential circuit of both amplifiers. The first stage noise is only a part of the total output amplifier noise. The noise contribution of the second stage amplifier at the output can be also calculated similarly.

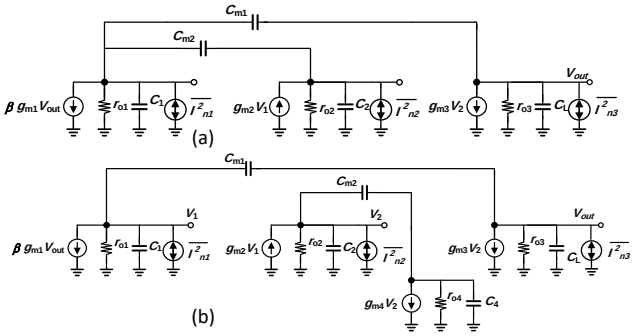

Fig. 3. Small-signal noise model of the three-stage (a) RNMC and (b) DFCFC amplifiers in the closed-loop configuration.

Therefore, the noise PSD and the NTF of the second stage at the output are given by:

$$\overline{I^2_{n2,RNMC}}=\overline{I^2_{n2,DFCFC}}=4kT\gamma(g_{m2}+g_{m8,9}) \quad (8)$$

$$H_{n2}(s)_{,RNMC}=\frac{V_{n,out}}{I_{n2}}=\frac{1}{\beta A_{v1}g_{m_2}}\frac{(1+r_{o1}(C_{m_1}+C_{m_2})s+s^2\dfrac{C_{m_1}C_{m_2}r_{o1}}{g_{m_3}})}{D(s)_{,RNMC}} \quad (9)$$

$$H_{n2}(s)_{,DFCFC}=\frac{V_{n,out}}{I_{n2}}=\frac{1}{\beta A_{v1}g_{m_2}}\frac{(1+r_{o1}C_{m1}s)}{D(s)_{,DFCFC}} \quad (10)$$

In (8), $g_{m8,9}$ is the transconductance of the $M_{8,9}$ transistors in Fig. 2. Both NTFs have a zero at low frequencies, and other zeros are at very high frequencies ($\omega_{z,RNMC}=g_{m1}/(A_{v1}(C_{m1}+C_{m2}))$, $\omega_{z,DFCFC}=g_{m1}/(A_{v1}C_{m1})$). Assuming $A_{v1}>>1$, we can replace the low-frequency zero with a zero at the origin, and thus the noise NTF for the second stage of amplifiers are approximated as follows:

$$H_{n2}(s)_{,RNMC}=\frac{1}{\beta g_{m1}r_{o1}g_{m_2}}\frac{sr_{o1}(C_{m_1}+C_{m_2})}{D(s)_{,RNMC}}=\frac{(C_{m_1}+C_{m_2})}{\beta g_{m1}g_{m_2}}\frac{s}{D(s)_{,RNMC}} \quad (11)$$

$$H_{n2}(s)_{,DFCFC}=\frac{1}{\beta A_{v1}g_{m_2}}\frac{(1+sr_{o1}C_{m1})}{D(s)_{,DFCFC}}=\frac{C_{m1}}{\beta g_{m1}g_{m2}}\frac{s}{D(s)_{,DFCFC}} \quad (12)$$

It is shown in [11] that the second stage noise contribution at the NMC amplifier output, although it is divided by the dc gain of the first stage, is still significant and even more than the noise contribution of the first stage. This is because of the low-frequency LHP zero that causes a peaking at high frequencies. According to (11) and (12), it is evidence that both NTFs, like the second stage NTF in the NMC amplifier, has a zero at low frequencies that create a peak in the second stage noise power, and it is expected that the second stage noise contribution at the output of these two amplifiers is also larger than the noise contribution of the first stage. However, to satisfy the closed-loop stability in the RNMC amplifier, the transconductance of the second stage is much larger than the transconductance of the second stage in the NMC and DFCFC amplifiers. As a result, it is expected that the second stage noise contribution in the RNMC amplifier to be negligible and the noise contribution of the second stage at the DFCFC output to be significant as the NMC amplifier. Finally, the noise contribution of the third stage amplifiers can be obtained similarly. Their PSDs and NTFs are given by:

$$\overline{I^2_{n3,RNMC}}=4kT\gamma(g_{m3}+g_{m13,14}) \quad (13)$$

$$\overline{I^2_{n3,DFCFC}}=4kT\gamma(g_{m3}+g_{m17,18}) \quad (14)$$

$$H_{n3}(s)_{,RNMC}=\frac{C_{m_2}}{\beta g_{m1}g_{m_3}}\frac{s}{D(s)_{,RNMC}} \quad (15)$$

$$H_{n3}(s)_{,DFCFC}=\frac{C_{m2}}{\beta g_{m2}g_{m_3}}\frac{s}{D(s)_{,DFCFC}} \quad (16)$$

It is be noted that the NTF relations (15) and (16) are simplified by neglecting the high frequency zeros and replacing the low frequency zeros with a zero in the origin. In the relations (13) and (14), $g_{m13,14}$ and $g_{m17,18}$ are the transconductances of the $M_{13,14}$ and $M_{17,18}$ transistors, respectively, that are shown in Fig. 2. As expected, the NTF of the third stage is divided by the dc gain of the first and second stages. Both NTFs have a zero at low frequencies that generate a peek at their frequency response, while the third stage NTF in the NMC amplifier in [11] has two low-frequency zeros. Therefore it is expected that the third stage noise contribution at the output of the RNMC and DFCFC amplifiers is lower than the third stage noise contribution at the NMC amplifier output. As a result, the noise contribution of the third stages is mainly due to these low-frequency zeros. In the absence of these zeros and considering a high dc gain in the first and second stages, it is expected that the third stage noise contribution at the output of the amplifiers will be negligible. Finally, the total integrated noise power of both amplifiers is obtained by summing up the noise power of the amplifier stages:

$$S_{N,out}=S_{N,out,1}+S_{N,out,2}+S_{N,out,3} \quad (17)$$

As a conclusion for this section, it is expected that in the DFCFC amplifier like the NMC amplifier, the noise contribution of the second stage at the output will be significant, while this value is insignificant at the RNMC amplifier output.

IV. Circuit Level Simulation Results

To prove the validity of the obtained relationships, the results of circuit-level simulations are provided using HSPICE and a 90 nm CMOS technology. The OTAs are employed in a fully-differential flip-around S/H

configuration shown in Fig. 4, that is used in an 11-bit pipelined ADC with 2 V_{pp} differential input signal, 50 MHz sampling frequency and a sampling capacitor of C_s = 1 pF. The power supply is 1.2 V and the effective load capacitor C_L = 2 pF. Both amplifiers were designed for settling times of less than 10 ns and low power consumption. To achieve large output signal swing and sufficient linearity, all devices are biased in strong inversion with an effective overdrive voltage (V_{eff}) about 150mV [11, 13, 14]. The final dimensions of devices in both amplifiers are reported in Table 1. To make the transconductance of the transistors independent on the power supply voltage, as well as the temperature and process variations, a constant-g_m biasing circuit has been used [12].

To provide information on the system stability, the step response and the frequency response of the amplifiers should be simulated. Fig. 5 shows the simulated amplifier settling response in different process corner cases and temperature variations when a 1 V step is applied into the amplifier's input. Fig. 6 shows the simulated open-loop frequency-response of the amplifiers, which indicates the amplifiers have a sufficient phase margin. The simulation results are summarized in Table 2.

Frequency domain simulations have been performed to verify the validity of the analysis of noise of each stage at the amplifier's output. The PSD noise of each stage at the output of amplifiers is simulated and is finally compared. The PSD noise of each stage at the amplifier's output is shown in Fig. 7. As it is expected, the noise PSD of the third stage is lower than the first and second stages. Because there are two low-frequency zeros in the NMC third stage NTF, and one low frequency zero in the RNMC and DFCFC third stage NTFs, the peak created in the NMC third stage NTF frequency response is larger than the RNMC and the DFCFC amplifiers.

As shown in Fig. 7, the analysis is well confirmed with the simulation results. Table 3 shows the noise contribution of each stage at the output of each amplifier. As it is seen from Table 3, the DFCFC amplifier, at the lower power consumption, has better conditions in the case of settling time and bandwidth. On the other hand, it is in the worst condition in the noise power case, which is due to the extra stage DFC block in the OTA. In the case of noise power, the RNMC amplifier has the best conditions. The lower power consumption in the DFCFC amplifier helps to prove the relation (3). Where it's said, the DFCFC amplifier, with less power consumption, could give bandwidth and speed nearly equal to the NMC.

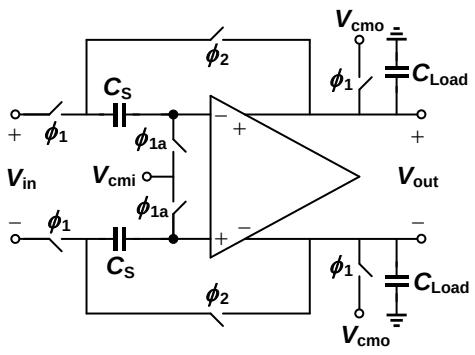

Fig. 4. A Fully-differential flip-around S/H.

Table 1: Simulated device parameters.

Parameter	RNMC	DFCFC
M_1, M_2	1×4 µm/0.2 µm	3×1.5µm/0.2µm
M_3, M_4	5×4.6 µm/0.3 µm	3×6.5 µm/0.3 µm
M_5	2×4 µm/0.2 µm	6×1.5 µm/0.2 µm
M_6, M_7	12×11.6 µm/0.2µm	3×4.7 µm/0.2 µm
M_8, M_9	12×4.5 µm/0.3µm	3×1.7 µm/0.3 µm
M_{10}	24×11.3 µm/0.2 µm	6×4.7 µm/0.2 µm
M_{11}, M_{12}	2×3 µm/0.2 µm	15×2 µm/0.2 µm
M_{13}, M_{14}	8×5 µm/0.3 µm	14×12µm/0.2µm
$M_{15,16}$	-	2×2 µm/0.2 µm
$M_{17,18}$	-	2×12 µm/0.3 µm
C_{m1}, C_{m2} (pF)	1, 0.35	0.8, 0.3
C_L (pF)	2.0	2.0

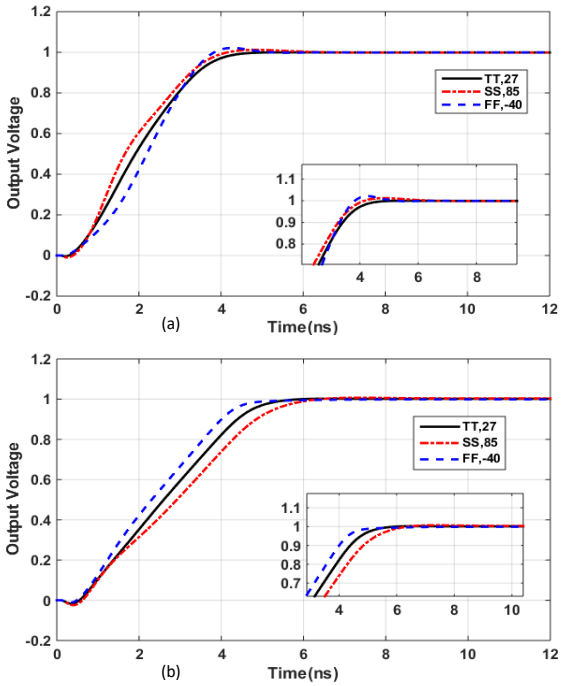

Fig. 5. Step response of three-stage (a) RNMC and (b) DFCFC amplifiers with a 1 V differential input step.

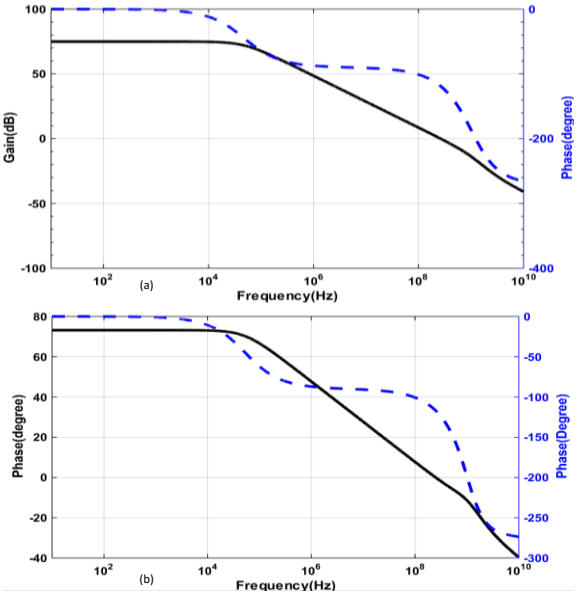

Fig. 6. Open-loop frequency response of the simulated three-stage (a) RNMC and (b) DFCFC amplifiers.

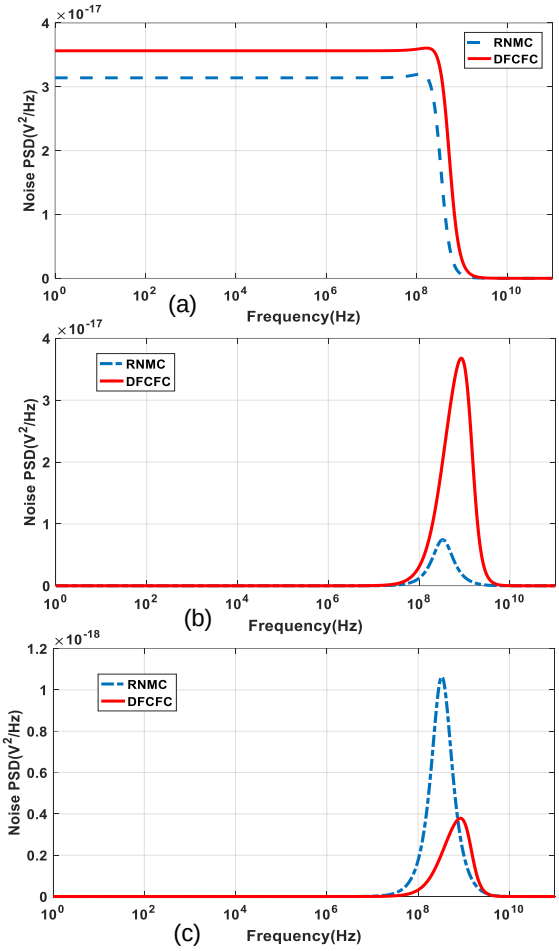

Fig. 7. The simulated PSD noise of the (a) first stage, (b) second stage, and (c) third stage at the output of the amplifiers.

Table 2: Simulation results and comparison with different OTAs.

Parameter	NMC [9]	RNMC	DFCFC
DC gain (dB)	72.1	72.7	73.2
f_{GBW} (MHz)	202.8	220.8	249.7
Phase margin	63.2	62.3	63.07
0.02% settling time, t_s (ns) @ 1 V input step	8.7	7.3	8.3
0.02% Small signal settling time, t_{ss}(ns)@ 100 mV input step	4.7	4.25	3.8
Power dissipation (mW)	5.2	4.05	3.0
Total integrated noise (nV^2)	43.6	15	62
Slew Rate (V/μs)	250.1	285.6	252.2
FoM_S (MHz × pF/ mW)	78	109.03	166.4
FoM_L (V/μs × pF/ mW)	96.1	141.03	168.1
C_L (PF)	2	2	2
C_{m1}, C_{m2}	1.4, 0.9	1.0 , 0.3	0.8, 0.3
Supply (V)	1.2	1.2	1.2

Table 3: Noise contribution of each stage at the output of the amplifiers.

Parameter	NMC [9]	RNMC	DFCFC
First stage noise	15.4 nV^2 (35.3%)	12.8nV^2 (80%)	20.2 nV^2 (24.2%)
Second stage noise	19.4 nV^2 (44.5%)	2.4 nV^2 (16%)	51.3 nV^2 (74.2%)
Third stage noise	8.8 nV^2 (20.2%)	0.75 nV^2 (4%)	0.55 nV^2 (1.6%)
Total integrated noise	43.6 nV^2	16 nV^2	72 nV^2

V. Conclusion

In this paper, a comprehensive analysis of the noise power of the three-stage amplifiers has been made. It is shown that the noise power of each stage at the output of the amplifiers, depending on the type of the compensation structure, could have different conditions. It means that in some of the three-stage amplifiers, the noise contribution of the first stage is dominant, and in others the noise power contribution of the second stage. For example, it has been shown that in the RNMC and DFCFC amplifiers the first and the second stages noise contribution are dominant, respectively.

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