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A 14-bit SAR ADC with Calibration for Comparator Offset and Capacitive DAC Mismatch

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***Abstract*— In this paper, A SAR ADC calibration method is proposed that compensates for comparator and DAC non-idealities. The presented method is both foreground and background. The comparator calibration uses a weight balance logic for the foreground phase and a body bias controller for the background phase; also, capacitive DAC utilizes a self-calibration method in the foreground and a correlation-based method in the background phase. Self-calibration is done by exploiting the main DAC capacitors, and the correlation-based calibration method is realized by an internal redundancy dithering (IRD) with a reference ADC that removes input voltage before calibration starts. The proposed method systematic simulations have been done using a Matlab code that assumes a constant arbitrary value for comparator offset and a zero-mean normal distribution with 1% standard-deviation for capacitor mismatches. Results show that we have achieved 29.51 dB and 39.07 dB improvement in signal-to-noise and distortion (SNDR) and spurious-free dynamic range (SFDR), respectively.**

Keywords*— *SAR ADC, foreground and background calibration, comparator, capacitive DAC.

I. Introduction

Nowadays, successive approximation register (SAR) Analog-to-Digital converters (ADCs) are widely used in power-limited applications because of their high energy efficiency. Another obvious feature of these ADCs is their maximum digitally structure, benefits from the scaling of advanced CMOS technologies. Overall, SAR ADCs are the best choice for moderate conversion speed and moderate resolution applications. Also, it is necessary to notify recent invented techniques like time-interleaving (for speed) and calibration or noise-shaping (for resolution) have made this ADC useable for high speed and resolution applications [1-2].

It is well known that digital circuits have negligible unwanted effects than analog circuits [3]; thus, we focus on the analog part of the SAR ADC for calibration, including comparator and DAC. The most limiting circuit effects for comparators are noise and offset [4]. The main block we must consider its behavior is DAC and, it is because of its various structures and different limiting circuit effects caused by the selected structure. Different types of capacitive DACs mostly suffer from capacitor mismatch, finite settling time, and parasitic effects [3]. Between mentioned non-idealities for DAC, capacitors mismatches are more considerable compared to others, and this is more tangible for moderate to high resolution and newer technologies. All of these effects can be mathematically modeled and used for systematic simulation [4-6].

In this research, we have proposed a calibration method that helps us achieve a better resolution by suppressing the comparator's offset and capacitive DAC mismatches. Our method is a combination of foreground and background calibration. The foreground part first lowers unwanted effects to small values, and after that background calibration, compensates for them to their minimum achievable values. Background calibration can follow PVT effects caused by environmental changes and process variations. Although the foreground part of the calibration adds latency to the calibration process, it helps us achieve significantly small non-idealities and overall a fast function.

For comparator offset, the foreground part is realized by a weight balance logic, which reduces offset to less than ±4 LSBs, and background calibration uses a body bias controller, which lowers offset to less than ±0.5 LSB. DAC mismatch also has the same process for calibration. A self-calibration process reduces capacitor mismatches to less than ±1 LSB using low-value capacitors of the main DAC. An adaptive loop using a dithering method calibrates the 5 most significant bits in the background.

The rest of the paper is organized as follows: In Sect. II, the analysis and models for non-ideal effects limiting our designed ADC, are described. Sect. III completely presents our proposed method. In Sect. IV, the system-level simulation results are provided. Sect. V concludes the paper, finally.

II. Models for Non-ideal Factors

As we mentioned in the introduction, the most important non-ideal factors belong to the ADC's DAC and comparator; therefore, they're discussed in following parts. Fig. 1 illustrates a common charge-redistribution SAR ADC, and also C_P is used for modeling of parasitic capacitors and will be discussed later. Fig. 2 shows a comparator with its distractive parameters.

A. Comparator Unwanted Factors

a. The first unwanted factor that we consider in a comparator is its offset. It is a roughly constant voltage added to the comparator's input terminals, and it changes slightly during ADC function.

b. The second limiting factor for a comparator is noise. Noise analysis for SAR ADCs has been well discussed in [4].

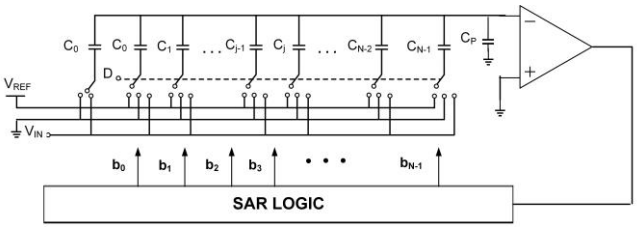


Fig. 1 A common charge-redistribution SAR ADC structure.

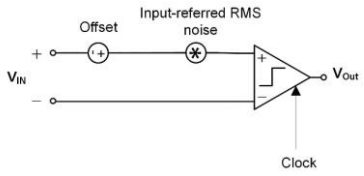


Fig. 2 Model for comparator and its input-referred noise and offset.

Also, reference [7] gives us a method to estimate the input-referred noise in fully dynamic regenerative comparators leveraging a reference architecture. We can conclude from these studies that any comparator has an intrinsic noise, but it is not the only noise existing in SAR ADC. As we know, any SAR ADC has two phases of operation; in the first phase, thermal noise due to capacitive array affects ADC's operation. In the second phase, again, the capacitive array's thermal noise exists but less than first phase. But the most significant noise for SAR ADC is comparator intrinsic noise, and it is roughly 10 times larger than thermal noise (voltage-based) [4].

As we can see in reference [2], assuming the noise of the comparator follows a normal distribution, then the input-referred noise and offset can be described by a random variable X_{COMP} with a normal distribution of mean μ (offset voltage) and standard deviation σ (input-referred noise voltage), as it can be seen in Eq. 1

$$X_{COMP} \sim N(\mu, \sigma^2). \tag{1}$$

B. Capacitive DAC Unwanted Factors

a. The first factor of capacitive DACs that we consider is capacitors mismatches. As studied in [5] and [6], capacitors mismatch in binary-weighted DACs can be assumed as a random value with a normal distribution. Its standard deviation is proportional to the area square root, and as in [5], matching can be achieved by equation 2

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{A_C}{\sqrt{WL}}. \tag{2}$$

Where A_C is a technology parameter, and also it depends on the capacitor type, which is used. W and L are representing geometric dimensions of the capacitor.

b. The second unwanted effect in DAC can be introduced as parasitic effects. As shown in Fig. 1, all of the array's parasitic capacitors are modelled in C_P. For a bottom-plate sampling structure of a SAR ADC (e.g., Fig.1), the parasitic capacitances on the bottom plate are driven by V_{REF} or GND, thus not affecting the conversion process because reference voltages are almost settled. The parasitic capacitances on the top plate, can attenuate the sampled input's amplitude, but won't change the polarity of the comparison result.

For a top-plate sampling structure of a SAR ADC, parasitic capacitances can change the comparison result's polarity. Still, this structure gives us a chance to have one more bit resolution by the first comparison. In recent studies, top-plate sampling has been a desired structure.

c. The third limiting effect in DAC is finite settling time in V_{DAC}, and it's resulted from the on-resistance of switches that causes an RC time constant. On-resistance of switches depends on switch dimensions, and it can be reduced by enlarging switches. As it has been modeled in [3], we can use a first-order circuit step response to explain this finite settling. It has been written in Eq. 3. This effect can be easily compensated using redundancy [8].

$$V_{DAC-st}(t) = V_{DAC}(1 - e^{-\frac{t}{\tau}}) \tag{3}$$

III. Proposed Calibration Method

In this section, we will present our calibration method for comparator offset and capacitive DAC mismatches. In particular, we assume an inherent random variation in capacitor sizes as a mismatch and a constant arbitrary value for comparator offset.

A. Comparator Offset Calibration

References [9] and [10] are our main ambitions, and we're going to make them better because of their FoM, which is better than other works. In [9], comparator inputs are grounded, and body bias changes by an 8-bit DAC until output toggles. But reference [10] has used 3 input pairs with different weights, including a pair with a heavier weighted left side, a pair with a heavier weighted right side, and in the last one both sizes are the same. Again, the input is grounded and input pair weights change using three 7-bit counter.

A problem associated with reference [9] is its slow convergence and large number of bits necessary for calibration. Reference [10] is fast but has other drawbacks, such as being foreground and not being able to track PVT changes; also, large number of gates. Therefore, we have decided to use a combinatorial method, which is both background and foreground. Fig. 3 shows our proposed comparator calibration. The function of weight balance logic is shown in Fig. 4, and body bias controller can be realized using a controller logic, which is connected to a capacitive ladder. Process variation simulation in prior works like Reference [10] shows that in the worst case, we have a comparator offset equal to a few decades of LSBs (e.g., around 70 LSBs), and our art is to remove the offset of the comparator before sampling.

First, weight balance logic starts calibrating by 4 LSBs step size; after that, we're sure that the comparator's input offset is less than 4 LSBs. Therefore, the body bias controller starts working with 0.5 LSB step size, and it only needs a 4-bit counter which can be achieved easily. Weight balance works foreground, and body bias calibration can work in background.

B. Capacitive DAC Mismatch Calibration

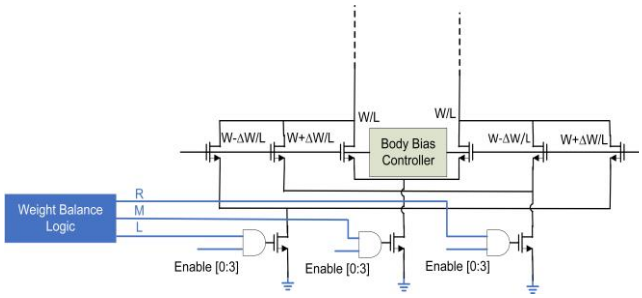


Fig. 3 Offset calibration scheme.

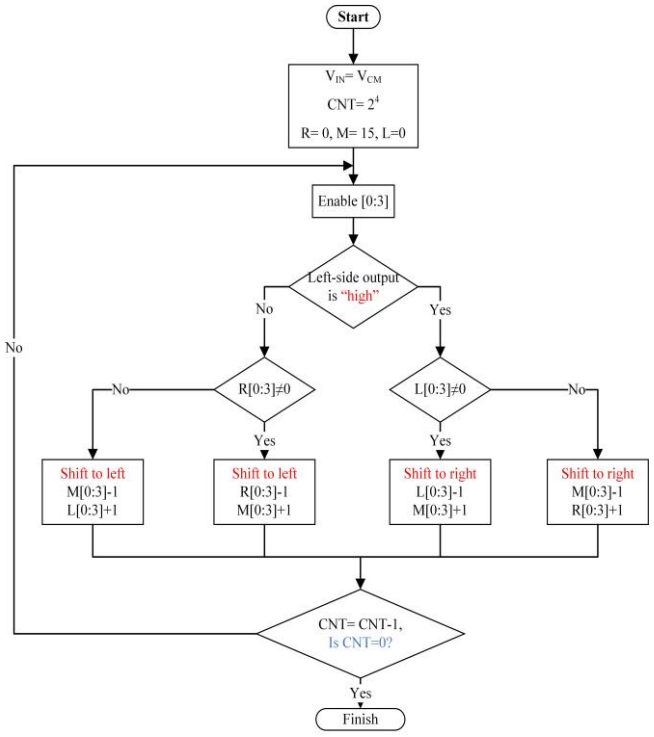


Fig. 4 Flew chart for weight balance calibration.

Like comparator offset calibration, DAC calibration is composed of foreground and background phases. In the foreground phase, a self-calibration is used, and the background phase, calibrates MSB capacitors using a correlation-based method. We will explain our method in the following parts. Note that complete structure is differential.

a. Self-Calibration: First, we must know that any imaginary differential structure has two capacitive arrays connected to the input terminals of the comparator. This approach is a foreground mismatch calibration method of SAR ADCs, and is based on DNL error estimation of individual capacitors using main DAC or an auxiliary DAC. Reference [11] is a classic sample for this method. As an example, we're going to calibrate the capacitor C_j and smaller capacitors are assumed to be ideal. Fig. 5 shows a block diagram of a self-calibration method which uses main DAC of the ADC for mismatch error estimation and consists of 3 following phases:

Phase I: The reset switch S is closed, and node X is grounded. Calibration logic will generate the following binary number:

$$D = \{d_{00}, d_0, d_1, \dots, d_{j-1}, d_j, \dots, d_{N-1}\} = \{1,1,1, \dots,1,0, \dots,0\} \quad (4)$$

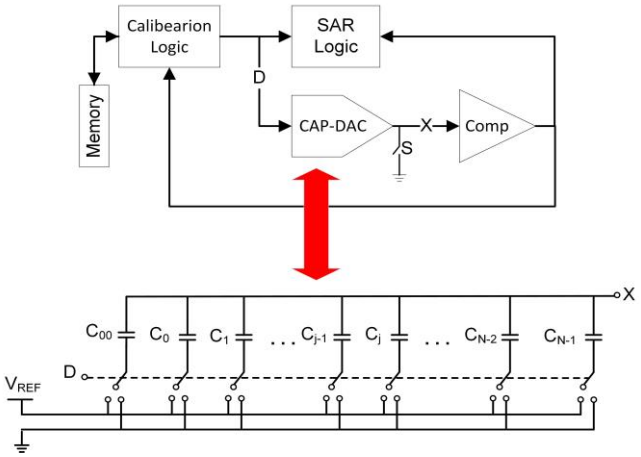


Fig. 5 Self- calibration scheme.

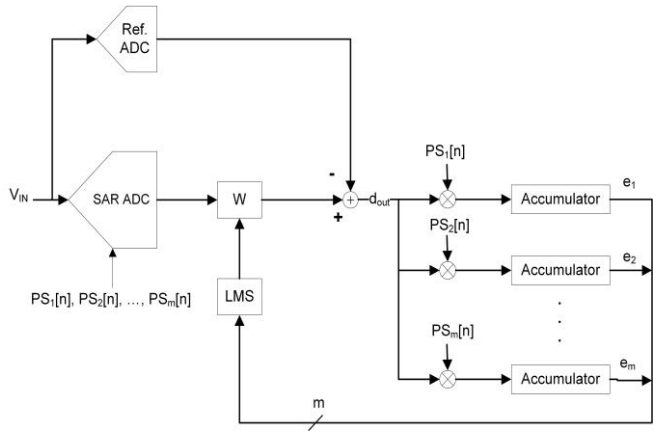


Fig. 6 IRD correlation-based calibration scheme.

Phase II: Switch S opens and D generates another binary number:

$$D = \{d_{00}, d_0, d_1, \dots, d_{j-1}, d_j, \dots, d_{N-1}\} = \{0,0,0, \dots,0,1, \dots,0\} \quad (5)$$

The charge on the node X changes to:

$$Q_X = V_{REF}.\left[C_j - \left(C_{00} + \sum_{i=0}^{j-1} C_i\right)\right] \quad (6)$$

Phase III: In this phase, the comparison is done, and the comparator's output determines the sign of mismatch of the capacitor C_j. The positive output is generated for $\Delta C>0$ and negative for $\Delta C<0$. When $\Delta C>0$, capacitors connected to the other terminal of the comparator will be connected to the V_{REF} in a successive algorithm by calibration logic until the output of the comparator changes; On the other hand, capacitors with smaller sizes in the same array with C_j start connecting to the V_{CM} until the sign of comparator's output changes when $\Delta C<0$. This value is the amount of the mismatch for the capacitor C_j and will be saved in memory.

If we imagine a zero-mean normal distribution for comparator's input-referred noise, a large number of comparisons and averaging must be done to overcome this

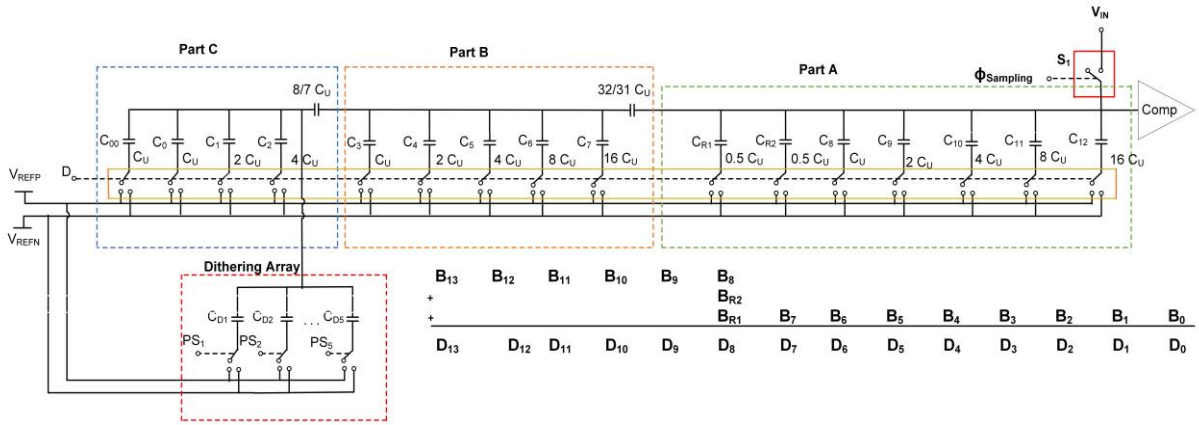


Fig. 7 Capacitive DAC for our proposed method.

effect. Recent arts show that comparators used in SAR ADCs can give us a standard deviation equal to a fraction of LSB; thus, we can be sure that large number of comparisons can significantly compensate for it.

These three phases are repeated for other capacitors under calibration. Still, there's a difference that next mismatch values give us summation of prior capacitors mismatches and mismatch of the capacitor under calibration. Therefore, we will need subtractors to achieve certain values for each capacitor in the array.

b. Correlation-based calibration: The main idea of this method is to inject a zero-mean pseudorandom bit sequence into the ADC and find out the correlation between output bits and injected sequence in order to extract the real bit-weights of the capacitive array. The main problem associated with these methods is their slow convergence. The Reference [12] injected a pseudorandom bit sequence (PRBS) into the summing node of the SAR ADC for mismatch error extraction and suffers from low-speed convergence. The Reference [13] has overcome low-speed convergence using an IRD correlation-based method and a reference ADC.

Fig. 6 illustrates the IRD correlation-based mismatch calibration using a reference ADC. The reference ADC removes the input signal before the bit-weight correlation takes place. In Reference [13], mismatch calibration is based on internal redundancy dithering, a method in which a pseudorandom bit sequence dithers the bit decision thresholds within the redundancy region. A capacitive array dithers bit decision threshold.

In our work, self-calibration is done first. In self-calibration mode, as shown in Fig. 7, the switch S_1, sampling switch, is opened. Capacitors of part C, and the first two capacitors of part B, C_3 and C_4, will calibrate the rest of the array using a self-calibration scheme. When self-calibration finishes, we will be sure that mismatches of the array are less than 1 LSB; note that we have assumed that part C capacitors and the first two capacitors of part B are ideal. Bridge-capacitors are also calibrated using parallel switched capacitors.

We have used IRD method with reference ADC, but our proposed correlation method has some strengths compared to Reference [13]. Self-calibration will result in a small number of bit-weight updates, and eventually, a faster convergence for the correlation-based method. 2 redundant bits, C_{R1} and C_{R2}, have helped us to tolerate dynamic comparator offsets and incomplete settlings less than $\pm V_{REF}/512$. Foreground calibration itself, brings us a reasonable resolution, and we can ignore background calibration for low-power applications. Eq. 7 and 8 give us error and bit-weight updated values:

$$e_i(j) = \sum_{n=jM}^{(j+1)M-1} PS_i(n).d_{out}(n) \quad (7)$$

$$W_{N-i}(j) = W_{N-i}(j-1) - \mu_i.e_i(j) \quad (8)$$

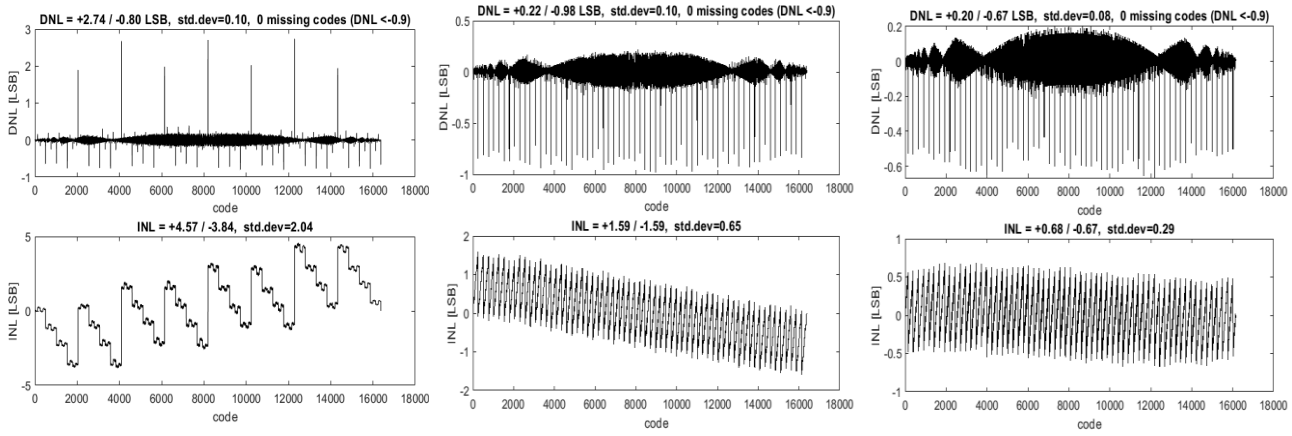
Where M is the correlation's estimator block size, PS is the pseudorandom bit sequence (-1 or +1), W represents the bit-weight of the capacitor under calibration, μ is the step-size of the LMS algorithm, and e represents the error of the iterations. Note that IRD method is only used for sub-binary structures, and our self-calibration provides such an array. We have used this correlation-based method for first 5 MSB bits.

IV. Simulation Results

Systematic simulation results of Fig. 7 structure for static and dynamic metrics, for a 14-bit, 1MS/s SAR ADC, without and with calibration are shown is Fig. 8 and 9, respectively. We have assumed a zero-mean normal distribution with standard deviation of 1% for capacitors mismatches and a constant arbitrary value of 10.25 LSBs for comparator offset. IRD calibration with a 6-bit reference ADC, is simulated for 10000 iterations. Bit-weight deviation from ideal bit-weight for MSB bit shown in Fig. 10 shows that after almost 5000 iterations, deviation will be small and suitable for expected result. Note that for systematic simulations, we have assumed unit cap equal to 1, so the MSB capacitor is equal to 16, and a deviation around 0.02, as shown in figure 10, can be ignored.

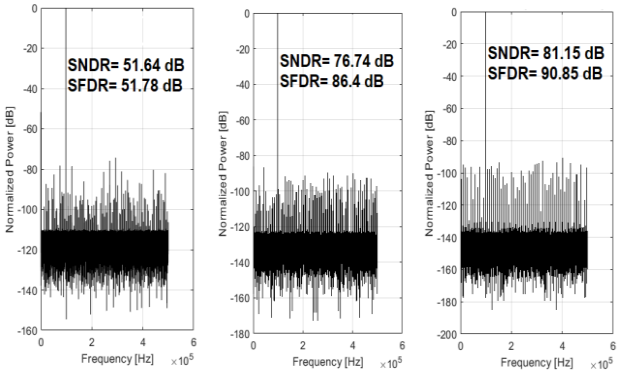
V. Conclusion

A SAR ADC calibration method is presented in this paper. Calibration process consists of two phases, foreground and background, and intends to reduce non-idealities of comparator and capacitive DAC. A Matlab code, simulates our method, and shows that proposed calibration method improves SNDR by 29.51 dB and SFDR by 39.07 dB.



(a) (b) (c)

Fig. 8 Simulation results for DNL and INL, (a) without calibration, (b) offset calibration and self-calibration, (c) offset calibration, self-calibration and correlation-based calibration.



(a) (b) (c)

Fig. 9 Normalized spectrum of output, (a) without calibration, (b) offset calibration and self-calibration, (c) offset calibration, self-calibration and correlation-based calibration.

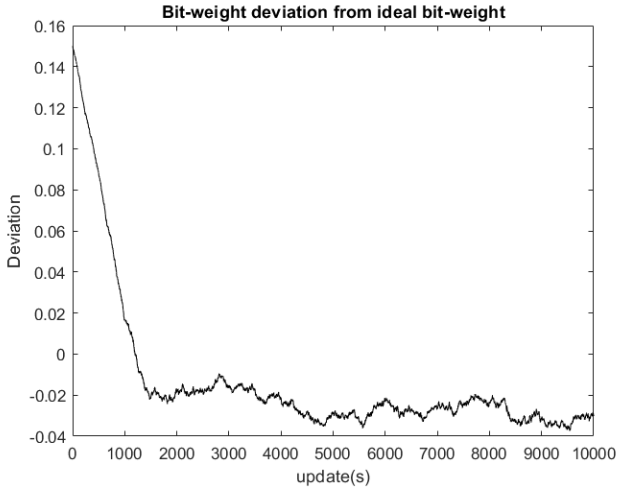


Fig. 10 MSB bit-weight deviation from ideal bit-weight.

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