A Digital Method for Offset Cancellation of Fully Dynamic Latched Comparators

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***Abstract*— In this paper, we have proposed a two-phase high precision digital offset cancellation method for dynamic latched comparators. The proposed method's first phase is weight balance control, and the second phase is named body bias control. The first phase reduces the offset of the comparator up to a few millivolts, and the second phase alleviates this amount to some decades of microvolts. The main reason for using the second phase is the weight balance calibration's sensitivity to the input pairs sizes and kickback noise. A retiming method is used to control the thermometer code DAC switching activities and minimize the glitches. The thermometer DAC structure is used for the body bias control method instead of R-2R DAC to ensure the body bias controller's monotonic signal. Circuitry simulations are done using Cadence with 180 nm standard CMOS technology under 1 V power supply. A strong-arm dynamic latched comparator is used for our calibration study. Before calibration, the input offset has three times of standard deviation equal to 19.56 millivolts. The weight balance control offset method has reduced this amount to almost 2.8 millivolts. Finally, the fully-calibrated comparator results have an offset equal to 363 microvolts. The calibration clock is set to be 33.3 MHz. Our offset cancellation prepares 53.9 times improvement in the input offset of the comparator using 389 microwatts.**

Keywords—offset cancellation, weight balance control, body bias control, thermometer code, retiming method.

I. INTRODUCTION

Comparators are the building blocks that transfer an analog value to a digital level, and this feature has made them an inseparable component of analog-to-digital converters (ADCs). Scaling the size of devices in advanced CMOS technologies will be contemporary with the power supply voltage reduction and will increase the speed of ADCs quickly. Here is the point that comparators limit ADCs function, and we have to concern about improvement in their role [1-2].

In most cases, voltage comparators, including the open-loop comparators, preamplifier-based latched comparators, and fully dynamic latched comparators, are the best choice for ADCs. Open-loop comparators don't have a clock-wised operation and work continuously with time and consume static power. Also, this structure has a limited gain-bandwidth product, and this causes a slow speed. Preamplifier-based latched comparators have improved open-loop comparator's speed using a latch stage. Also, they have low input offset, but their preamplifier consumes static power as in the previous structure. Fully dynamic latched comparators have overcome this issue. Their preamplifier only works in the comparison phase, and because of this, they only have dynamic power consumption. This fact has made the fully dynamic latched comparator structure the best choice for ADC applications [3-5].

Fully dynamic latched comparators use a positive feedback mechanism by one pair of cross-coupled inverters called latch to convert an input voltage to a full-scale digital level sharply. Nonetheless, this structure's accuracy is limited by the random offset voltage originating from the device mismatches, including threshold voltage V_{TH}, internal parasitic, external load capacitance mismatches, and current factor β ($=\mu C_{OX}W/L$). Therefore, the offset voltage is one of the main concerns in dynamic latched comparator design [6].

Offset cancellation techniques have been introduced that usually, we call them calibration in ADC works. Depending on the operation time, we can classify them into two groups, foreground and background. Background calibration is performed during normal ADC operation, but it requires at least one additional clock cycle for each ADC conversion. In the foreground calibration, the offset correction is performed during the ADC startup. Hence, it is relatively easier than background calibration to implement and is suitable for most ADC topologies [7-8]. The main fact that makes us need to use background offset calibration is their ability to follow PVT effects caused by environmental changes that are impossible to do by foreground methods.

Here we have categorized offset cancellation methods into 4 groups. The first three classes use impedance tuning, current tuning, and voltage tuning. The fourth group uses specific circuits to cancel the input offset. In literature, we can see [9] has used an impedance tuning in which a control logic controls the body bias of the input pair of the comparator using an impedance array. This will cause a level change in the comparator's output terminals, and step-size of the body bias changes make us sure about the accuracy of the offset cancellation method. References [7] and [10] have exploited current tuning methods; in [10], an extra input pair has been used, and two current sources charge and discharge the input capacitances of the extra pair, and a controller logic controls this current injection. This method is limited by the current injection step's accuracy and mismatches of the extra pair. Reference [7] has overcome this issue by controlling the tail current of exploited pairs. Offset cancellation is made using the main pair's current tuning employing two extra pairs. One of them has a heavier left transistor, and the other has a heavier right transistor. Three pairs current is controlled by some of the logic gates connected to their source pins and controlled by three counters and try having the same weights for the right and left sides. Digital implementation of current tuning has helped us achieve better performance. Voltage tuning methods also have the same scheme but different in implementation. Reference [11] exploits a voltage tuning method and offset canceled using an additional pair that its input voltage is controlled by tunable voltage signals controlled by up/down counters. The fourth group of offset cancellation methods use extra circuits; References [12] and [13] have used this method. In

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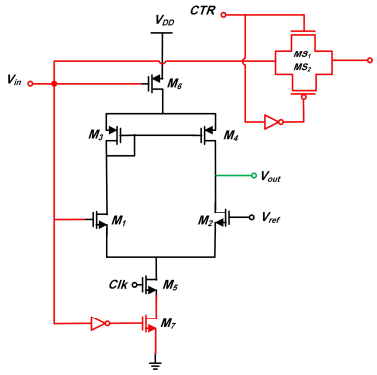


Fig.1. A preamplifier with bypass analog switch.

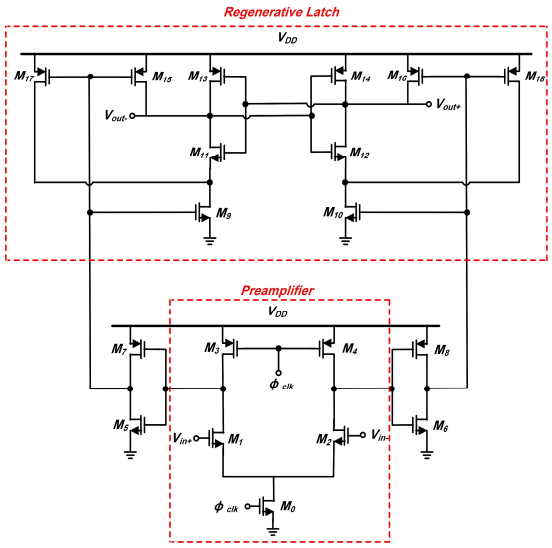


Fig.2. A two-stage fully dynamic latched comparator.

[12], we see a chopping circuit used for offset cancellation; this method is used for SAR ADC's comparator offset calibration and calculates the output bits twice with contrary terminals for a single sample in the foreground. The averaging operation for outputs reveals the offset. Reference [13] uses an estimator to adjust the offset of two comparators used for subrange SAR ADC structure.

The rest of the paper is organized as follows: In Sect. II, the analysis and models for fully dynamic latched comparators, are described. Sect. III presents our proposed method. In Sect. IV, the simulation results are provided. Sect. V concludes the paper, finally.

II. Comparator Architectures

Here we have classified dynamic latched comparators into two groups depending on their building blocks. A conventional dynamic latched comparator comprises three blocks, including a preamplifier, regenerative latch, and a buffer stage that can be a filter or a postamplification stage. Some techniques are developed to reduce the area and power dissipation of dynamic latched comparators, and according to them, we classify these structures into two or three-stage comparators.

A. Three-stage fully dynamic latched comparators

Considering comparator limitations, including chip area, power dissipation, input-referred noise and offset, kickback noise, input capacitance, and routing signal complexity, we must decide about the selected structure. A determinative block in three-stage comparators is the preamplification stage. The preamp is often used to diminish the comparator input offset voltage for more accurate matching and metastability effects, despite boosting total power dissipation.

Although dynamic preamp consumes less power than static gain-stages in preamp based latched comparators, it still is a bottleneck for power-limited applications. Therefore, new techniques have been developed to overcome this issue. Reference [14] has introduced a structure in which a bypass switch is addressed to ignore the preamp stage in a specific condition. Thus, two important design features are observed; first, the stated dynamic latch, and second application-dependent reconfigurability. The dynamic latch stage is designed so that the proposed modified circuit does preamplification and decision both. The reconfigurability is realized using an analog switch—also, a postamplifier stage is used to increase the slew rate. The preamp with bypass analog switch for this structure is shown in Fig. 1.

The aforementioned reconfigurable technique gives very high-speed conversion with low power consumption; therefore, it is suitable for Flash-type ADC applications. The power-hungry preamp stage is neglected for the higher input signal *(≥ Vth)*.

B. Two-stage fully dynamic latched comparators

Limited-power and limited-area applications tend to diminish power-hungry blocks. Preamplifier and buffer are chosen blocks for modifying the overall structure because of their flexibility. As an instance for two-stage comparators, we can mention reference [6], in which there's no third stage. As shown in Fig. 2, this structure is composed of a preamp connected to the regenerative latch through two inverters that isolate these two stages from each other.

There are two popular structures of dynamic latched comparators, named the strong-arm latch and the double-tail latch. The extensively applied latching comparator circuits were originally stated as part of a low-power digital circuits suite. For low-power ADC applications, like SAR ADCs, we prefer to neglect the power-hungry preamp; thus, we will discuss the aforementioned structures.

Fig. 3 shows a "double-tail" dynamic latched structure from [15]. The double-tail comparator keeps internal dynamic amplification benefits, usually using 4 MOSFETs as indicated in Fig.3 with M_1 to M_4. This stage helps it buffering the kickback noise during the regeneration phase, which is realized by two cross-coupled pairs. There's no isolation between the preamp and regeneration stages in this structure, but two MOSFETS, *M7* and *M8*, play a critical role in connecting the preamp's output to the static latch.

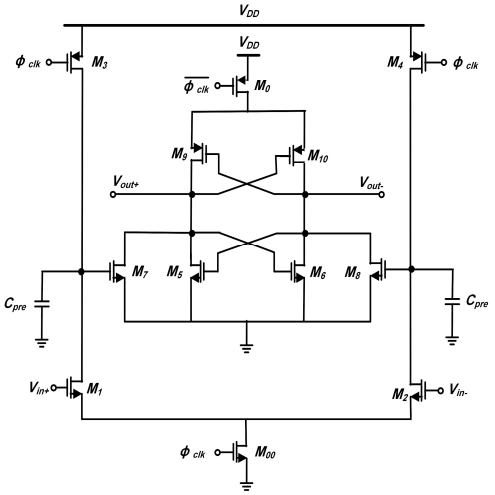


Fig.3. A double-tail dynamic latched comparator.

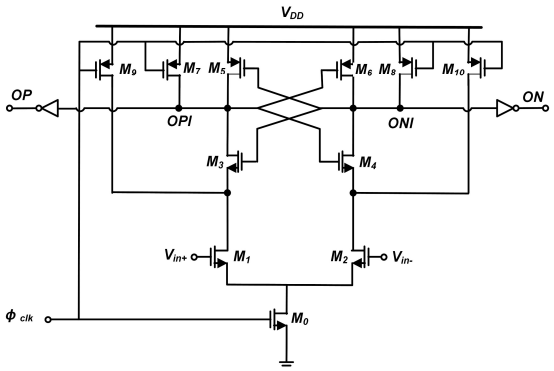


Fig.4. A strong-arm dynamic latched comparator.

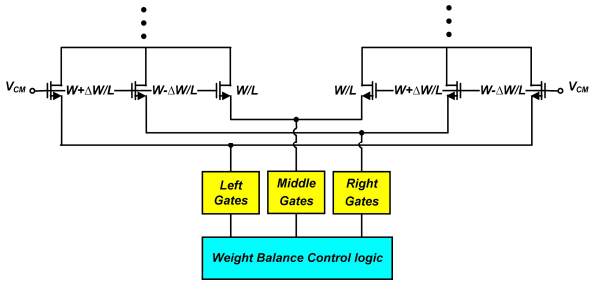


Fig.5. Block diagram of weight balance control method.

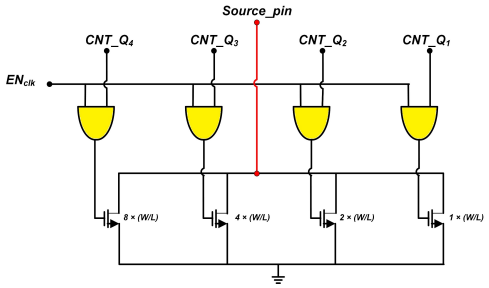


Fig.6. Gates Block.

Fig. 4 illustrates a structure called the "strong-arm" dynamic latched comparator used in [9]. The pre amplification stage is neglected in this structure and has made this structure the best choice for ultra-low-power applications like SAR ADC architectures. To further decrease the strong-arm dynamic latched comparator's offset voltage, analog or digital controlled offset voltage compensation techniques are suggested.

Reference [16] has prepared a comparison between the double-tail and strong-arm architectures in the same condition based on noise, offset, and speed. As a consequence of its smaller noise bandwidth, the strong-arm latch displays 15% lower input-referred noise than a double-tail comparator; Although the double-tail's input-referred noise is moderately higher, it will be supply-independent. The double-tail also gives a shorter regeneration time. As reported in [16], this shortens regeneration time by 20%. As the double-tail comparator decouples latency and regeneration, each can be separately optimized. Withdrawal from the double-tail structure, such as more integration stages in the dynamic amplifiers, worsens noise lightly. Although the strong-arm latch is the most compact regenerative comparator, it requires a well-controlled input common-mode voltage and a minimum supply voltage. This runs counter to the trend in scaled CMOS, and because of this, conventional technologies like 65nm (reference [9]) prefer using the strong-arm architecture. Still, newer technologies like 28nm (reference [17]) use the double-tail topology to overcome the mentioned issues. Usually, an offset cancellation method is used for strong-arm structures, and we will propose one in the next section.

III. Offset Cancellation Method

Our proposed offset cancellation is composed of two phases with long and small step accuracies. The first phase is called weight balance control calibration and uses long steps for offset cancellation, and the second one is the body bias control calibration method with small operation steps. We will explain our method in the following parts.

A. Weight balance control offset cancellation method

The weight balance offset cancellation method uses three input pairs instead of one with the same drain and gate pins and the difference in their source pin connections. We call these three pairs the middle, right, and left pair according to their weight, as the middle pair has two equal-sized transistors, the right pair uses a heavier transistor for its right side, and finally, the left pair owns a heavier left side. Fig. 5 depicts this method block diagram.

The drain-source current for an N-type MOSFET working in the subthreshold region can be determined by Eq.1

$$I_{DS} = KU_T^2 e^{1.8} \exp\left(\frac{V_{GS} - V_t}{nU_T}\right); \qquad K = \mu_n C_{ox} \frac{W}{L} \tag{1}$$

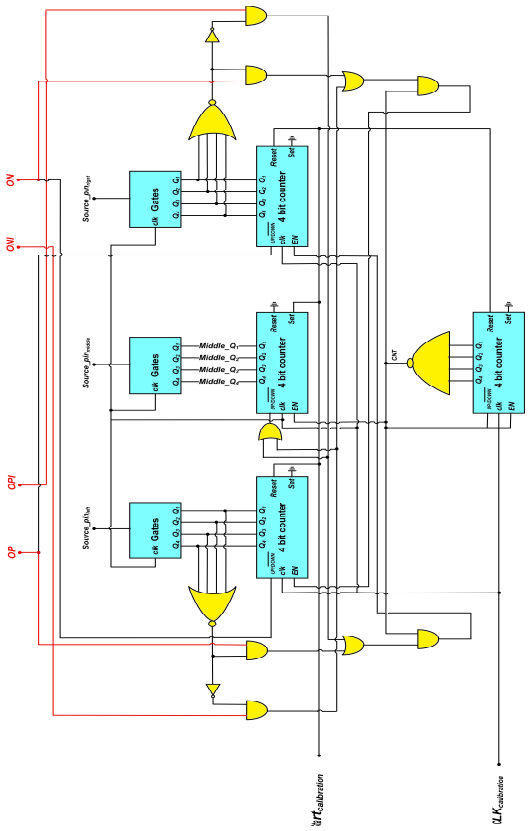


Fig.7. Weight balance logic implementation

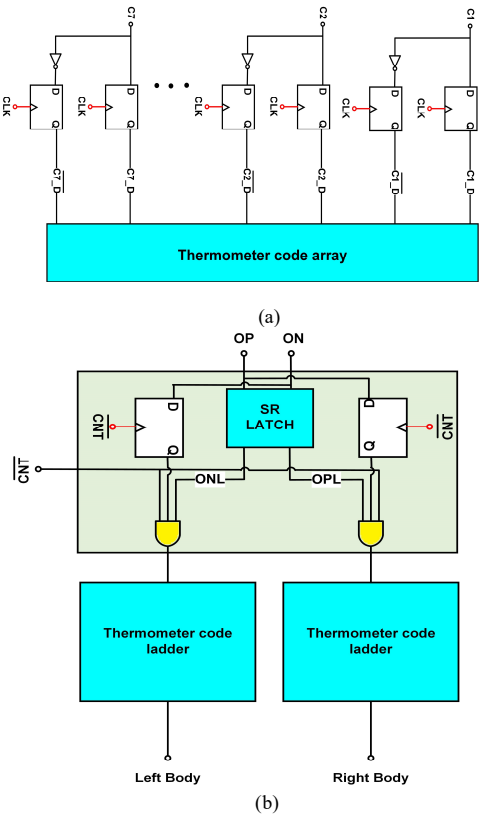


Fig.8. (a) retiming logic and (b) control logic for body bias control method .

Where U_T is the thermal voltage, V_{GS} shows the transistor's gate-source voltage, and V_t is the transistor's threshold voltage.

Also, μ_n is the electron's surface mobility, C_{OX} is the capacitance per unit area of the gate electrode, W and L show transistor size, summarized in K. For the comparator's input pair, if there were no mismatches in the circuit, the drain-source current of both transistors would be the same and equal to half of the tail current and consequently no offset. As determined in [7], the offset will correlate with some parameters of Eq. 1, and this correlation is shown in Eq. 2

$$V_{offset} = nU_T \ln\left(\frac{K_2}{K_1}\right) \qquad (2)$$

Therefore, three used pairs help us achieving a balanced right and left side.

As we depicted in Fig. 5, three pairs are connected to a control logic through some gates called gates block. The gates block structure is shown in Fig. 6. It shows 4 "and gates" connected to the gate pin of binary-weighted transistors (binary fingering is used) that are controlled by calibration clock and 4 other terminals powered by weight balance controller.

The circuit's operation is such that **first**, the input pairs are connected to the common-mode voltage; the 4 terminals connected to the middle pair's "gates block" are high, and the other pairs 4 terminals are low; a comparison is made and shows us which side has a heavier weight caused by the mismatch. **Second**, we start reducing the number of gates connected to the middle pair and increase the lighter side weight in a binary-weighted scheme. This process will continue until 16 comparisons are made, and the process is controlled by a control logic shown in Fig. 7. ON and OP are the outputs of the comparator, and ONI and OPI represent their inverse. This type of naming is used in the strong-arm dynamic latched comparator shown in Fig. 4.

The weight balance control offset cancellation using 4-bit-counters helps us decrease the offset to some millivolts. We ignore using more bits because of the method's sensitivity to the input pairs sizes and kickback noise. Thus, we exploit the second phase to improve the input offset voltage to some decades of microvolts.

B. Body bias control offset cancellation method

The second phase of offset cancellation exploits a precise method called body bias control. This method changes the body bias of input pairs in a successive algorithm. When the output toggles, offset cancellation is finished, so the control logic will have no changes anymore. During changing one side body bias, the counter side bulk is grounded.

Implementation blocks of the body bias control method are shown in Fig. 8. Due to the reference [20], we have again used a retiming method to minimize the glitches and maybe the switches' turn off effects, such as channel charge

injection or clock feedthrough. Also, a thermometer code ladder is used instead of R-2R DAC, and because of this, we will be sure about the monotonicity of the body bias voltage controller.

This method's most important bottleneck is its high power dissipation, but we will have no choice for high precision comparators. Fig. 8 illustrates the method's implementation block diagram.

IV. Simulation Results

Circuitry simulations are done using Cadence with 180 nm standard CMOS technology under 1 V power supply. The strong-arm dynamic latched comparator shown in Fig. 4 is used for our calibration study and designed in a way to have less than 246.8 microvolts input-referred noise. Fig. 9 shows the Monte-Carlo simulation for the comparator architecture, considering both mismatch and process variation parameters. As shown in Fig. 9, the output's transition level's threshold voltage will change due to the mentioned effects. Fig. 10 shows the data histogram and normal distribution with fitting plots. As shown in Fig. 10 a, an input offset has a mean equal to 222 microvolts and a standard deviation of 6.52 millivolts, so we have assumed the three times of standard deviation as the comparator's input offset, which is equal to 19.56 millivolts. The weight balance control offset method has reduced this amount to almost 933 microvolts and is assumed to be 2.8 millivolts for 99% assurance. Finally, Fig. 10 c shows the fully-calibrated comparator results, which has an offset equal to 363 microvolts. Power dissipation for different parts of the calibration is mentioned in table 1. As we mentioned before, the body bias control method has high power dissipation but high precision, and its power dissipation is dominants compared with other parts. The calibration clock is set to be 33.3 MHz. Our offset cancellation prepares 53.9 times improvement in the input offset of the comparator.

TABLE I. Power of the Circuit

Power Dissipation		
Without calibration	***Weight balance calibration***	***Body bias calibration***
2.27 µW	31.7 µW	355 µW

V. Conclusion

A two-phase high precision digital offset cancellation method for dynamic latched comparators is presented. This method exploits a scheme called weight balance control as its first phase and another method called body bias control as the second phase. The first phase reduces the offset of the comparator up to a few millivolts, and the second phase mitigates this amount to some decades of microvolts. We ignore using the weight balance calibration for more bits because of its sensitivity to the input pairs sizes and kickback noise. A retiming method is used to control turn on-turn off activities of the switches and minimizing the glitches. A thermometer ladder structure is used for the second phase instead of R-2R DAC to ensure the body bias controller's monotonic signal. Resistors are realized using poly devices. The calibration clock is set to be 33.3 MHz. Under 1 V supply, we have achieved 53.9 times better offset using 389 microwatts.

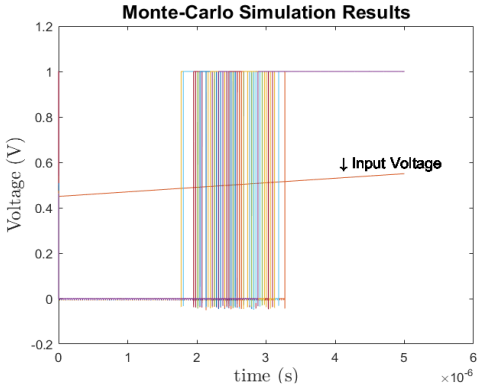
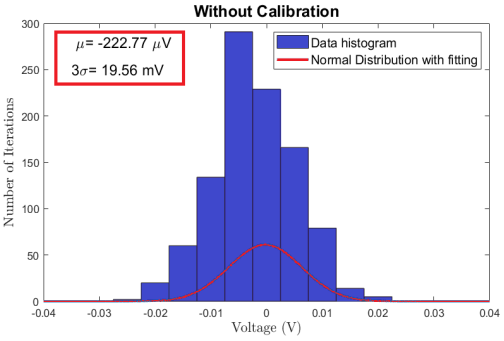
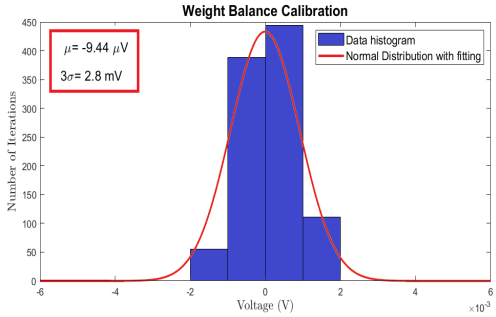


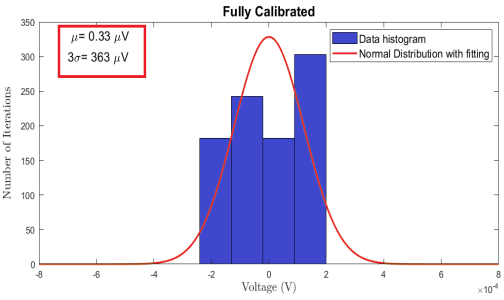
Fig.9. Output transition point variation due to mismatch and process.



(a)



(b)



(c)

Fig.10. Offset distribution (a) before offset cancellation, (b) only weight balance controller, (c) two offset cancellation phases added.

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