A New Architecture for Low-Power High-Speed Pipelined ADCs Using Double-Sampling and Opamp-Sharing Techniques

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***Abstract*— This paper presents a low-voltage low-power pipelined ADC with 1V supply voltage in a 90nm CMOS process. A new architecture is proposed to reduce the power consumption in high-speed pipelined analog-to-digital converters (ADCs). The presented architecture utilizes a combination of two current power-reduction techniques, double sampling and amplifier sharing. To decrease the power dissipation more efficiently, the stage scaling technique has been applied to the ADC and dynamic comparators have been used in sub-ADCs. Using this approach, a 10-bit 200MSample/s pipelined ADC has been designed in a 90nm CMOS technology. HSPICE simulation results show a signal-to-noise plus distortion ratio (SNDR) of 58.5dB with a 9.375MHz, 1-$V_{P-P,diff}$ input signal while consuming only 30.9mW power from a 1V supply voltage.**

I. INTRODUCTION

Nowadays, high-speed medium-resolution analog-to-digital converters (ADCs) are widely used in applications which require a combination of high-speed and low-power. However, the power dissipation of an ADC is remarkably raised as its sampling rate and resolution increase. An effective way to reduce the power consumption in high speed pipelined ADCs is the application of the double sampling concept which is especially common in multi-channel pipelined ADCs. This technique which is also known as I/Q amplifier sharing in time-interleaved pipeline based ADCs involves sharing an amplifier between I-channel and Q-channel ADCs. Another proper power reduction method is to share the amplifiers between two successive stages along a single pipeline ADC. Although each of these approaches can introduce some degradation in the performance of a single pipeline, they have been widely used because of their impressive effect on power consumption [1].

Considering the advantages and disadvantages of the mentioned techniques, double sampling and amplifier sharing along a single pipeline, a novel architecture using a combination of them is presented which takes advantages of them both and attenuates their drawbacks. To verify the efficiency of the proposed architecture, a 10-bit 200MSamples/s pipelined ADC is designed in a 90nm CMOS technology. To achieve low-power and high performance, the capacitor scaling, gain-boosted two-stage class A/AB and class A amplifiers, and dynamic comparators have also been employed. Simulation results in a 90nm CMOS process with 1V supply voltage show 58.5dB SNDR while consuming only 30.9mW power.

This paper is organized as follows. Section II describes the proposed architecture for low-power high-speed pipelined ADCs, and Sect. III presents a design example and the simulation results. The conclusions are given in Sect. IV.

II. THE PROPOSED ARCHITECHTURE

A. Comparison between Amplifier Sharing and Double Sampling

In the conventional opamp sharing technique an opamp is shared between two adjacent stages. As shown in Fig. 1(a), in ϕ_1 when the first stage is in the sampling mode, the amplifier is used in the second stage which is in the multiplying digital-to-analog converter (MDAC) mode. Then in ϕ_2, the second stage samples its input and the first stage uses the amplifier. In this way, the number of amplifiers is halved compared to the basic pipelined ADC. However, the total power dissipation is only reduced by one third, because the capacitor scaling cannot be efficiently applied to the ADC [2].

In the basic pipeline ADC, the optimum sampling capacitor for each stage is determined by noise budgeting, which leads each stage to have a relatively smaller sampling capacitor in comparison with its previous stage, without significant degradation in the total signal-to-noise ratio (SNR). As a result, the current consumed in the amplifier of the second stage can be considerably decreased compared to that of the first one, since power of the amplifier is scaled down

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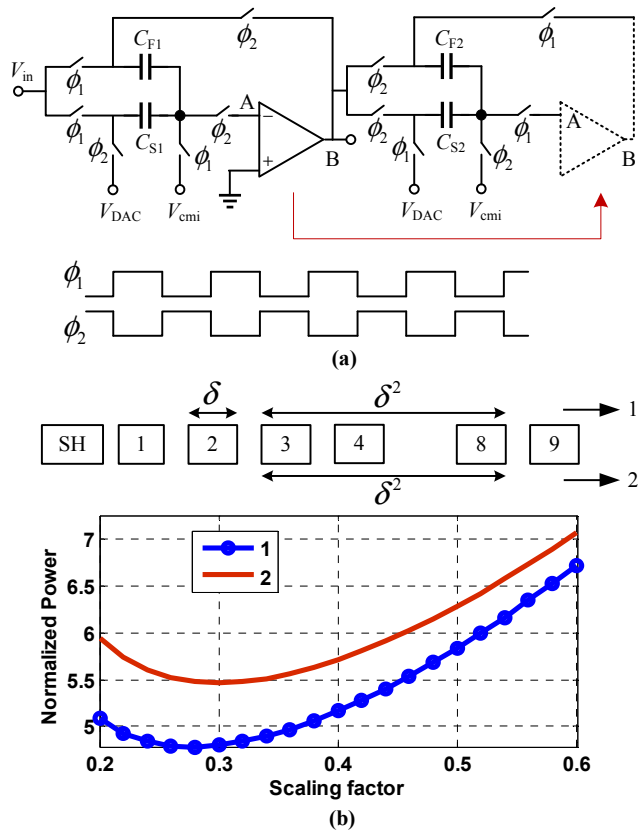

Figure 1: (a) Two consecutive gain stages using the conventional amplifier sharing technique, (b) two configurations of a 9-stage 1.5-bit per stage pipelined ADC and their power consumption versus the scaling factor.

according to the sampling capacitor. Therefore, when an amplifier is shared between the first and the second stages, the capacitor scaling cannot be effectively used along the ADC [2]. To more clearly show how this problem affects the power consumption of a pipelined ADC, a model based on what introduced in [3] has been used to plot the normalized total power consumption (P) versus scaling factor (δ) in two configurations of a 9-stage 1.5-bit per stage pipelined ADC. As illustrated in Fig. 1(b), stage 2 and stages 3 to 8 of the first configuration are scaled compared to stage 1 with scaling factors δ and δ^2, respectively. But in the second configuration the amplifiers of stage 2 and stage 1 are the same and only stages 3 to 8 are scaled to stage 1 with scaling factor δ^2. Figure 1(b) shows the results in which the curves named 1 and 2 belong to the first and second configurations, respectively. The results obviously show that the total power dissipation of a 1.5bit/stage pipelined ADC remarkably increases when the second stage is not scaled down compared to the first one. Therefore, this is a considerable drawback of the amplifier sharing, since it is regarded as a power reduction technique.

As it is shown in Fig. 2, each gain stage using the double sampling technique has its own opamp. But, there are two sets of capacitors in each stage, C_{S1}-C_{F1} and C_{S2}-C_{F2}, each of which samples the input signal at $f_s/2$, while the sampling frequency of the whole ADC is f_s [4]. In this way, the amplifier operates in both phases. Therefore, not only the double sampling technique reduces the power consumption of the amplifier due to its reduced unity-gain-bandwidth, but also makes it possible

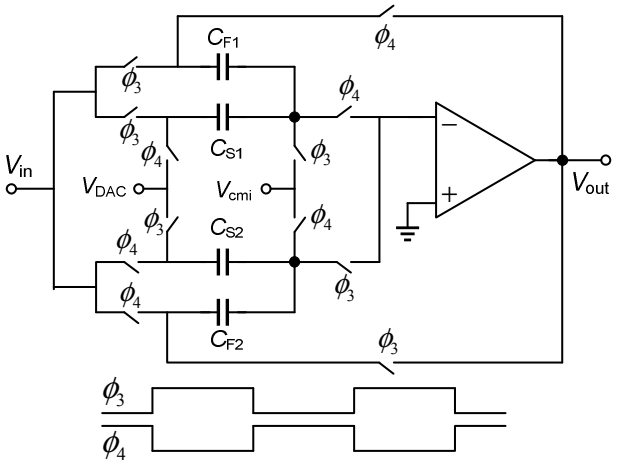

Figure 2: A gain stage using the double sampling technique.

to use the optimum amplifier in each stage. But, this technique doubles the number of capacitors and switches in each stage.

B. The Proposed Architecture; A combination of Two Techniques

The proposed architecture for a 10-bit pipeline ADC with 1.5-bit per stage is presented in Fig. 3. The front-end sample-and-hold (SH) and the first two stages use the double sampling (DS) technique. In this way, each of the stages has its optimum amplifier; the power of which is approximately halved in comparison with that in the basic pipeline ADC. In addition, the SH amplifier has a lower power compared to that of a pipeline ADC using the conventional opamp sharing in which the amplifier of the SH cannot be shared.

In the last stages of pipelined ADCs, the size of the optimum sampling capacitors which is based on noise and matching characteristics do not usually differ for two successive stages. For example, in the prototype designed ADC the optimum unit capacitor for stage 3 is equal to that of stage 4, and the same is true for the next stages of the pipeline. Therefore, an amplifier can be shared between these two consecutive stages optimally. This fact leads the double sampling technique not to be preferable for these last stages. Moreover, it adds too much switches and capacitors to the ADC which makes it inefficient from chip area point of view.

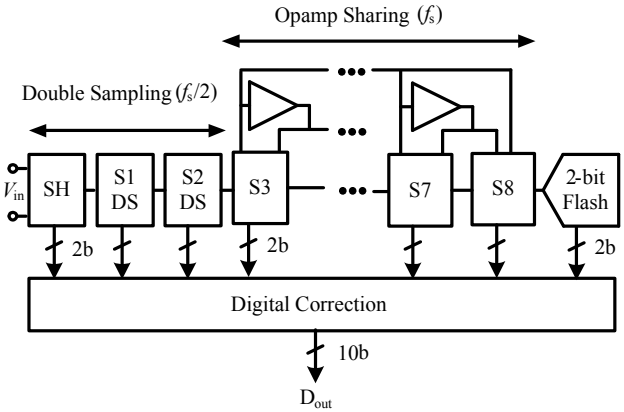

Figure 3: The proposed architecture.

Thus, the amplifiers in the last stages of the proposed architecture are shared between two successive stages instead of being double sampled. In this way, the number of opamps, and therefore the area devoted to them, is also reduced compared to that of a pipelined ADC where all of the stages are using the double sampling technique.

Figure 4 presents the switched capacitor architecture of the third stage which matches the double sampling stages (stage 1 and stage 2) with the next stages. The two sets of capacitors, C_{S13}-C_{F13} and C_{S23}-C_{F23}, sample the input signal to stage 3 in ϕ_1 and ϕ_2, respectively. But, these capacitors are connected to the amplifier in only half of the next clock phase (ϕ_2 or ϕ_1), which is ϕ_{23} and ϕ_{13}. This means that the amplifier of stage 3 works in ϕ_3 and it can be used for stage 4 in ϕ_4. In this way, this opamp is shared between stage 3 and stage 4 in ϕ_3 and ϕ_4, while the input signal to stage 3 is sampled in ϕ_1 and ϕ_2. In other words, the holding time for outputting the signals from stage 2 to stage 3 is the same as a conventional stage using the double sampling technique, while the amplifiers of stages 3 to 8 are shared between two adjacent stages and are twice as fast as the double sampling stages (stage 1 and 2).

Since the architecture uses both opamp sharing and double sampling techniques to reduce the power consumption, the capacitor scaling can be applied to it in the most effective way, as apposed to the conventional amplifier sharing along a single pipeline. In addition, it does not use more capacitors and switches in order to reduce the power, which results this ADC to be efficient from the die area and design viewpoints, too.

III. Design Example and Simulation Results

To verify the effectiveness of the proposed architecture, a 10-bit 200MSample/s pipelined ADC has been designed. The 1.5-bit per stage resolution has been chosen for this ADC, because it has been proven to be efficient for high speed and low power pipelined ADCs.

The SH, operating in ϕ_1 and ϕ_2, uses the timing skew insensitive double sampled architecture [4]. The MDACs of the first two stages also employ the double sampling technique and have the architecture shown in [4]. In stages 3 to 8, the amplifiers are shared between two successive stages in ϕ_3 and ϕ_4. Using this architecture, all of the stages of the designed ADC have their optimum unit capacitor based on noise budgeting calculations and mismatch requirements of a 10-bit pipeline ADC. The first configuration of Fig. 1(b) has been applied to the ADC to implement the capacitor scaling technique, while this configuration cannot be applied if the amplifiers of adjacent stages are shared along the whole ADC. In addition, all of the amplifiers are active in both phases to reduce the total power consumption.

A low-voltage and low-power two-stage class A/AB amplifier based on an OTA introduced in [5] is used for the SH. This amplifier combines a folded cascode as the first stage, active current mirrors as the second stage and the hybrid cascode compensation technique to achieve fast settling and low power consumption [10]. Since this opamp is active in both phases, there is a potential problem of introducing a correlation between consecutive samples. Due to the finite gain of the opamp, a charge is injected in the input parasitic capacitance which never resets. Therefore, the output voltage will be a recursive function of the present and the previous samples [6]. To overcome this "memory effect" in a 10-bit pipeline ADC, the gain-boosting technique is applied to the first stage of the amplifier to achieve a gain higher than $2\times(2^{10+1})$. The boosting amplifiers are two fully-differential folded cascode opamps which have a p-type or n-type input differential pair for nMOS and pMOS cascode transistors of the main amplifier to allow a flexible input common-mode range.

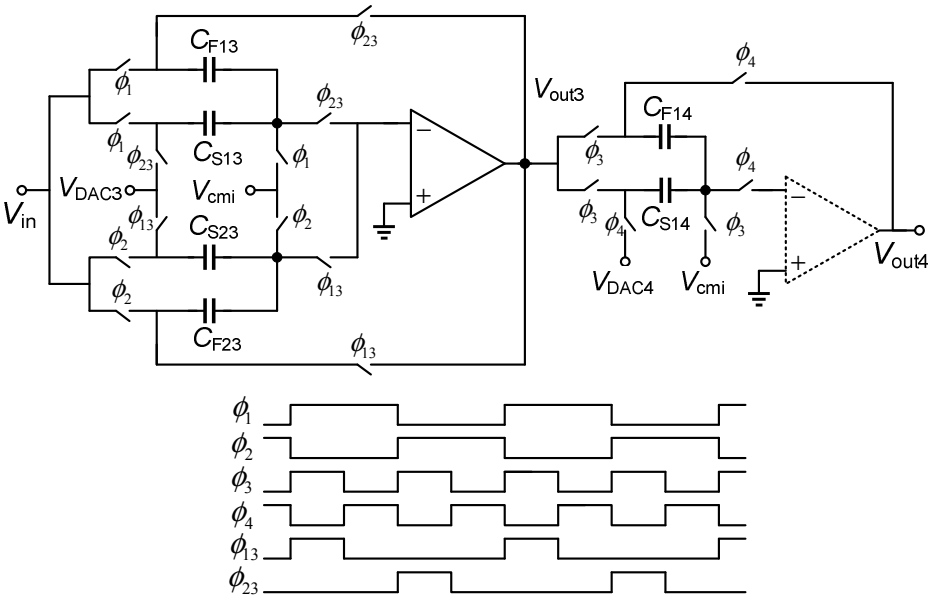

Figure 4: The proposed architecture for the third and fourth stages.

In the first two stages of the pipeline, the amplifiers have the same structure as the S/H amplifier. The amplifiers of the next stages also have the same structure as that of SH circuit except that they do not use the class AB technique in their second stage, since their capacitance load is relatively smaller and it would not be efficient to use the class AB approach. Moreover, depending on the gain requirements of the stages, only one gain-boosting opamp has been applied to pMOS cascode transistors of stage 3, and the other stages have not used the gain-boosting technique.

The input sampling and feedback switches are implemented in a reliable bootstrapped configuration to minimize the nonlinearity introduced by signal dependant on-resistance, based on linearity requirement of a 10-bit ADC. In addition, some switches connecting to $V_{DD}/2$ needed to use this configuration to provide properly low on-resistance.

In the 1.5-bit per stage pipeline architecture, there is one redundant quantization level in each sub-ADC which with the digital correction allows $\pm V_{Ref}/4$ offset in the comparator decision levels, where V_{Ref} is the single-ended reference voltage. Therefore, a simple dynamic comparator consuming no static power and a conventional switched-capacitor scheme as a capacitive dynamic divider sampling the input signal and the references have been used in the prototype ADC to achieve very low power consumption.

The proposed ADC is simulated with HSPICE models of a 90nm CMOS process with MIM capacitors. The full-scale input signal is $1V_{p\text{-}p,diff}$ and the supply voltage is 1V. Simulation results show that the power consumption of the 10-bit 200MS/s ADC is 30.9mW and SNDR is 58.5dB and 56.8dB at 9.375MHz and 93.75MHz input signal frequencies, respectively. The output FFT plot for f_{in} = 9.375MHz is shown in Fig. 5. The performance of the ADC has been checked in the different process corner cases under temperature variations spanning from -40°C to 85°C, and the worst case results (SS@85°C and FF@-40°C) are summarized in Table I, in comparison with some recently reported pipelined ADCs. The comparison is based on a figure of merit defined as:

$$FOM = \frac{P}{2^{ENOB} \times f_s} \qquad (1)$$

The proposed ADC shows the lowest figure of merit, though its reported performance has been obtained by simulation. This comparison shows that the proposed architecture is an efficient way to decrease power consumption in pipelined ADCs without any degradation in the ADC function or remarkable increase in its chip area.

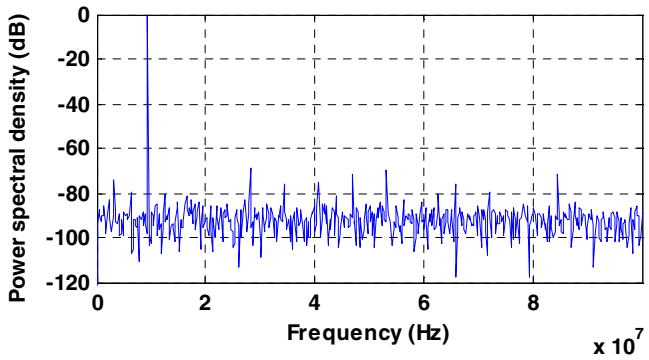

Figure 5: The FFT plot of the designed ADC at f_{in} = 9.375MHz.

TABLE I. COMPARISON WITH SOME REPORTED ADCS.

Ref.	Tech (nm)	V_{DD} (V)	f_s (MSPS)	Power (mW)	SNDR (dB)	FOM (pJ/step)
[1]	90	1.2	200	55	54.4	0.64
[7]	90	2.5	40	25	56.5	1.18
[8]	90	0.5	10	2.4	48.1	1.15
[9]	65	1.2	800	30	44.2	0.28
This work (TT@27)	90	1	200	30.9	58.5	0.22
This work (SS@85)				27.8	55.9	0.28
This work (FF@-40)				33.8	56.5	0.31

IV. CONCLUSIONS

A new architecture combining two existent methods was proposed to reduce the power consumption in pipeline ADCs more efficiently. Since this Architecture takes the advantages of both amplifier-sharing and double-sampling techniques, the capacitor scaling is efficiently applied along it, and the power consumption of the SH amplifier is approximately halved compared to the conventional amplifier sharing. In addition, the ADC does not suffer from too much capacitances and switches which are added to ADCs using the double sampling technique. Employing the proposed architecture, a 10-bit 200MSamples/s pipelined ADC is designed in a 90nm CMOS technology. To achieve low-power and high performance in this ADC, the capacitor scaling, gain-boosted two-stage class A/AB and class A amplifiers, and dynamic comparators have also been used. The simulation results in a 90nm CMOS process with 1V supply voltage show 58.5dB SNDR while consuming only 30.9mW power that confirms the effectiveness of the applied techniques in reducing the power consumption while maintaining the desired performance.

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