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A Wideband Low-Noise Inductorless CMOS Active Mixer With Improved Linearity

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***Abstract*—This paper presents a CMOS active inductorless downconversion mixer for zero-IF receivers. The structure implements the IM2 injection and derivative superposition techniques to improve the linearity. Nonlinear currents are generated by auxiliary transistors and they are injected to the nonlinear currents of the input transistors into increase the second-order input intercept point (IIP2) and third-order input intercept point (IIP3) values of the mixer. Common-Gate structure is used in the RF input stage. To reduce the noise contribution of the input transistors, a noise cancellation technique is employed. The proposed mixer is designed in 65 nm CMOS technology and simulated using Spectre-RF in Cadence. The simulation results show 8.34 dB, 6.81 dB, and 4.15 dB on average improvement for IIP2, IIP3, and NF, respectively, in the 0.8-5 GHz input frequency range. The proposed mixer consumes 13.95 mW power which is 64.1% more than the conventional CMOS active mixer.**

Keywords—CMOS active mixers, wideband, linearity improvement, noise cancellation, zero-IF receivers.

I. Introduction

Mixers are widely used in radio frequency receivers and transmitters to down and/or up convert the frequency of the input signal. Mixer's performance affects the whole receiver or transmitter's performance and can degrade the total linearity and noise. In low-power systems, it is crucial to have a high linear and low noise mixer. Therefore, linearity improvement and noise reduction of CMOS active mixers have recently been the topic of current research activities.

Several linearization techniques have been recently presented for narrowband and wideband CMOS active mixers [1-13]. In [1], a high linearity mixer for narrowband applications is proposed by using an enhanced derivative superposition method. In this mixer, an auxiliary transconductor biased in moderate inversion region along with a source degeneration inductor are utilized to enhance the linearity and reduce the noise figure (NF). In [2], the IIP3 of the proposed mixer is improved by implementing two techniques. First, by optimally biasing the inductively source degenerated (ISD) transconductor, its second-order derivative transconductance is reduced. Second, by injecting second-order intermodulation (IM2) terms to the bulk of the ISD, the IIP3 is improved. A feedforward linearization technique is presented in [3] to enhance the third-order input intercept point (IIP3). In this approach, the second-order intermodulation terms are generated and multiplied with the mixer's output to improve the IIP3. In [4], in order to improve the IIP3, a second-order derivative transconductance is generated by transistors that are biased in weak inversion region. Moreover, the conversion gain and NF are improved by using auxiliary transistors. This mixer has been designed for wideband applications. [13] represents two techniques for improving the IIP2 and conversion gain. The IIP2 is increased by implementing an IM2 current generator circuit. The generated current is injected to the drain of the input transistors, and hence, the output IM2 current of the transconductance stage is removed. Moreover, by realization of a negative capacitance, the parasitic capacitances at the drain of the input transistors are cancelled and the conversion gain is increased.

This paper presents an inductorless and high linear CMOS active mixer for wideband zero-IF receivers. Using auxiliary transistors, the first and second-order derivative transconductances are generated and injected to the nonlinear currents of the input transistors. Hence the IIP2 and IIP3 values are improved. In addition, the noise of the input transistors is canceled by using two transistors that are in parallel with the input transistors.

The rest of the paper is organized as follows. Section II explains the structure of the proposed mixer in details. Section III illustrates the simulation results, and Section IV concludes the paper.

II. Structure of the Proposed Mixer

Fig. 1 shows the schematic of the proposed inductorless wideband CMOS active mixer. The transconductance stage consists of M_1-M_{16} transistors and R_1-R_5 resistors. M_{17}-M_{20} transistors form the switching stage, and the IF stage includes R_L and C_L. The common-gate structure is utilized for input M_1-M_4 RF transistors since it results in better linearity compared to the common-source structure. M_3 and M_4 transistors are also used to provide input matching with less DC power consumption. Gate terminals of the input transistors are connected to the source of the counterpart transistors so that we can have more conversion gain and satisfy the linearity conditions easier as will be discussed in the next section. M_5 and M_6 transistors improve the noise figure, and M_7-M_{16} transistors enhance the linearity of the proposed mixer. Moreover, to have a robust behavior against process, voltage, and temperature (PVT) variations, a constant-g_m bias circuit has been utilized as shown in Fig. 2 where several MOS decoupling capacitors are employed to cancel out the thermal noise of the biasing transistors. The biasing transistors in Fig. 2 are sized to maintain M_7-M_{10} transistors in the weak inversion region and other transistors in the saturation region. In Fig. 2, M_1-M_4 and off-chip R_1 resistor are the core of the biasing circuitry. M_{s1}-M_{s3} transistors form the start-up circuit, which is off during the normal function of the biasing circuitry. For the mixer's transistors that their source terminal is not connected to ground, the exact condition is met in the biasing circuitry.

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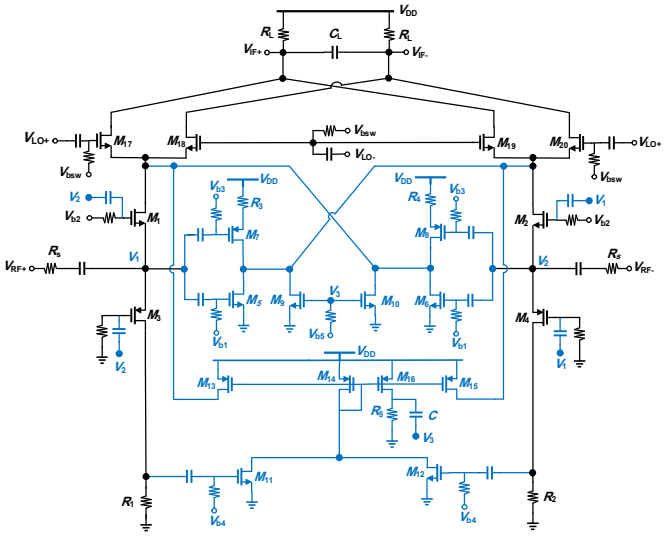

Fig. 1. The proposed CMOS active double-balanced mixer.

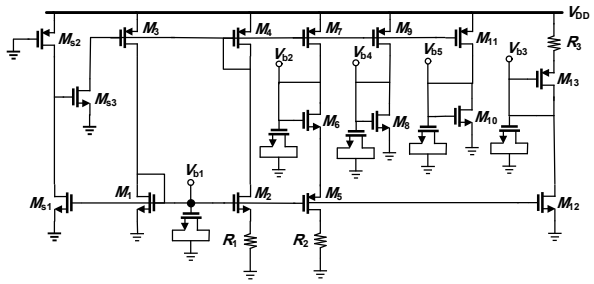

Fig. 2. Constant-g_m bias circuit.

A. Input Impedance Matching

To provide a good input impedance matching over the desired input frequency range, the following condition should be satisfied:

$$R_s = \frac{1}{2\left(g_{m1}+g_{m3}\right)} = 50\,\Omega \;\Rightarrow\; g_{m1}+g_{m3} = 10\,mA/V \tag{1}$$

Where R_s is the source resistance. By using M_3 transistor, the required g_{m1} is reduced, and hence, lower bias current is needed to satisfy the input impedance condition.

B. Linearity Analysis

IM2 injection and derivative superposition techniques have been used to improve the linearity of the conventional mixer. By using auxiliary transistors, nonlinear currents have been generated and they are injected into the current of the input transistors. The switching transistors steer the resulted current to the load resistors and create the linear IF output voltage. Using the Taylor series expansion, the current of the switching stage is expressed as follows:

$$i_{sw+} = i_{ds1} + i_{ds6} + i_{ds8} + i_{ds10} + i_{ds13} \tag{2}$$

According to (2), the switching stage current, i_{sw+}, consists of five currents, which we calculate in the following. These currents contain nonlinear terms that help improving the linearity. The drain current of M_1, M_6, and M_8 can be easily calculated as:

$$i_{ds1} = -2g_{m1}v_1 + 4g'_{m1}v_1^2 - 8g''_{m1}v_1^3 + \ldots \tag{3}$$

$$i_{ds6} = -g_{m5}v_1 + g'_{m5}v_1^2 - g''_{m5}v_1^3 + \ldots \tag{4}$$

$$i_{ds8} = -\alpha g_{m8}v_1 + \alpha^2 g'_{m8}v_1^2 - \alpha^3 g''_{m8}v_1^3 + \ldots \tag{5}$$

Where $\alpha = 1/(1+g_{m8}R_4)$. For the drain currents of M_{10} and M_{13}, we first calculate the voltage over R_1 as:

$$v_{R1} = i_{ds3}R_1 = R_1\left[2g_{m3}v_1 + 4g'_{m3}v_1^2 + 8g''_{m3}v_1^3 + \ldots\right] \tag{6}$$

M_{11} and M_{12} transistor form an IM2 generator circuit. Their drain terminals are connected together, and the structure is differential. Therefore, no odd harmonics are presented at the drain current of M_{14}, and it contains only even-order harmonics of nonlinearities as:

$$i_{ds14} = 2g'_{m11}v_{R1}^2 + \ldots \tag{7}$$

Then, M_{13} and M_{16} transistors mirror the generated current by a factor of $n = (W/L)_{13}/(W/L)_{14}$ and inject it to the input transistors' drain current as:

$$i_{ds13} = 2n \times g'_{m11}R_1^2\left[4g_{m3}^2v_1^2 + 16g_{m3}g'_{m3}v_1^3 + \ldots\right] \tag{8}$$

As illustrated in (8), the generated current contains second-order and higher order nonlinearities. To calculate the drain current of M_{10}, we need to obtain the voltage of node V_3, which is calculated as:

$$v_3 = 2m \times R_1^2R_5 \times g'_{m11}\left[4g_{m3}^2v_1^2 + 16g_{m3}g'_{m3}v_1^3 + \ldots\right] \tag{9}$$

where $m = (W/L)_{16}/(W/L)_{14}$. Now, M_{10} transistor converts this voltage to the current as:

$$i_{ds10} = 2m \times R_1^2R_5 \times g_{m10}g'_{m11} \times\left[4g_{m3}^2v_1^2 + 16g_{m3}g'_{m3}v_1^3 + \ldots\right] + \ldots \tag{10}$$

Finally, the current of the switching stage is obtained as:

$$
\begin{aligned}
i_{sw+} = &-\left[2g_{m1}+g_{m5}+\alpha g_{m7}\right]v_1 \\
&+\left[4g'_{m1}+g'_{m5}+\alpha^2 g'_{m7}-8nR_1^2 g_{m3}^2 g'_{m11}\right. \\
&\left.+8mR_1^2 R_5 g_{m3}^2 g_{m10} g'_{m11}\right] v_1^2 \\
&-\left[8g''_{m1}+g''_{m5}+\alpha^3 g''_{m7}+32nR_1^2 g_{m3} g'^2_{m3} g'_{m11}\right. \\
&\left.-32mR_1^2 R_5 g_{m3} g_{m10} g'_{m11}\right] v_1^3
\end{aligned} \tag{11}
$$

In relation (11), the first term is the effective transconductance of the RF input stage. This term affects the conversion gain of the mixer. We expect a higher level of conversion gain from the proposed mixer compared to the conventional mixer as the effective transconductance is increased. The second term in (11) causes the second-order nonlinearity, which degrades the IIP2 of the mixer. In order to increase the IIP2 of the mixer, the following condition should be satisfied:

$$
\begin{aligned}
&4g'_{m1}+g'_{m5}+\alpha^2 g'_{m7}-8nR_1^2 g_{m3}^2 g'_{m11} \\
&+8mR_1^2 R_5 g_{m3}^2 g_{m10} g'_{m11}=0
\end{aligned} \tag{12}
$$

All transistors are biased in the saturation region, except for M_7-M_{10} transistors that are biased in the weak inversion region. This makes the first, second and last term in (12) to be positive, and the third and the fourth terms to be negative. Therefore, by properly sizing the transistors and resistors, these terms cancel out each other. The third term in (11) causes the third-order nonlinearity, which degrades the IIP3 of the mixer. In order to increase the IIP3 of the mixer, the following condition should be fulfilled:

$$
\begin{aligned}
&8g''_{m1}+g''_{m5}+\alpha^3 g''_{m7}+32nR_1^2 g_{m3} g'^2_{m3} g'_{m11} \\
&-32mR_1^2 R_5 g_{m3} g_{m10} g'_{m11}=0
\end{aligned} \tag{13}
$$

As explained before, the transistors are biased in different regions. Therefore, in relation (13), the first, second, and last terms are negative, and the third and fourth terms are positive. Consequently, by properly sizing the transistors and resistors, these terms can cancel out each other. According to the simulation results, which are presented later, the proposed mixer has an average of 8.34 dB and 6.81 dB improvement in IIP2 and IIP3, respectively, compared to the conventional mixer in the RF input bandwidth. The conventional mixer is the Fig. 1 mixer without the added blue components, R_1, and R_2. Also, M_3 and M_4 are realized by NMOS transistors.

C. Conversion Gain

As discussed in the previous sub-section, the conversion gain of the proposed mixer is improved compared to the conventional mixer. The conversion gain of the proposed mixer is given by:

$$
CG=\frac{2}{\pi}\left[2g_{m1}+g_{m5}+\alpha g_{m7}\right]R_L \tag{14}
$$

Where R_L is the load resistor. Although the effective transconductance of the input stage is increased, we have designed the conventional mixer with almost the same conversion gain as the proposed mixer because in order to provide a better comparison in terms of the linearity improvement.

D. Noise Analysis

The common-gate input stage generates more noise than the common-source structure. To reduce this noise, we have used a noise cancellation technique. M_5-M_6 transistors convert the noise voltage at V_1 and V_2 nodes in Fig. 1, which is generated by the noise current of the input transistors, to the currents and inject them to the drain of the input transistors. These noise currents have the opposite sign compared to the noise current of the input transistors. Therefore, they can reduce the NF of the proposed mixer. To further explore the noise cancellation mechanism, we use Fig. 3. Using *KCL* at node V_1, we calculate the injected current to the drain of the input transistor. As discussed already, drain terminals of M_{11} and M_{12} are connected together, and hence, they cancel each other's noise. So, we have:

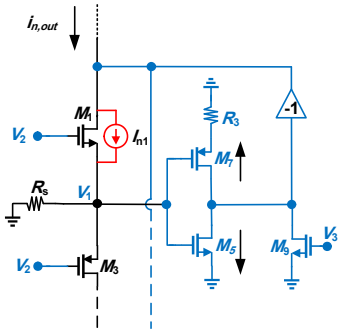

Fig. 3. Equivalent half circuit for noise analysis.

$$
\frac{V_1}{R_s}+2\left(g_{m1}+g_{m3}\right)V_1=I_{n1} \tag{15}
$$

Transistor M_9 has no noise current that is generated by the input transistor's noise current. Using *KCL* at the drain of the input transistor, we calculate the output noise generated by the input transistor as:

$$
i_{n,out}=I_{n1}-2g_{m1}V_1-g_{m5}V_1-\frac{g_{m7}}{1+R_3 g_{m7}}V_1 \tag{16}
$$

By equating (16) to zero, the noise cancelation condition is obtained as:

$$
g_{m5}+\frac{g_{m7}}{1+R_3 g_{m7}}=G_s+2g_{m3} \tag{17}
$$

III. Simulation Results

The proposed mixer is designed for wideband applications that covers the input frequency range of 0.8-5 GHz, and the output IF bandwidth is 50 MHz. The common-gate input transistors are sized to meet the input impedance matching and linearity conditions. In order to have a high conversion gain, the W/L ratio of the input transistors should be high. However, they should not be too large. Otherwise, the gate-source parasitic capacitance is increased and, therefore, the high frequency operation will be limited, and also, the mixer will have more NF. Other transistors are sized to meet the linearity and noise cancellation conditions. For MOS devices, we have used RF models, and rnpoly for resistors, and metal-insulator-metal (MIM) for capacitors because MIM capacitors have better linearity compared to MOS capacitors. Fig. 4 shows the layout of the proposed

mixer in 65 nm RF-CMOS technology. Without the pads, the total die area is 0.4973×0.5703 mm^2.

The circuit simulations are done using RF-CMOS 65 nm technology with 1 V supply voltage. Fig. 5(a) shows the simulation results of conversion gain for the proposed mixer versus the power of the local oscillator (LO). The maximum conversion gain of 11.2 dB happens at 1 dBm LO power (P_{LO}). Therefore, P_{LO} of 1 dBm has been chosen for the rest of the simulations. Fig. 5(b) shows the simulation results of conversion gain for the proposed and conventional mixers versus input RF frequency. As discussed earlier, initially, both mixers were designed to have approximately the same conversion gain. The little difference is because of the improved effective transconductance according to (14). The PVT simulation results of the conversion gain are illustrated in Fig. 5(c). Owing to using a constant-g_m bias circuit, the conversion gain changes are reasonable over PVT variations.

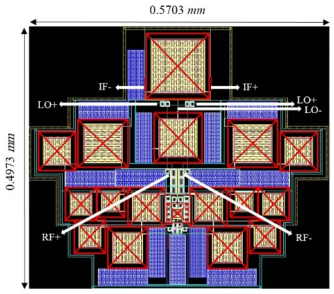

Fig. 4. Layout of the proposed mixer.

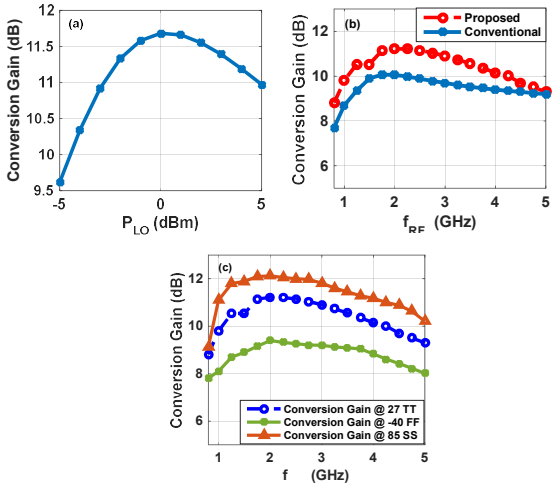

Fig. 5. Simulated conversion gain of the (a) proposed mixer versus P_{LO}, (b) proposed and conventional mixers versus input RF frequency, and (c) conversion gain PVT simulation results of the proposed mixer.

Fig. 6(a),(b) shows the simulated IIP3 of the proposed and conventional mixers. At input frequency of 2 GHz, the IIP3 of the proposed mixer is improved about 9.6 dB. The proposed mixer has higher IIP3 compared to the conventional mixer within the input frequency range. The different IIP3 values are because of the variation in magnitude and phase of IM3 at different frequencies. As shown in Fig. 6(c), the IIP3 of the proposed mixer is improved 6.81 dB on average compared to the conventional mixer. To investigate the effect of mismatch between device components of the proposed circuit on the IIP3, Monte Carlo simulation is done and Fig. 6(d) shows the results. The mean value of the IIP3 is 13.5 dBm, which shows that the mismatch between device components has a minor effect on the. Moreover, the simulated IIP3 over PVT variations is shown in Fig. 7 indicating almost robust performance over PVT. Fig. 8(a) depicts the Monte Carlo simulation results for IIP2 of the proposed mixer at 2 GHz input frequency. IIP2 at this frequency is 57.24 dBm. Monte Carlo simulations have been done for the entire input frequency range and the results are shown in Fig. 8(b). The proposed mixer has higher IIP2 compared to the conventional mixer within the input frequency range. This improvement is about 8.34 dB on average. In addition, PVT simulations of IIP2 have been taken into account and the results are shown in Fig. 8(c).

Fig. 9(a) illustrates the NF simulation results of the proposed and conventional mixers at 2 GHz input frequency. As it is seen, the proposed mixer has less NF than the conventional mixer, which shows the good performance of the proposed noise cancellation technique. Fig. 9(b) depicts the simulated NF versus input frequency range. The improvement is 4.15 dB on average for 1.5-5 GHz input frequency range. Moreover, the PVT variations are considered for NF simulation, and the results are illustrated in Fig. 9(c).

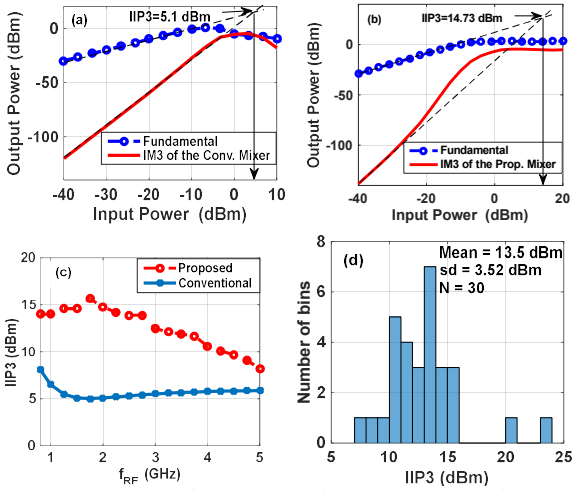

Fig. 6. Simulated IIP3 of the (a) conventional and (b) proposed mixers at 2 GHz, (c) IIP3 of conventional and proposed mixers versus input RF frequency, (d) IIP3 Monte Carlo simulation results of the proposed mixer at 2 GHz.

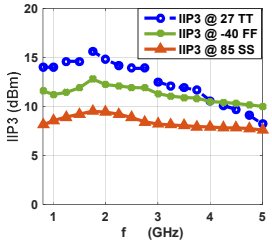

Fig. 7. PVT simulation results of the IIP3.

Table I summarizes the simulation results of the proposed mixer in PVT conditions. The proposed mixer almost has a robust performance against PVT variations. In order to further verify the performance of the proposed mixer, its results are compared with several mixers in Table II. For a fair comparison among these mixers, the following figure of merit is used (FoM) [5], where BW represents the RF input bandwidth, Gain is the conversion gain, IIP3 denotes the average third-order input intercept point, P_{dc} is the power consumption, and F_{DSB} represents the DSB noise factor of the mixer.

Table II. Performance comparison with several CMOS active mixers.

Reference		Freq. (GHz)	$IIP3_{avg}$ (dBm)	$IIP2_{avg}$ (dBm)	$NF_{(DSB)avg}$ (dB)	CG_{avg} (dB)	V_{DD} (V)	Power (mW)	Process (nm)	Area (mm^2)	FoM (GHz)
TCAS-II'21 [1][a]		2.4	7.6	59	10.5	12.5	1	1.2	65	0.22	-
TMTT'10 [6][a]		1 – 10.5	-2.4	-	7.8	12.8	1	5	65	0.011	4.14
JSSC'15 [7]		0.85 – 1.8	3.7 – 5.3	57	5.8	7.2 – 9.3	1.2	1.92	110	-	3.32
TCAS-I'18 [8][a]		76 – 84	1	-	15	-8	1.2	213	65	0.68	0.00025
CSSP'17 [9][a]		0.1 – 2	-0.9	67.13	11.1	17.5	1	4.6	180	0.071	1.6
Conventional mixer[b]		0.8 – 5	5.715	52.1	16.971	9.455	1	8.5	65	-	0.333
Proposed mixer[b]	Pre-layout	0.8 – 5	12.53	60.45	11.2	10.4	1	13.95	65	-	4.85
	Post-layout	0.8 – 5	11.83	57.3	11.53	9.8	1	13.95	65	0.284	3.46

[a] Measurement results, [b] NF at 25 MHz

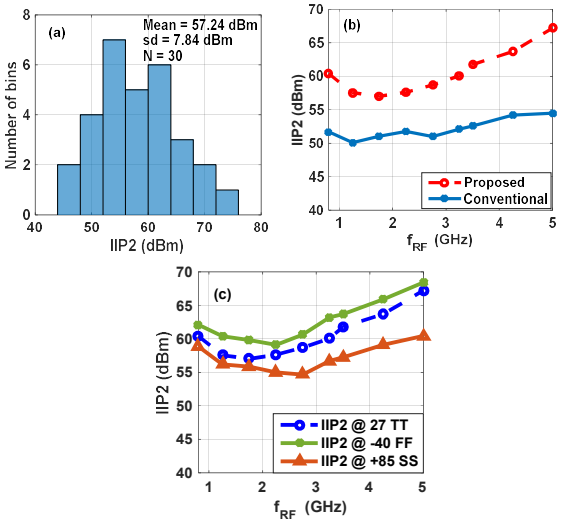

Fig. 8. (a) IIP2 Monte Carlo simulation results of the proposed mixer at 2 GHz, (b) Simulated IIP2 of the proposed and conventional mixers, (c) IIP2 PVT simulation results of the proposed mixer.

$$FoM\ (GHz) = \frac{BW\,(GHz) \times Gain\,(Lin) \times IIP3\,(mW)}{P_{dc}\,(mW) \times \left[F_{DSB}\,(Lin) - 1\right]} \qquad (18)$$

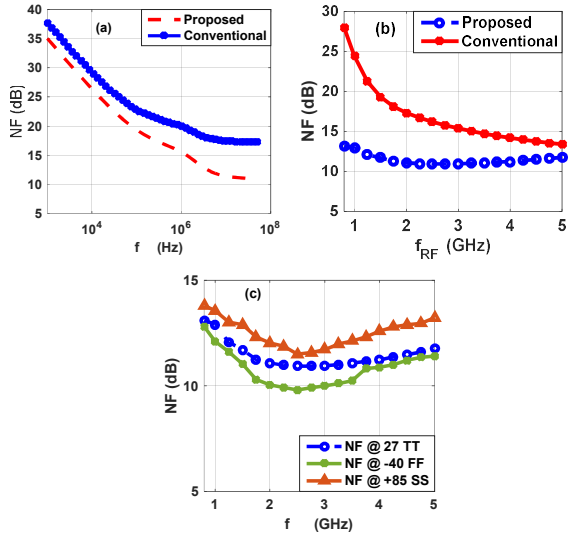

Fig. 9. (a) Simulated NF of the proposed and conventional mixers at 2 GHz input frequency, (b) Simulated NF versus input frequency range; (c) NF PVT simulation results.

IV. Conclusion

In this paper, a CMOS active downconversion mixer is proposed for wideband zero-IF receivers. This mixer has a high level of linearity and lower noise figure compared to the conventional Gilbert mixer. IM2 injection and derivative superposition techniques have been implemented to improve the linearity. The proposed mixer has a robust performance

Table I. PVT simulation results of the proposed mixer.

Parameter	TT @ +27°C, 1 V	FF @ -40°C, 1.1 V	SS @ +85°C, 0.9 V
CG (dB)	8.82 – 11.22	7.8 – 9.4	9.12 – 12.2
IIP3 (dBm)	8.2 – 15.65	10 – 12.8	7.6 – 9.5
IIP2 (dBm)	57.02 – 67.2	59.1 – 68.43	54.67 – 60.2
NF (dB)	10.93 – 13.96	9.8 – 12.8	11.5 – 13.8
Power (mW)	13.95	14.9	13.2

PVT variations, and it can be used for a wide input frequency range without using inductors.

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