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Adapted near-state PWM for dual two-level inverters in order to reduce common-mode voltage and switching losses

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Amir Aghazadeh[1] ✉, Naser Khodabakhshi-Javinani[1], Hamed Nafisi[1], Masoud Davari[2], Edris Pouresmaeil[3]

[1]*Electrical Engineering Department, Amirkabir University of Technology, 424 Hafez Avenue, Tehran PC: 15916-34311, Iran*
[2]*Department of Electrical and Computer Engineering, Georgia Southern University (Statesboro Campus), Statesboro, GA 30458, USA*
[3]*Department of Electrical Engineering and Automation, Aalto University, 02150 Espoo, Finland*
✉ *E-mail: amir_aghazadeh@aut.ac.ir*

Abstract: In this paper, a near-state pulse-width modulation (NSPWM) algorithm is proposed and implemented on dual-two-level voltage-source inverters (D2L-VSIs) in order to reduce the common-mode voltage (CMV), the inverter switching losses, the current total harmonic distortion, and the side effects of bearing currents --compared with space vector modulation (SVM) and PWM7. To gain these goals, two conventional two-level inverters of the D2L-VSI are controlled, separately, with specific switching sequences and an adjusted phase difference between the carriers of two inverters. For evaluating and comparing these PWM techniques mathematically, both CMV root mean square generated and switching losses of the D2L-VSI are formulated as a function of the power factor of the D2L-VSI, which is driven by the methods detailed in this study. Eventually, theories and analysis, as well as simulations and experimental results --which are generated by MATLAB/Simulink environment and a 300 W scaled-down D2LVSI prototype, respectively --authenticate the superiority of the proposed NSPWM over both SVM and PWM7.

1 Introduction

Different types of inverters, thanks to the recent advances in the field of power electronics industry, are utilised in a wide range of industrial applications, ranging from low-voltage, low-power devices (such as micro-inverters used in household photovoltaic systems [1]) to high-voltage (HV), high-power systems (such as electric motor drive [2], active filters [3, 4], and HV direct current electric power transmission systems [5–8]). Regarding all considerable advantages offered by industrial inverters, all of them – especially multi-level (ML) inverters – suffer from complicated pulse-width modulation (PWM) techniques [9], unbalanced neutral point voltages [10], and so on. Among all ML inverters, dual-two-level voltage-source inverters (D2L-VSIs) proposed in [11] are being prevalent since D2L-VSIs compared with other ML inverters operate with the half dc-link voltage [12] and simple controlling method with no need to control neutral point voltages [13]. Owing to these benefits, D2L-VSIs are being widely employed to drive electric motors [14], transportation devices [15, 16], electric power generation [17], and grid-connected systems [18].

The presence of triple harmonic currents in motor phase current, also commonly known as zero-sequence current (ZSC), leads to a core saturation, a higher-current total harmonic distortion (THD), and copper losses. The aforementioned presence of triple harmonic currents and its consequences are the main drawbacks of the D2L-VSI. To eradicate ZSC and its harmful effects on the D2L-VSI, a large number of efforts have been reported to add extra hardware [19] and utilising rich switching [20, 21]. While adding extra windings incurs extra expenses and difficulties to determine the size of windings, using switching redundancies is not capable of taking all advantages of the D2L-VSI, especially at high modulation indexes (MIs) and voltage THDs.

When ZSC flows, which is caused by the generated zero-sequence voltage (ZSV) on the path provided by the structure of single dc source D2L-VSI, using D2L-VSIs with isolated dc sources is able to eliminate ZSC completely since there is not any path for ZSC to flow [11, 22]. By using an isolating transformer to isolate dc sources, common-mode current (CMC) could not flow from the frame of electric motors to ground, star-point of the three-phase supply, and finally mid-point of the dc-link capacitors due to the fact that the secondary windings are not grounded [23]. Although D2L-VSIs with two isolated dc sources do not suffer from the ZSC and CMC – similar to other kinds of inverters, shaft voltage, bearing currents – they contain capacitive bearing current (dv/dt) and electric discharge machining (EDM) currents. Thus, electromagnetic interference problems are brought by CM voltage (CMV) [24, 25]. Inspired by a growing body of studies carried out to reduce or eliminate CMV in both two-level 2L [26, 27] and ML inverters [28–30], substantial efforts have been devoted to reduce the harmful effects of CMV in D2L-VSIs. The point that deserves to be asserted here is that in most studies the ZSV was delineated instead of the CMV in case of D2L-VSIs with single dc source [31]. However, up to now, far too little attention has been paid to consider the CMV for D2L-VSIs with isolated dc sources. A passive second-order filter called CM filter containing an inductor, a capacitor, and a resistor is introduced in [32] as a solution to reduce generated CMV in D2L-VSI with isolated dc sources. It is pertinent to note that in order to eliminate the generated CMV, two CM filters must be installed at both sides of an open-end induction motor – which is leading to increasing the setup and maintenance costs especially at HV, high-power applications. In [33], a modified CM filter known as the single CM filter is proposed which is only connected to one side of the open-end induction motor. Consequently, the setup and maintenance costs decrease significantly. However, for HV, high-power applications, it still incurs considerable expenses. Making use of rich switching redundancies of D2L-VSI, so as to reduce or eradicate CMV is addressed in [31] leading to introduce 29 PWM methods. Among these methods, some methods are ineffective because of non-idealities and dead time effects. Between all remaining methods, three PWMs are selected and identified as PWM7, PWM9, and PWM15 that not only reduce CMV and dv/dt current effectively, but also eliminate EDM currents completely. Nevertheless, these methods also suffer from notable weaknesses. For instance, PWM9 and PWM15 suffer from double switching problem that increases the switching losses of D2L-VSI. In addition, PWM9 undergoes a higher-voltage THD compared with that of other methods. As a conclusion, PWM7 has superiority over PWM9 and PWM5 since it does not undergo double switching problem and has the same