Introduction and Advantage of Space Opposite Vectors Modulation Utilized in Dual Two-Level Inverters With Isolated DC Sources

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***Abstract*—In this paper, space opposite vectors modulation (SOVM) is proposed to decrease common-mode voltage (CMV), and also improve inverter switching losses compared to pulsewidth modulation 7 (PWM7) for dual two-level inverters (DTLI). Employing the control simplicity of DTLI to achieve multilevel winding voltages, the two conventional two-level inverters of DTLI are independently controlled; consequently, the capability of adjusting phase difference between the carriers (PDC) of two inverters is established. To mathematically evaluate and compare the performance of DTLI driven by SOVM and PWM7, CMV and losses for different PWMs are formulated. Moreover, contour, three- and two-dimensional analyses are conducted to investigate the effects of PDC and modulation index on CMV, voltage total harmonic distortion (THD), voltage weighted THD and switching losses. All theoretical bases, simulation results from MATLAB/Simulink and experimental results conducted by a DTLI prototype validate the superiority of SOVM over PWM7.**

***Index Terms*—Common-mode voltage (CMV) reduction, dual two-level inverter (DTLI), inverter losses, isolated dc sources, pulsewidth modulation 7 (PWM7), space opposite vector modulation (SOVM).**

I. Introduction

THANKS to spectacular advances made in the field of power electronics and semiconductor devices, different types of inverters are employed in a wide range of industrial applications, from low-power ones such as electric vehicles (EVs) [1], [2] to high-power high-voltage purposes like high-speed trains [3]. While a variety of inverters enormously suffer from complicated pulsewidth modulations (PWMs) [4], unbalanced neutral point voltages [5], and power quality management [6], dual two-level inverters (DTLIs) and dual multilevel inverters (DMLI) have been introduced [7]. These types of inverters are getting popular since they need fewer dc sources with half of the voltage required by neutral point clamped (NPC) multilevel inverters [8], no control of neutral point voltages, simple controlling methods, and minimal operation costs [9]. These advantages make dual inverters (DIs) suitable to drive electric motors [10], EVs [11], [12], doubly fed reluctance generators [13], and grid-connected systems [14].

Zero sequence voltage (ZSV), which is termed as common-mode voltage (CMV) in some studies, is the major disadvantage of DIs with common dc sources. This term creates triplen harmonic currents known as zero sequence current (ZSC) in motor phase currents, which lead to destructive effects such as core saturation, higher current total harmonic distortion (THD), and copper losses. To limit ZSC, a great deal of studies have been undertaken [15]–[18]. Whereas imposing extra hardware and expenses by some of the literature [18], employing rich switching redundancies of DI is an alternative adopted by other researchers to eliminate ZSC for DTLIs [15]–[17] and DMLIs [16]–[19]–[24]. In these studies, vectors are selected in such a way that ZSV generated by DIs is completely eliminated. Furthermore, the methods addressed in [20]–[23] and [24] are able to not only suppress ZSV but also control dc-link voltages, which play a pivotal role in guaranteeing the appropriate performance of DMLIs.

Utilization of isolated dc sources is another possible way to completely eliminate ZSC as addressed in [7]–[25]. This structure not only eliminates ZSC due to the lack of any path for triplen harmonic currents to flow, but also achieves winding voltages with lower voltage THD in comparison to DMLI with common dc sources. Although ZSC is eliminated entirely by utilizing two isolated DC sources, similar to other kinds of inverters, DTLI and DMLI suffer from CMV, which is responsible for shaft voltages, bearing currents (with *dv/dt* and electric discharge machining (EDM) currents as its transient parts), and electromagnetic interference (EMI) problems [26], [27]. Likewise, current literature concerning CMV reduction [28], a modified carrier-based modulation scheme to reduce the third harmonic component of CMV [29], and auto-screening carrier phase-shift scheme to suppress EMI problems causing

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